Application Report
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Achieve 20-A Circuit Protection and Space Efficiency Using Paralleled eFuses

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ABSTRACT

Today Texas Instrument's eFuse devices are sought-after to replace discrete frontend protection circuits in many applications. These eFuses are available in the current range from 0.1 A to 12 A. However, certain applications like servers and communication equipment demand currents in the range of several tens of amperes. In general, device paralleling is seen as the first option by the system designers to scale the system for higher current requirements and better thermal management. While these devices are operated in parallel, it is essential that individual e-fuse share equal or near to equal load current for proper system operation and dynamic response. This application note describes the design considerations and performance characteristics of using eFuses in parallel configuration. An example of paralleling four eFuse devices to support 20-A load current is considered here to demonstrate load current sharing performance and to illustrate device behavior during transient overload, short-circuit events.

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1 Introduction

In this application, the TPS259241 device from the TPS2592xx family is considered for parallel operation. The TPS259241 device has an integrated power switch which is controlled to manage current, voltage, and the output voltage ramp profile to a connected load. Figure 1 shows the block diagram of the TPS259241 device. The basic operation of eFuse is as follows. Once the eFuse is enabled, the integrated power switch is controlled in linear-mode to match the desired output voltage ramp. After a successful start-up sequence, integrated power switch is fully turned-on just like a power switch to minimize voltage drop in the power path. If at any point the load current reaches the set current-limit level I_{LIM}, the gate control transits the integrated power switch into linear mode. This increases ON resistance and corresponding voltage drop across the eFuse to provide constant output current. The inherent current source characteristic of eFuse helps to a great extent for successful parallel operation.

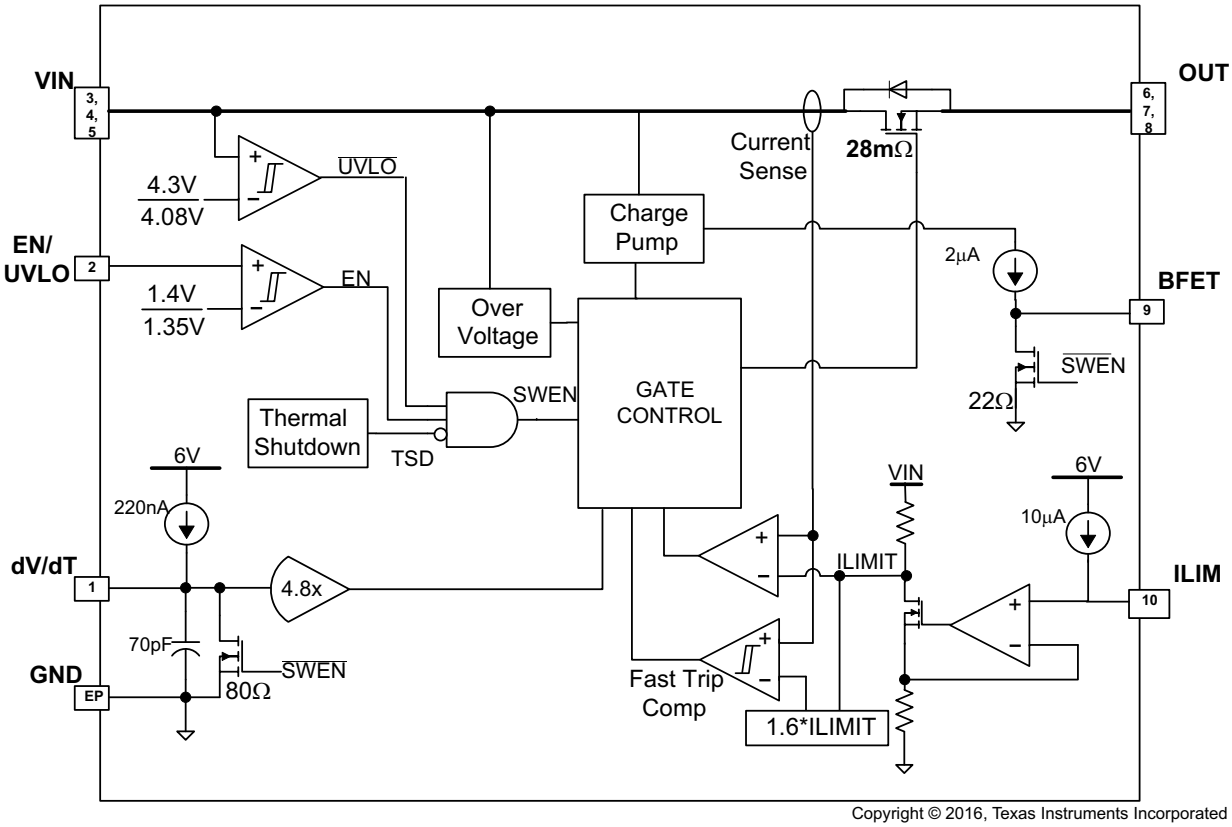

Figure 1. TPS259241 Block Diagram

The ramp time (T_{dVdT}) of output voltage can be adjusted by configuring the external capacitor (C_{dVdT}) at dVdT pin using Equation 1. Similarly, the current limit (I_{LIM}) which the device needs to restrict under fault/over load conditions can be configured by setting the current-limit resistor (R_{ILIM}) as per Equation 2.

$$T_{dVdT} = 10^{6} \times V_{IN} \times (C_{dVdT} + 70\ pF) \quad (1)$$

$$R_{ILIM} = \frac{I_{LIM} - 0.7}{3 \times 10^{-5}} \quad (2)$$

2 Parallel Operation of eFuse

When eFuses are operated in a parallel configuration, load sharing among the eFuses is a major challenge. A successful parallel operation ensures equal current sharing among the parallel-connected devices both under steady-state and dynamic conditions. Figure 2 shows the number of “N” eFuse devices connected in parallel configuration. The input and the output terminals are connected together. The following subsections explain how the parallel-connected eFuse devices work in steady state, current limit, and startup modes.

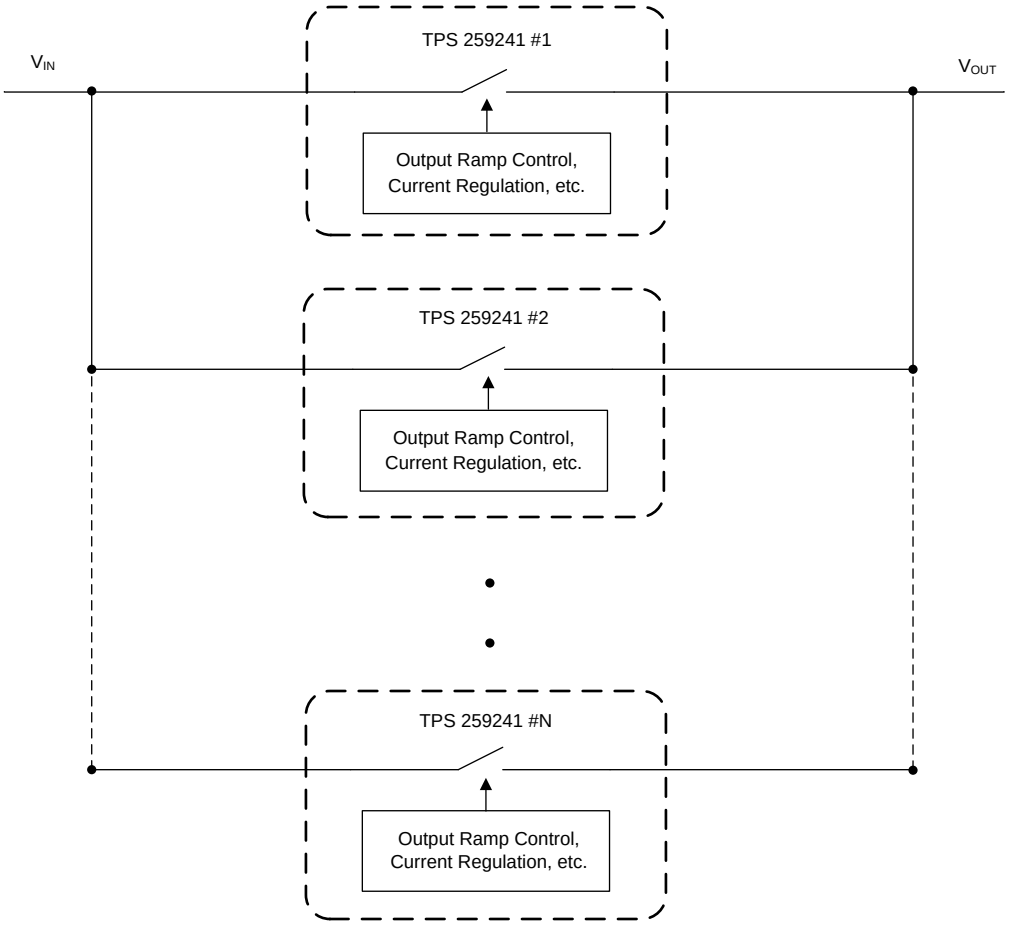

Figure 2. Number of “N” eFuse Devices Connected in Parallel Configuration

2.1 Operation in Steady-State

When none of the eFuse hits the current limit, the ON-resistance $R_{DS(on)}$ of the eFuse becomes the equivalent circuit as shown in Figure 3. During steady-state operation, the current sharing is decided by the $R_{DS(on)}$ mismatch among the parallel-connected eFuse devices. The device having the lowest $R_{DS(on)}$ ($R_{DS(on)\_min}$) shares the highest current (I_{MAX}) than the rest of the devices. For example, one device in the parallel configuration has the lowest $R_{DS(on)\_min}$ and the rest of the devices have the highest $R_{DS(on)\_max}$. The maximum current (I_{MAX}) shared by a device from overall load current (I_{LOAD}) can be obtained using Equation 3.

$$I_{MAX} = \frac{\left(\frac{R_{DS(on)\_max}}{(N-1)}\right)}{R_{DS(on)\_min} + \left(\frac{R_{DS(on)\_max}}{(N-1)}\right)} \times I_{LOAD} \quad (3)$$

The $R_{DS(on)}$ variation for a particular device can be found from the datasheet to calculate the current sharing imbalance. However, the self-heating effect due to positive temperature characteristics of the MOSFET helps to a certain extent towards equal load current distribution in parallel applications. The device with the lowest $R_{DS(on)}$ conducts slightly more load current which leads to a higher junction temperature. This increases ON resistance and slightly reduces its current. A stable operating point is achieved with near to equal current sharing among the parallel-connected eFuses.

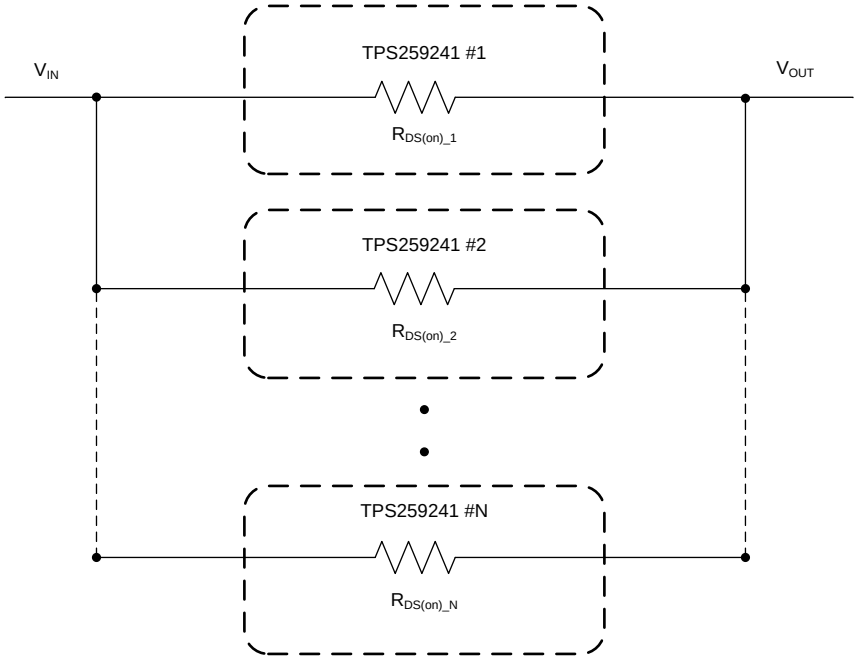

Figure 3. Equivalent Circuit of 'N' Devices in Steady-State Operation

2.2 Operation When One or More Devices Reach the Current Limit

As discussed in Section 2.1, due to the mismatch in the device parameters, one or more eFuses in a parallel configuration may enter current-limit mode. In such a scenario, the internal closed current loop aids in proper system operation. Figure 4 shows the equivalent circuit of N parallel-connected eFuses with one or more devices hitting the current-limit. When device #1 reaches the current-limit level, its control circuitry regulates current to the programmed I_{LIM} value. To facilitate this, the gate drive to its internal integrated power switch is reduced; causing its ON resistance and corresponding voltage drop to increase. This causes the load current to steer towards the other device in parallel, forcing load sharing. In order to achieve this accurately to a larger extent, it becomes necessary to have same programmed current limit for all the devices in parallel configuration. One way to do that is to connect the I_{LIM} pins of all the parallel-connected eFuses and use a single equivalent current programming resistor (R_{ILIM_eq}). This avoids any mismatch in current-limit setting among the devices that could arise due to tolerances in the current-limit resistors. The equivalent current-limit resistor in 'N' array parallel configuration can be calculated using Equation 4.

$$R_{ILIM\_eq} = \frac{I_{LIM} - 0.7}{N \times 3 \times 10^{-5}} \quad (4)$$

where

- R_{ILIM_eq} is the equivalent current-limit programming resistor
- I_{LIM} is the individual eFuse current limit

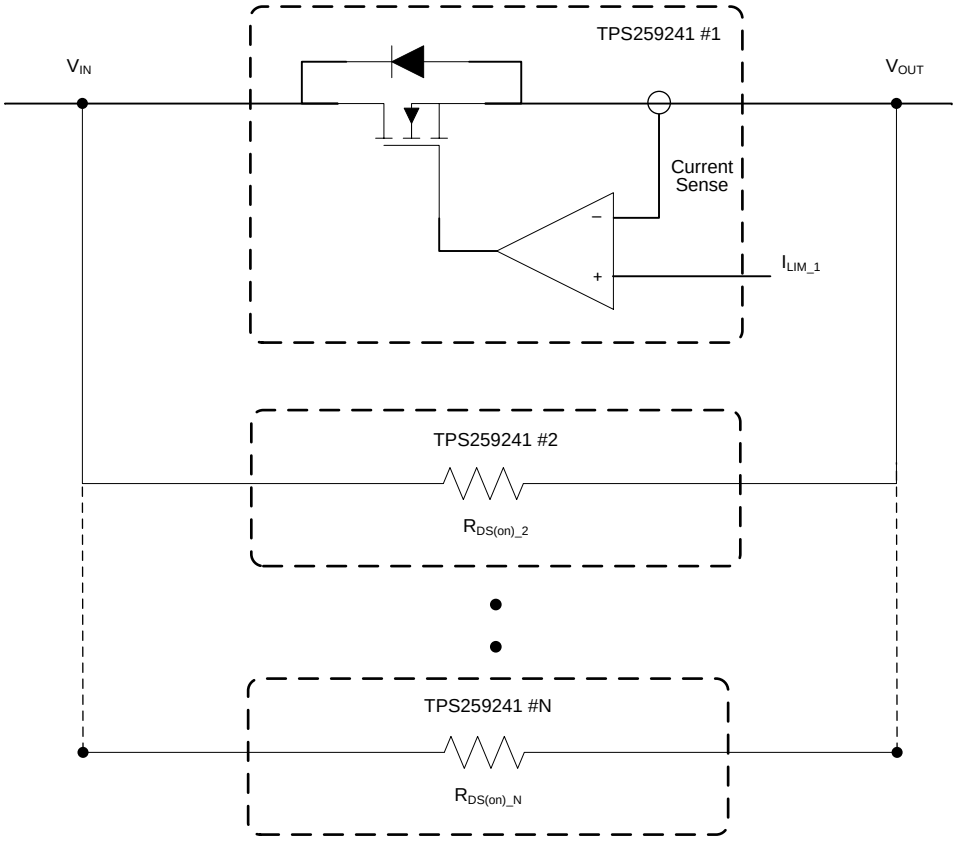

Figure 4. Equivalent Circuit of Parallel-Connected eFuses When One Device Reaches Current Limit

2.3 Operation During Startup

It is important to have equal current sharing among the parallel-connected eFuses during startup to ensure successful startup. Current sharing during startup is dependent on the threshold voltage mismatch among the integrated power switches of eFuses. However, eFuses are generally used for output slew control to limit the inrush current and hence these are slow turn-on devices. The gate drive of eFuse controls the integrated power switch to match the output ramp rate set at the dVdT pin. To have synchronized operation, you must connect “EN/UVLO” pins of all the parallel-connected eFuses. Similarly dVdT pins of all the eFuses should be connected together to ensure uniform output ramp rate and equal dynamic power stress. The equivalent dVdT capacitor in ‘N’ array parallel configuration to achieve output voltage ramp time T_{dVdT} as that of a single device is calculated using Equation 5.

$$C_{dVdT\_eq} = \left(\frac{N \times I_{dVdT} \times GAIN_{dVdT} \times T_{dVdT}}{V_{IN}} \right) - \left(N \times C_{INT} \right) \quad (5)$$

where

- C_{dVdT_eq} is the equivalent capacitor at the dVdT pin
- I_{dVdT} = 220 nA (typ)
- $GAIN_{dVdT}$ = 4.85
- C_{INT} = 70 pF (typ)
- V_{IN} is the input voltage

3 Application Circuit Schematic for 20-A Load Support

Figure 5 illustrates the TPS259241 circuit schematic.

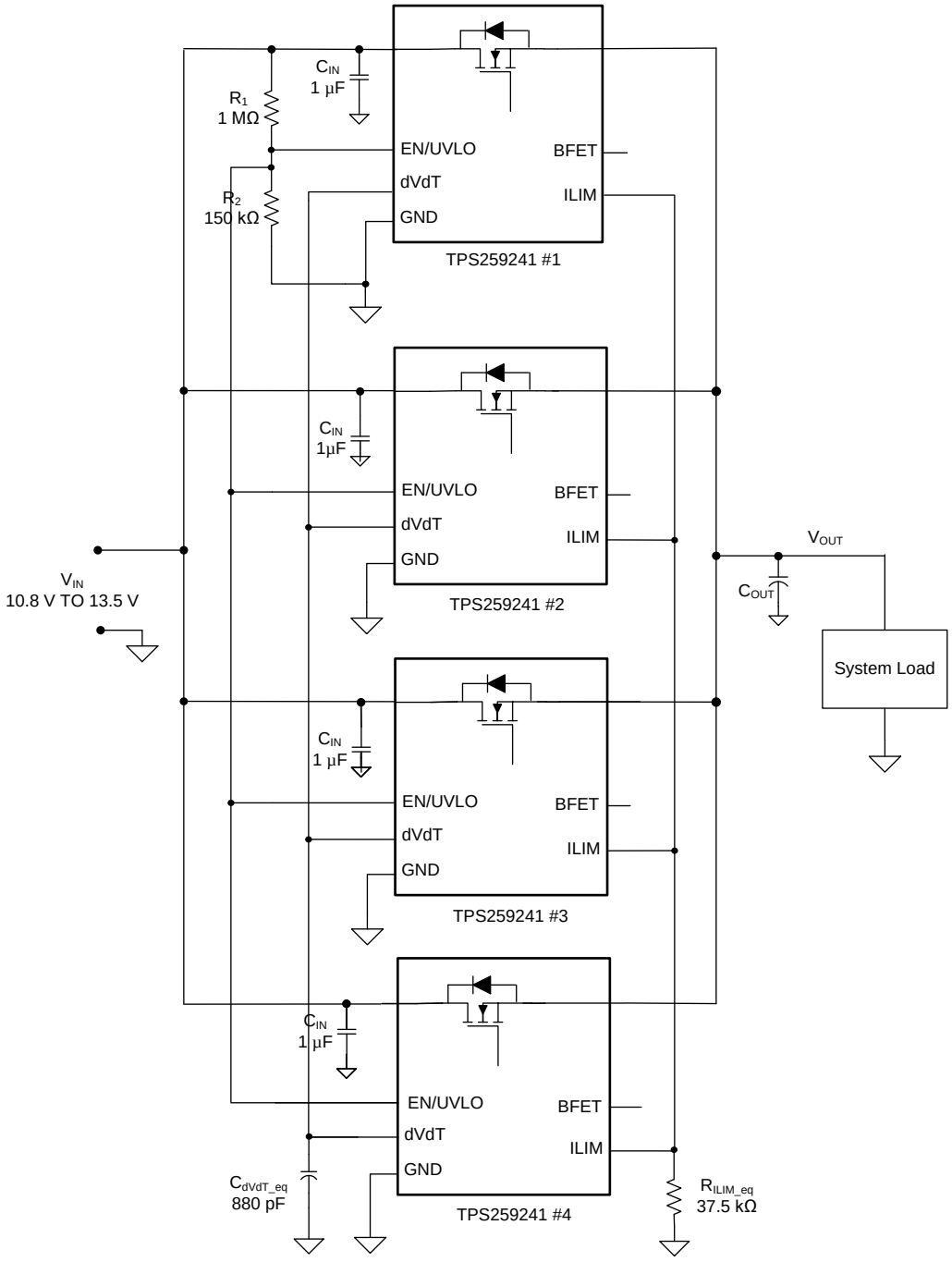

Figure 5. TPS259241 Devices Connected in Parallel to Support 20-A Load Current

4 Performance Results

In this section, test results are presented to demonstrate eFuse performance in a parallel configuration. Figure 6 shows the current sharing performance of four-phase eFuse parallel configuration in steady-state operation. The difference between the average load current and the current of any phase is within ±70 mA in the whole load range. The maximum current sharing error at full load is less than 3%.

Table 1. Design Parameters

Design Parameter	Example Value
Input voltage range, V_{IN}	12 V
Undervoltage lockout set point, $V_{(UV)}$	10.8 V
Overvoltage protection set point, $V_{(OV)}$	Default: V_{OVC} = 15 V
Current limit, I_{OL}= I_{ILIM}	20 A
Load capacitance, C_{OUT}	10 µF
Load, R_L	0.6 Ω

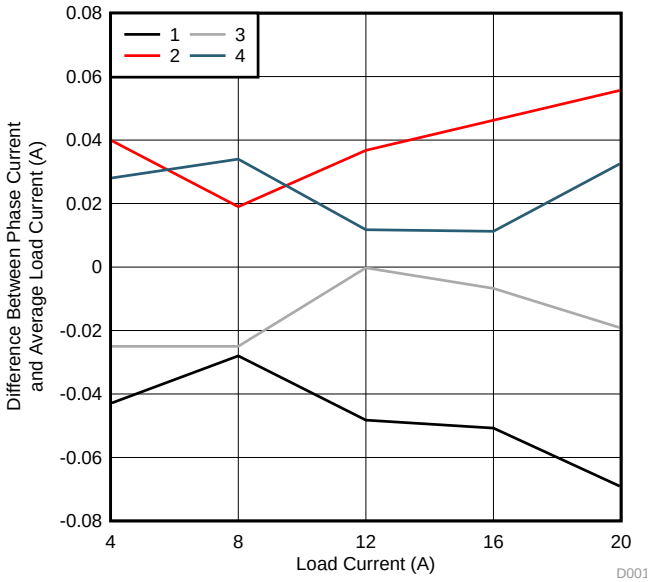

Figure 6. Steady-State Current Sharing of Four-Phase eFuse Parallel Configuration

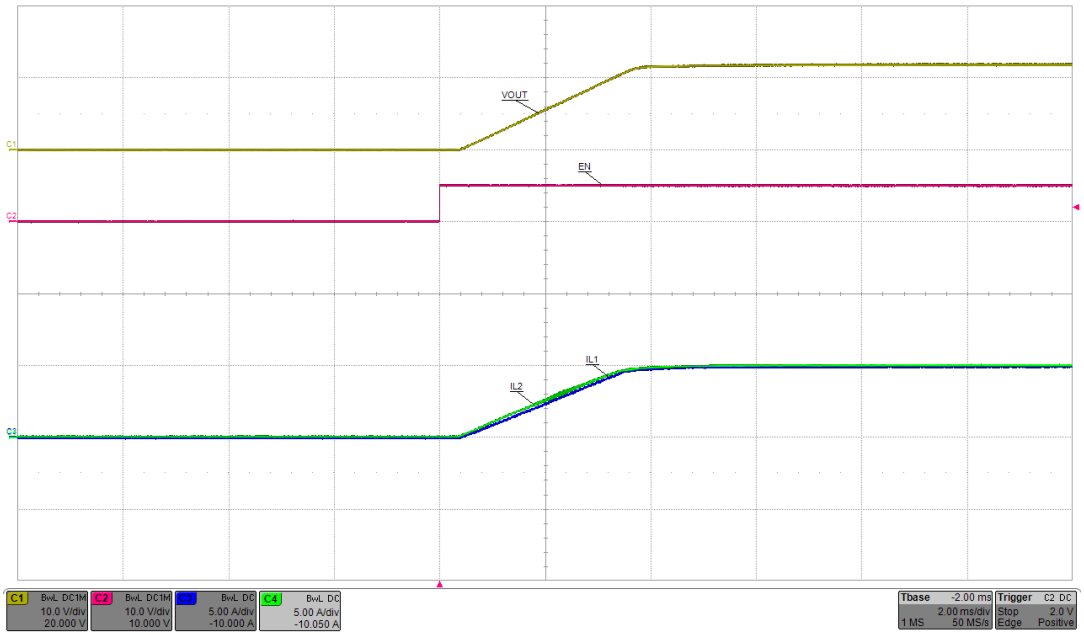

Figure 7. Current Sharing Among Two Devices During Output Voltage Ramp

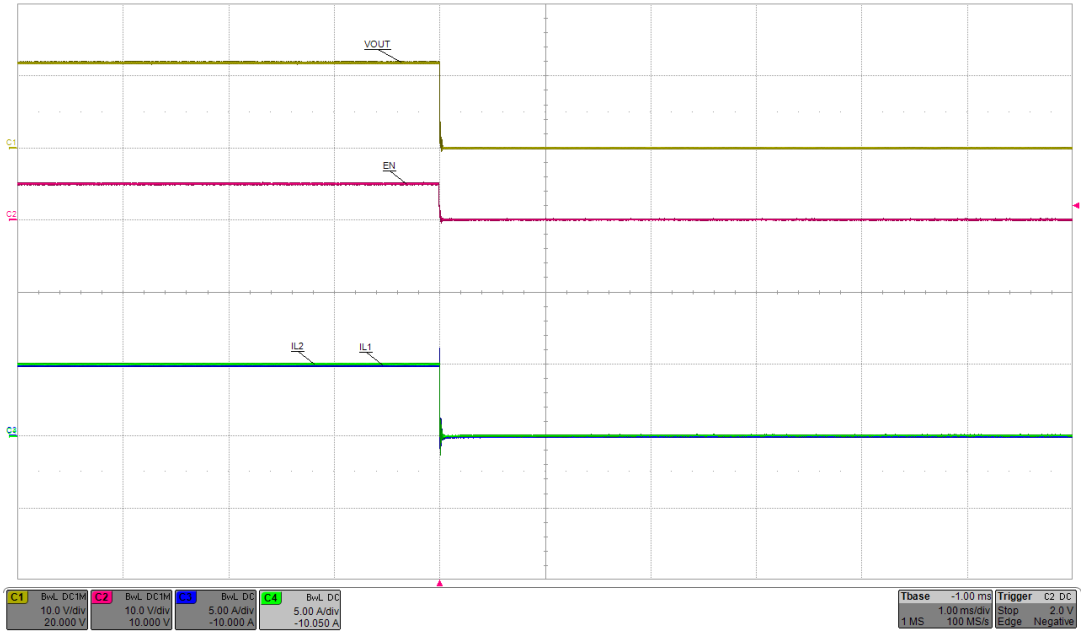

Figure 8. Current Profile of Two Devices During Shut-Off

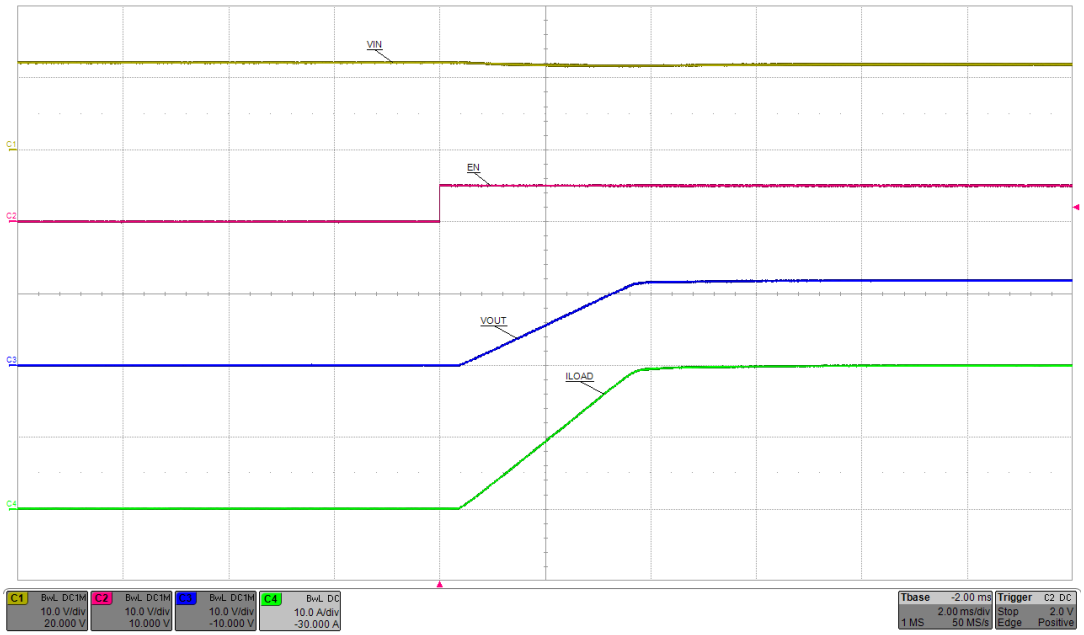

Figure 9. Load Turn-On Behavior of 20-A eFuse With Enable-On

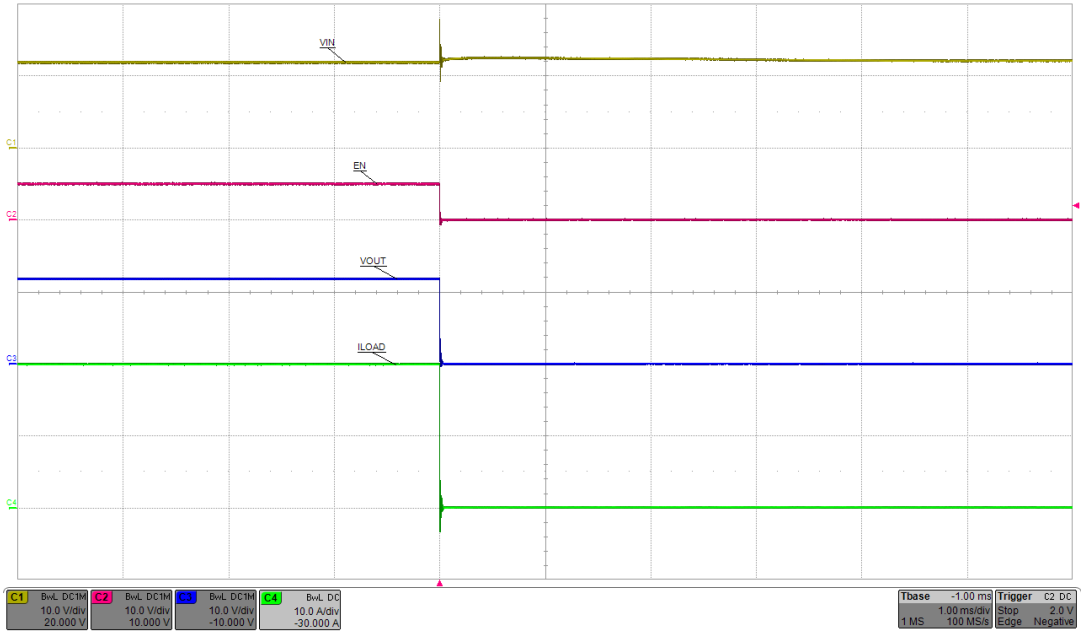

Figure 10. Load Turn-Off Behavior of 20-A eFuse With Enable-Off

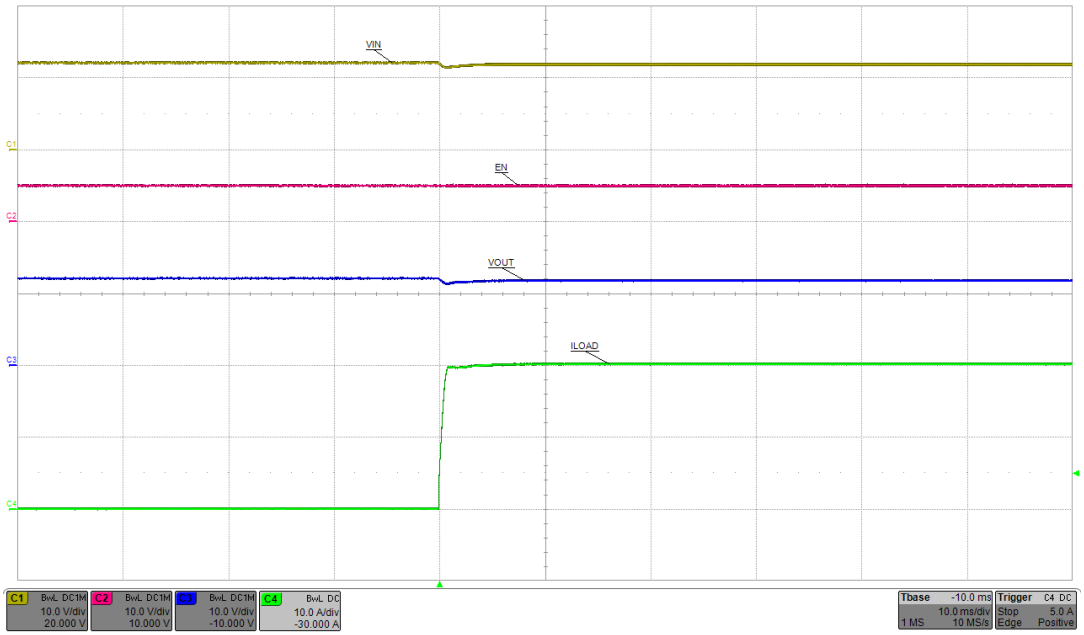

Figure 11. 20-A Load Step-Up Response of Four-Phase eFuse Parallel Configuration

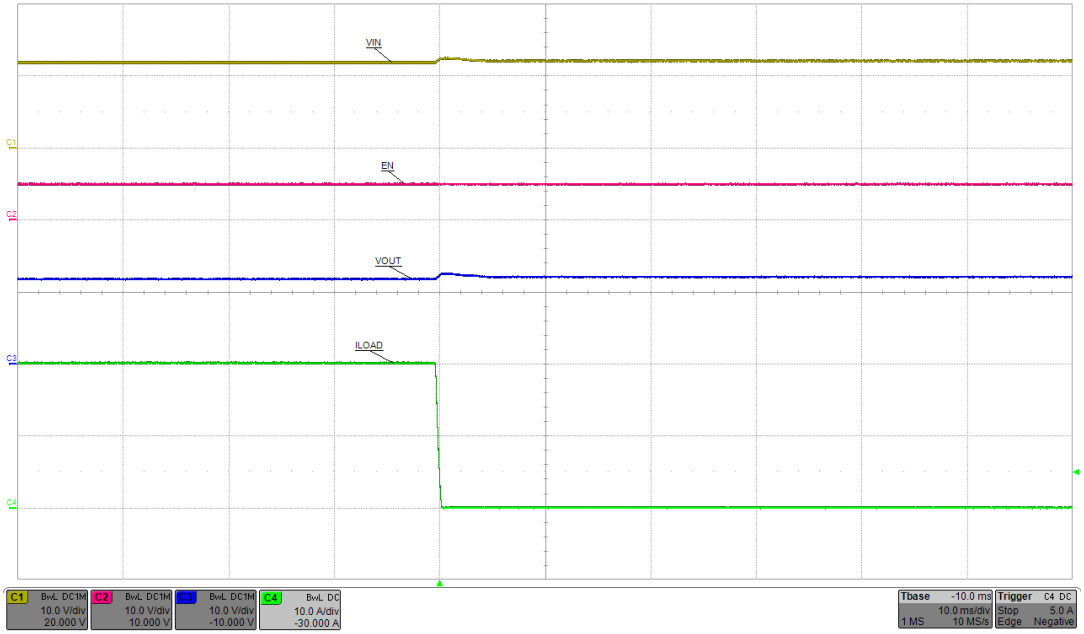

Figure 12. 20-A Load Step-Down Response of Four-Phase eFuse Parallel Configuration

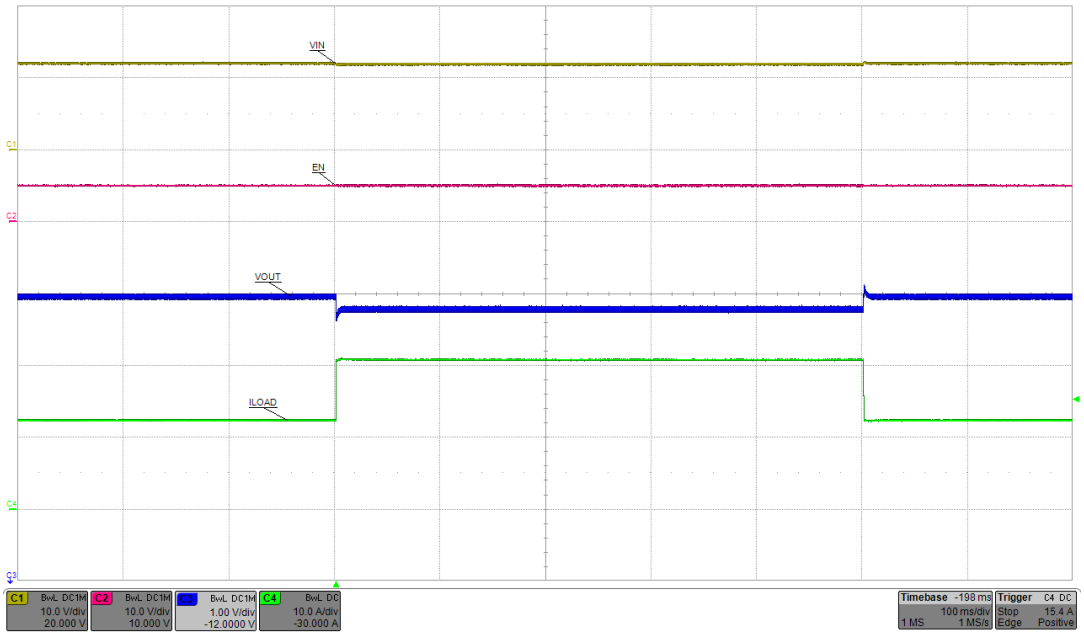

Figure 13. Transient Overload Response of 20-A eFuse

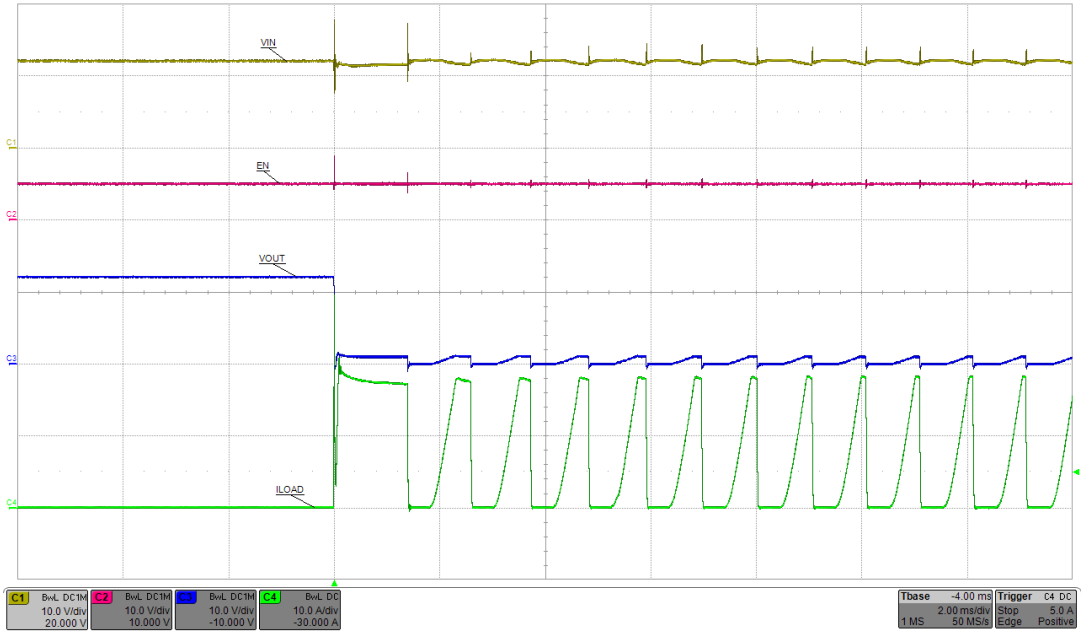

Figure 14. Output Short-Circuit Response of 20-A eFuse

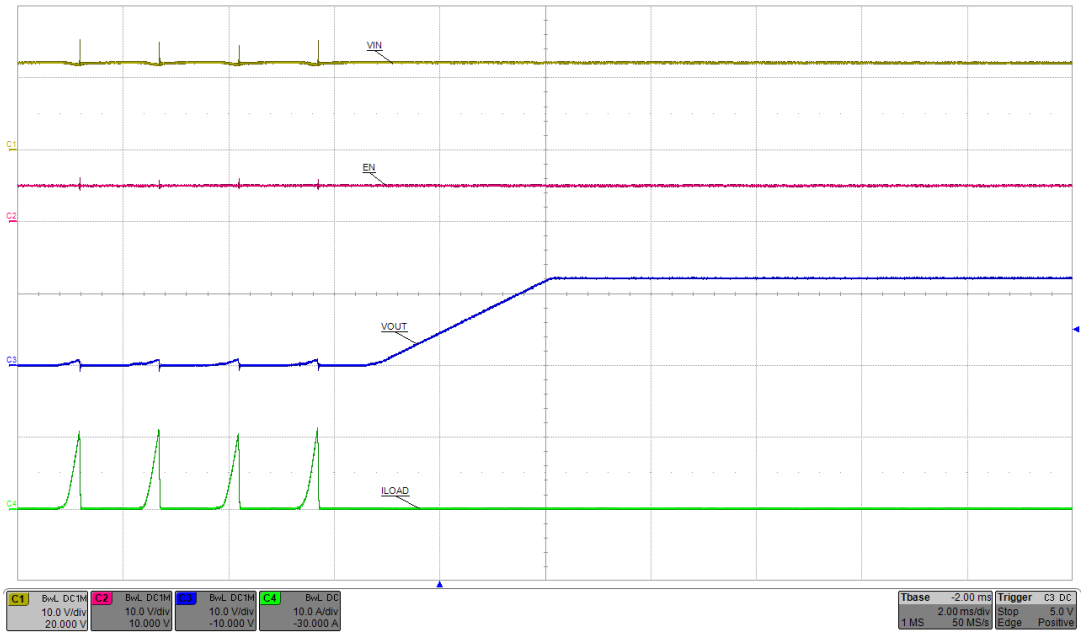

Figure 15. Recovery From Output Short Circuit

5 Comparison with External FET Solution

In this section, the basic space-efficiency comparison between the eFuse solution and the external FET solution is carried out for a 20-A load circuit protection. Only the critical space occupying components are considered and are shown in Table 2. The eFuse solution uses four TPS259241 devices, each are 3 mm × 3 mm and occupies a space of 36 mm^2 on the board. The external FET solution, for example, a TPS24720 hot-swap controller with two external FETs (CSD16401Q5, SON package, and 5 mm × 6mm) and a current sense resistor (1 W, 1210 package, and 3.2 mm × 2.5 mm) occupies 77 mm^2 on the board.

Table 2. Area of Critical Space Occupying Components

Component	eFuse Solution		External FET Solution	
	Part Count	Area (mm2)	Part Count	Area (mm^2)
Controller IC	4	3 × 3	1	3 × 3
External FET	0	0	2	5 × 6
Current Sense Resistor	0	0	1	3.2 × 2.5
Total Area (mm^2)	**36**		**77**	

6 Conclusion

In this application note, four TPS259241 devices are used in parallel to meet 20-A circuit protection, but the approach can be easily extended for other current levels. Parallel eFuse configuration also helps the system designers for better thermal management as the power loss is spread across multiple devices. For more information on the TPS259241 eFuse, see http://www.ti.com/product/TPS25924.

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