Space Optimized, "Clam Shell" Layout for Step-Down DC/DC Converters

Jim Perkins, Matthias Ulmann   *Monolithic Catalog Power*

ABSTRACT

An optimized layout is critical to good DC/DC regulator performance, and there have been whole libraries written on DC/DC converter layout. Some really useful articles are Tim Hegarty's three-part series on DC/DC layout published in EDN[1], and Chris Glaser's paper in the *TI Analog Applications Journal*[a]. There are many factors to be considered in achieving a good layout. Some are critical to performance while others are perhaps marginal (and un-proven!).

The demand for smaller electronic products packed with more features means that the most space efficient layout is also desired. DC/DC converter ICs are available in tiny packages and it is generally the inductor which is the largest component. This paper examines the use of both sides of the PCB to achieve the most space efficient DC/DC converter layout while maintaining optimal performance.

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1   Critical Steps in DC/DC Layout

A summary of the key layout steps, in order of priority is:

1. Place the input capacitor as close as possible to the IC with wide, short traces to the V_{IN} and P_{GND} pins. Every millimeter makes a difference! Minimize the area of the loop from C_{IN} to V_{IN} and P_{GND} back to C_{IN}.

2. Place the inductor, as close as possible to the SW pin of the device, keeping the switch node area as small as possible.

3. Place output capacitors from the inductor, returning to the P_{GND} close to the input capacitor. Again minimize the area of the loop from the SW pin through the inductor to C_{OUT} and back to P_{GND}.

4. As in the previous steps, C_{IN}, C_{OUT}, and P_{GND} are connected together to form a return path for the switching currents. This should be connected to the system GND at a single point.

2   Double-Sided Layout

It is generally a good practice to avoid layer changes and hence vias in the power loops described in Section 1. This is because vias add parasitic inductance and can lead to ringing and add to EMI. However, if the vias are directly in series with the inductor they should add to the inductance and not cause parasitic issues. This consideration suggests the IC and other components may be placed on the opposite side of the PCB to the inductor. With the IC and capacitors directly under the inductor footprint, the total PCB area used by the DC/DC converter circuit is minimized.

3   Testing the Theory

In order to test the double-sided layout ideas, a board with three versions of an identical electrical circuit was created, with three different layouts. The circuit uses the TPS563209DDCR 3-A buck regulator in an SOT23 package to convert from 12 V to 2.5 V at 2.5 A. Figure 1 shows the schematic.

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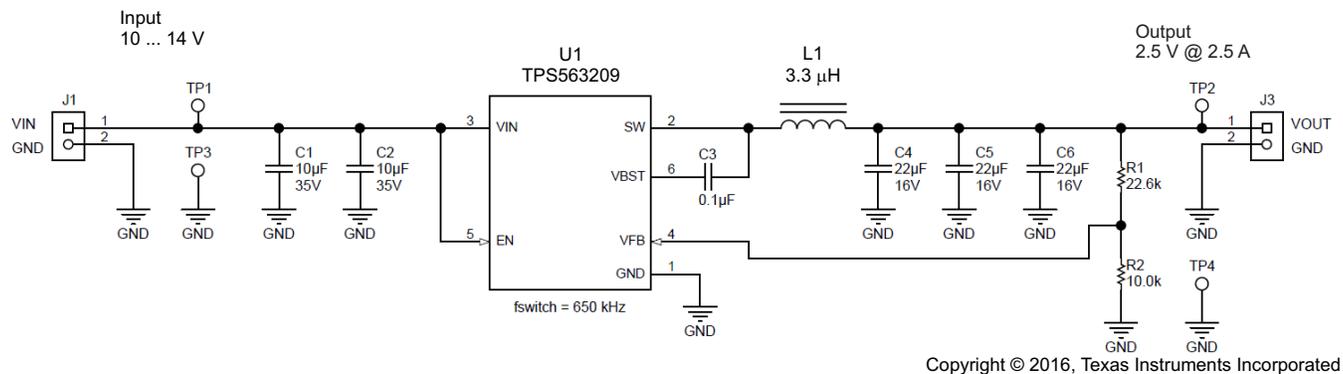
**Figure 1. TPS563209DDCR 12 V to 2.5 V at 2.5 A**

- Input capacitors
  - TDK C3216X5R1V106M160AB
  - 10 µF, 35 V, 20%, X5R, 1206
  - Approx. 6 µF at 12-V DC (-40%)
- Output capacitors
  - TDK C2012X5R1C226M125AC
  - 22 µF, 16 V, 20%, X5R, 0805
  - Approx. 13 µF at 2.5-V DC (–40%)
- Inductor
  - Taiyo Yuden NRS5040T3R3NMGJ
  - 3.3 µH, 30%, 3.3 A at 40°C temperature rise, 4.0 A at 30% inductance drop

The first layout uses an entirely single-sided layout and measures 14.6 mm x 11.9 mm, with an area of 173 mm^2. The second layout has the inductor on the opposite side of the PCB to the IC and capacitors. The inductor on the second layout measures 13.6 mm x 10.4 mm with an area of 141 mm^2. The third layout has the inductor and output capacitors on the opposite side of the board to the IC and input capacitors. This final layout measures a tiny 13.5 mm x 7.8 mm, with an area of 105 mm^2. In both the double-sided layouts, the components on each side are directly above and below each other so the area used is the total area looking through the board.
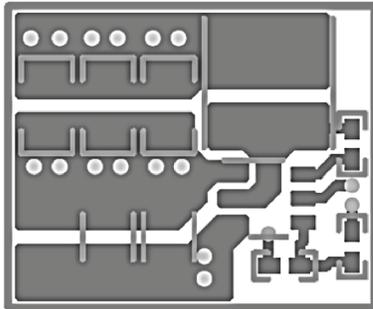

Figure 2. Layout 1 - Single Sided
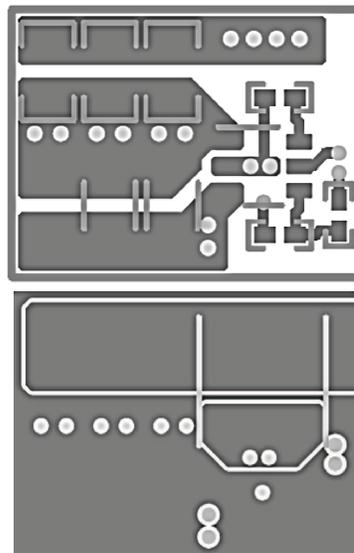
**Figure 3. Layout 2 - Inductor on Other Side**
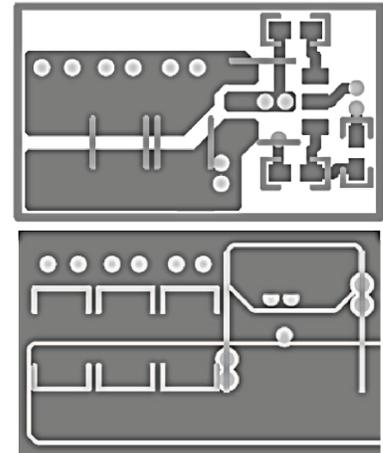
**Figure 4. Layout 3 - Inductor + Output Capacitors on Other Side**

Figure 5 shows the PCBs used for testing the layouts.

Top Side

Bottom Side
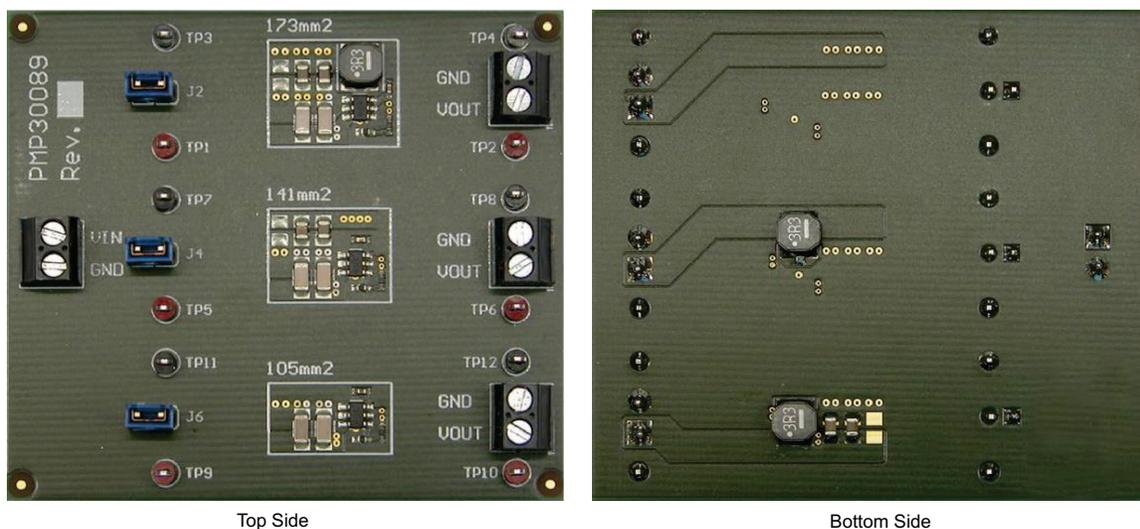
Figure 5. Test PCB

The PCBs used were 4-layer, 1-oz/35-µm copper thickness, FR4 material. Figure 5 illustrates layers 1 and 4. Internal layers 2 and 3 were ground and 12-V, respectively.

3.1 *Results – Output Ripple*

Figure 6, Figure 7, and Figure 8 show the output ripple measured directly across the output capacitors using a coax lead[3].

Figure 6. Output Ripple – 12 V to 2.5 V at 2.5 A. Layout 1
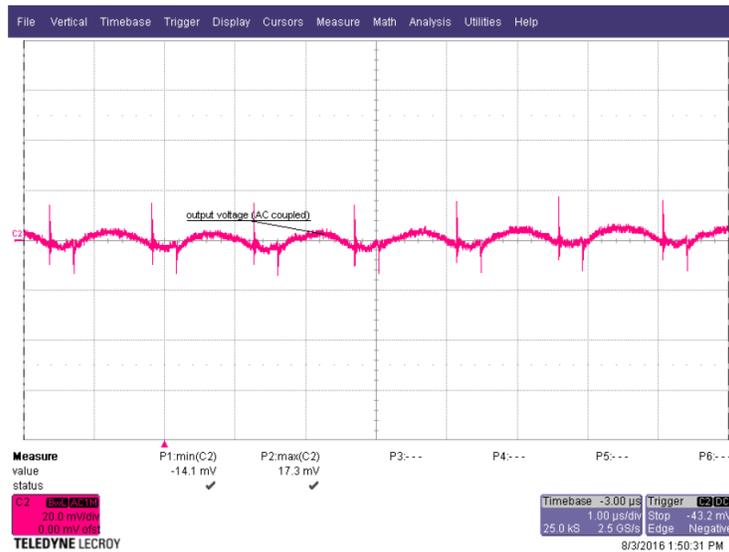
Figure 7. Output Ripple – 12 V to 2.5 V at 2.5 A, Layout 2
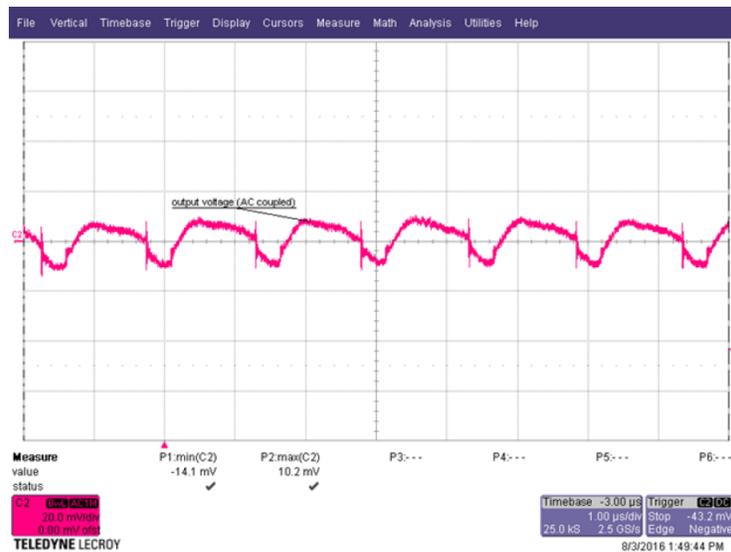
Figure 8. Output Ripple – 12 V to 2.5 V at 2.5 A, Layout 3

There is little difference between the three layouts; although the switching-edge pick up on the single-sided layout 1 is slightly higher. For layout 1, the output ripple amplitude without the ringing edges is about 24 mVpp, with the switching edge ringing taking this to 45 mV. For layout 2, the ripple is lower, approximately 14 mVpp, increasing to 32 mV with switching edge ringing. Layout 3 achieves an output ripple of 24 mVpp with the least switching edge ringing.

It is interesting to note that the orientation of the inductor can make a difference. The inductors, seen in Figure 5, have a dot on one connection. This denotes the start of the winding where the conductor is closest to the central core. The other side is the end of the winding finishing on the outside of the inductor. As the SW node experiences large voltage swings with fast edges, this should be connected to the start of the coil. The quieter Vout end of the inductor windings on the outside then shield the noisier inner windings. Figure 9 shows the output ripple for layout 1 with the inductor in both orientations. The brown trace is with the inner coil connected to SW and the blue is with the outer coil connected to SW. The difference is clear, although whether one is better than the other is not so obvious!
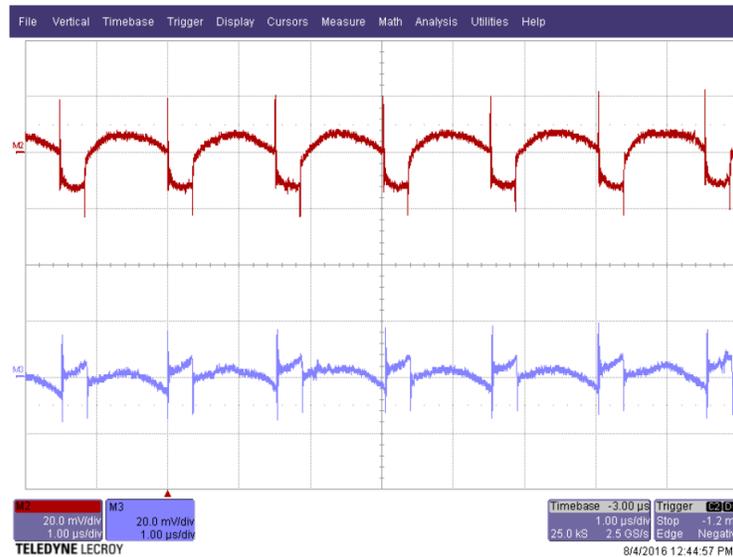
Figure 9. Output Ripple for Layout 1 With Inductor in Both Orientations

3.2 *Results – Input Ripple*

The input ripple was measured directly across the input capacitors of each circuit using the same coax method. There is almost no difference in input ripple between the three layouts, with 90–100 mVpp for all three layout versions.
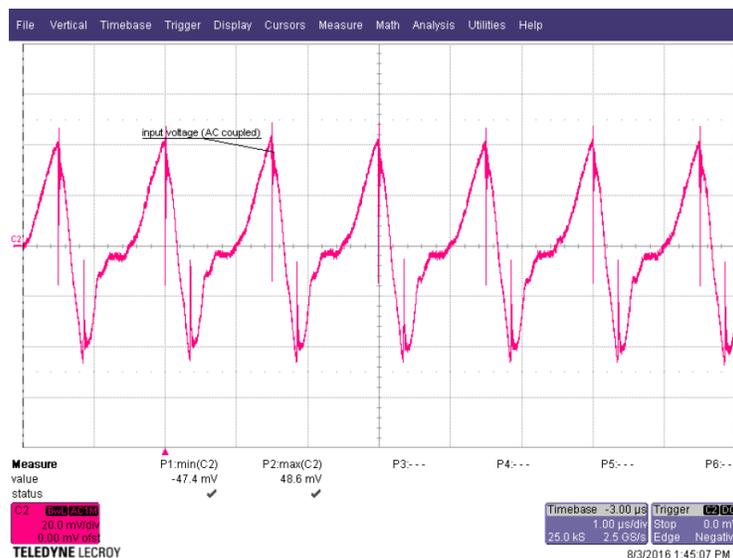
Figure 10. Input Ripple – 12 V to 2.5 V at 2.5 A, Layout 1
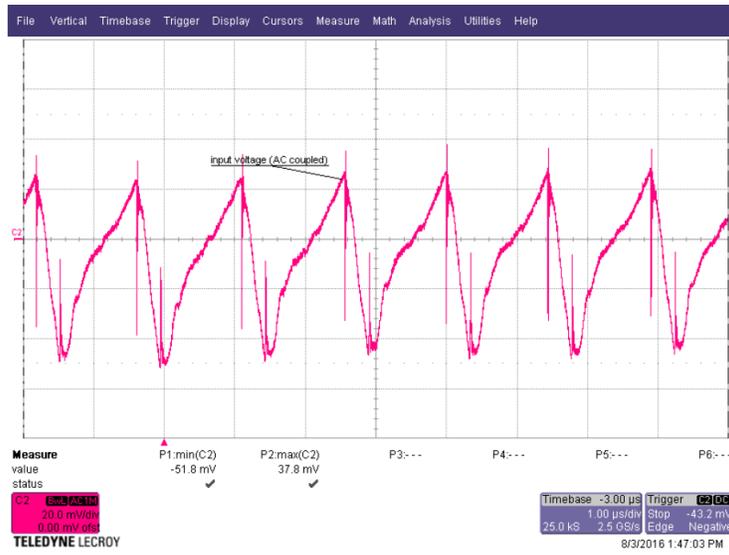
Figure 11. Input Ripple – 12 V to 2.5 V at 2.5 A, Layout 2

Figure 12. Input Ripple – 12 V to 2.5 V at 2.5 A, Layout 3

3.3   *Results – Switch Node*

The switch node ringing shows little change between layouts.

Figure 13. Switch Node Waveform – Layout 1
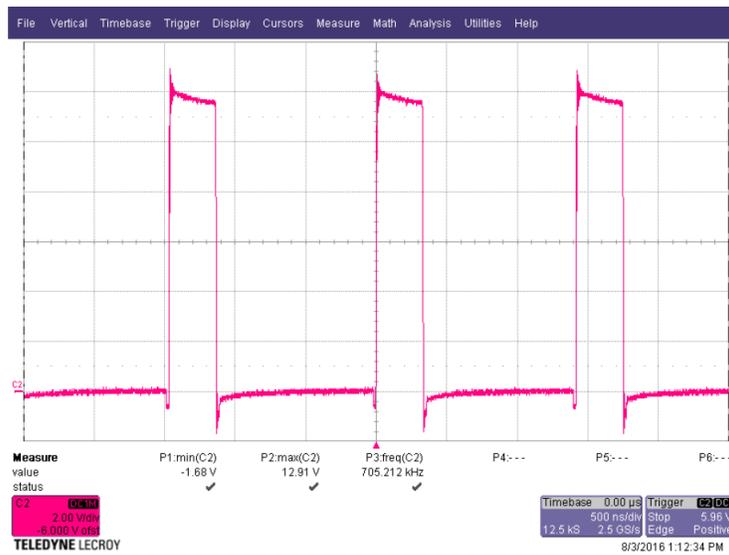
Figure 14. Switch Node Waveform – Layout 2

**Figure 15. Switch Node Waveform – Layout 3**

3.4   Results – Thermal Performance

Thermal images of each circuit were recorded with the converter running at 2.5-A continuous output. Layout 1 was measured from above. For the other two layouts, the PCB was inverted to simulate a typical PCB topology where the inductor (being the highest component) would be on the top of the PCB with IC on the bottom. The thermal image of the inductor side was recorded from above; with the IC side recorded from below, looking up.


**Figure 16. Layout 1 - IC and Inductor Topside**
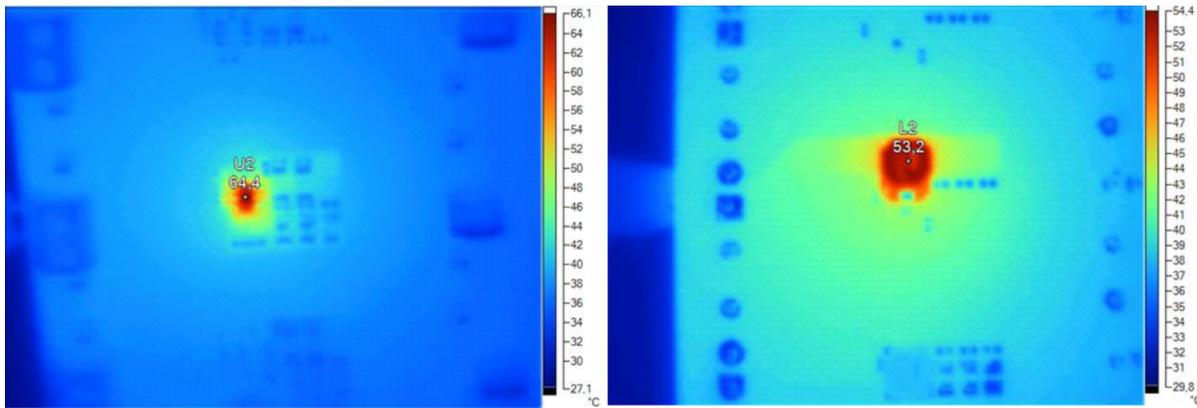
**Figure 17. Layout 2 - IC Bottom Side (Left) Inductor Topside (Right)**
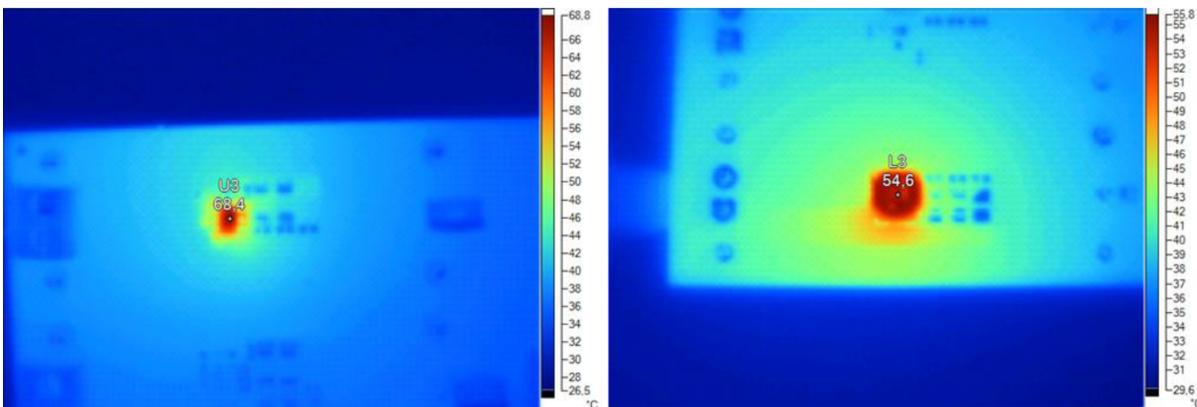
Figure 18. Layout 3 - IC Bottom Side (Left) Inductor Topside (Right)

The two-sided layouts appear to run cooler than the single-sided layout. This is most likely to be due to the co-heating of the inductor and IC when placed side by side.

4 Conclusions

Table 1 shows a summary of results for this investigation. Using both sides of the PCB for components, with the inductor or inductor and output capacitors on the opposite side to the IC, significantly reduces the PCB area used. The electrical effects of this smaller layout seem to be minimal. In fact, the double-sided layout may perform better. Output ripple and temperature appear to be lower for a double sided layout.

Table 1. Summary of Results

	Area (mm^2)	Output Ripple pk-pk (mV)	Input Ripple pk-pk (mV)	Switch Node Overshoot/ Undershoot (V/V)	IC Temp./ Inductor Temp. (°C/°C)
Layout 1: Single sided	173	45	96	0.98/–2.06	73.8/57.1
Layout 2: Inductor on bottom	141	32	90	0.91/–1.68	64.4/53.2
Layout 3: Inductor + output capacitors on bottom	105	24	100	0.66/–1.87	68.4/54.6

Where space is at a premium, using both sides of the PCB to achieve a smallest-possible layout can be done without compromising electrical performance.

5   References

1. DC/DC converter PCB layout, Part 1,2&3. Timothy Hegarty -June 15, 2015.

2. *Five steps to a great PCB layout for a step-down converter* Chris Glaser, TI Analog Applications Journal, 1Q2015. (SLYT614).

3. *How You Measure Ripple Can Make You or Break You.* George Lakkas, TI Powerhouse Blog, July 2016.

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