

External Soft-Start Circuit for TPS7H3301-SP Power-Up Sequencing Applications

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ABSTRACT

The TPS7H3301-SP is a radiation-hardened, Double Data Rate (DDR) memory, 3-A termination regulator with a built-in VTTREF buffer. The TPS7H3301-SP has an enable pin (EN) that, in DDR1 and DDR2 applications, might be connected to the reference input voltage of the device (VDDQSNS). However, in certain applications, the enable pin might be driven independently. If that is the case and the DDR memory is in a S0 or S3 state (VDDQSNS present), there is a possibility of a large inrush current (up to 8 A maximum for sourcing current limit) when the enable pin goes high. This current demand will be seen by the upstream source for VLDOIN and could potentially create problems. This application note is intended to provide an external soft-start circuit to avoid inrush current in these situations.

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1 Power-Up Scenarios

As indicated in the functional block diagram of the TPS7H3301-SP, the enable pin controls only the output buffer since VTTREF is required to be ON and within specifications while in S0 or S3 states. Assuming all other input voltages are present (VDDQSNS, VDD, and VLDOIN), there are 2 possible scenarios for the enable pin:

1. EN pin connected to VDDQSNS
2. EN pin driven independently

1.1 EN Pin Connected to VDDQSNS

In this case, when the device is powered up, there will be a small time constant of 345 μ s at the VDDQSNS pin due to an RC filter at the input of the VTTREF buffer as shown in Figure 1. This time constant will translate to the output of the device and there will not be a large inrush current. This can be verified using the TPS7H3301EVM-CVAL under the following conditions :

- VDDQSNS = VLDOIN = EN = 1.8 V
- VTT/VO = 0.9 V
- VDD/VIN = 2.5 V
- COUT = 3 x 150 μ F and 3 x 4.7- μ F capacitors
- Resistive load of 1 Ω

As Figure 2 shows, the VTT/VO rise time is driven by the RC filter at the input of the VTTREF buffer. Also, the output current stays within the normal operating load current condition of the device.

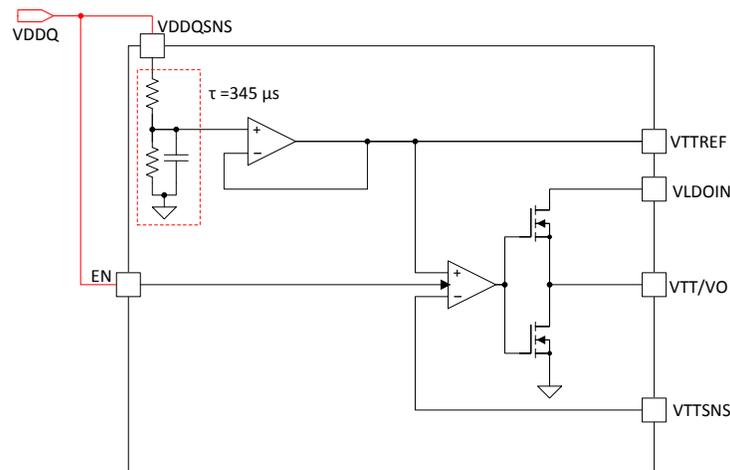


Figure 1. EN Pin Connected to VDDQNS

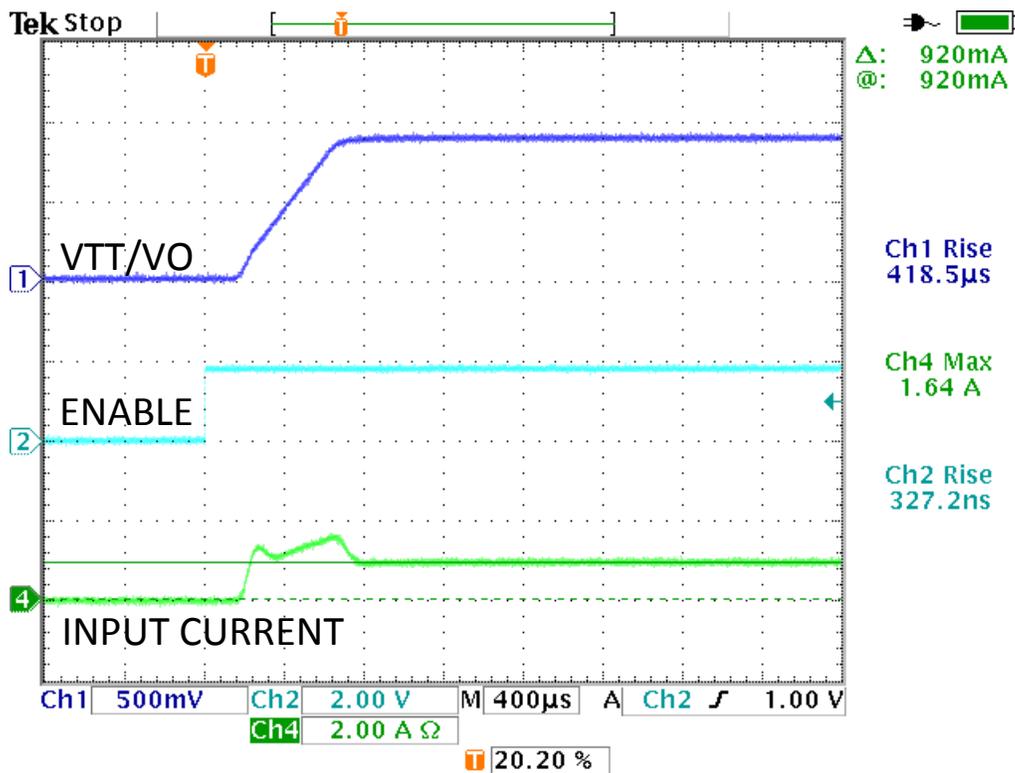


Figure 2. Input Current When EN Pin is Connected to VDDQNS

1.2 EN Pin Driven Independently

If the enable pin is controlled independently and all other input voltages are present, the time constant is not applicable anymore as shown in Figure 3. In this case, inrush current might arise due to the charging of the output capacitors for VTT/VO. The TPS7H3301-SP does not have internal soft-start circuitry, due to the need for quick power up of the DDR memory. Using the TPS7H3301EVM-CVAL under the same previous conditions but driving the EN pin independently with a signal generator, results in an inrush current of almost 6 A, as shown in Figure 4. Also, the VTT/VO rise time of 64 µs can be observed, corroborating that the time constant at the input of the VTTREF buffer is not present in the VTT/VO output. If in a specific application, a controlled soft start is needed to limit inrush current, external circuitry could be implemented as discussed in Section 2.

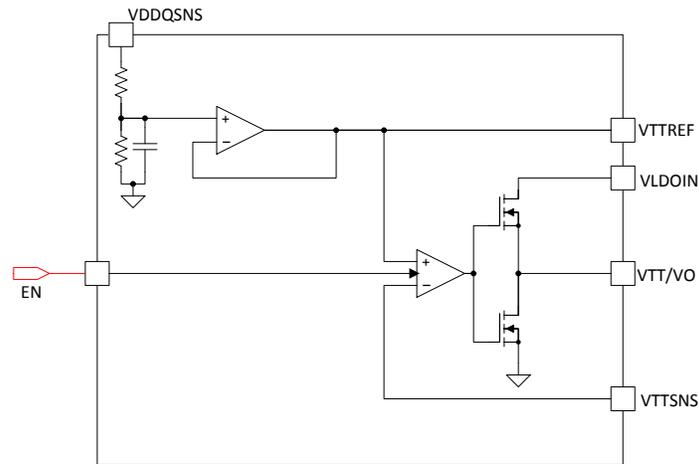


Figure 3. EN Pin Driven Independently With VDDQNS, VDD, and VLDOIN Present

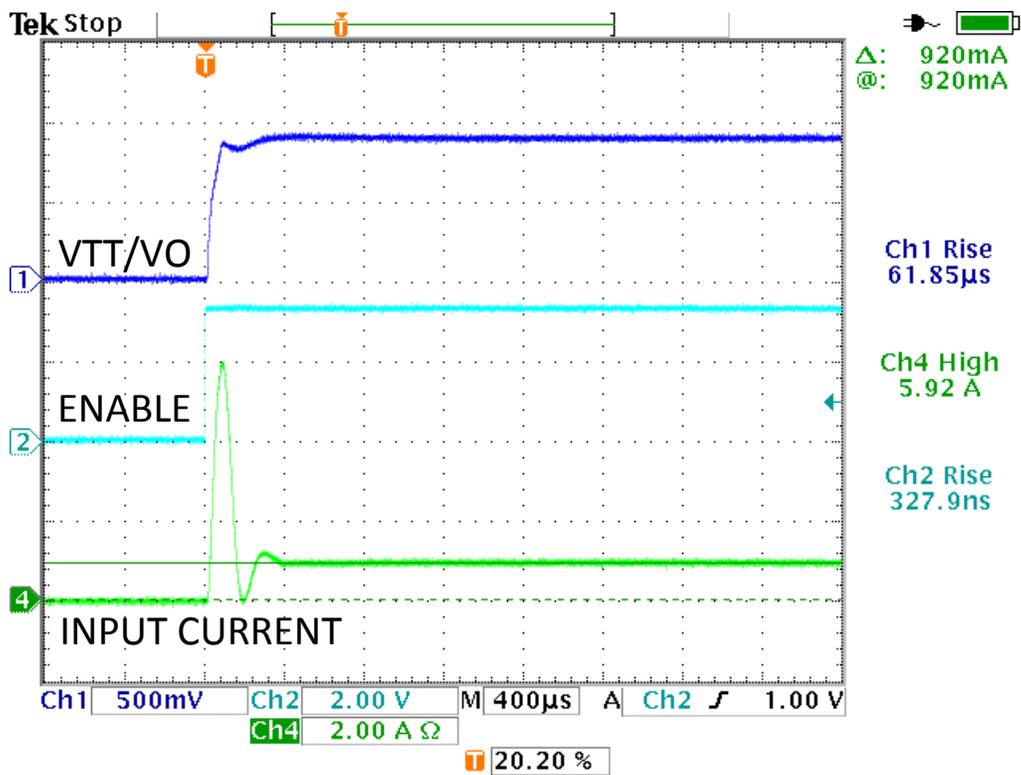


Figure 4. Inrush Current When EN Pin is Driven Independently

2 External Soft-Start Solution

Adding external circuitry like the one shown in Figure 5 results in a controlled rise of the output voltage and also avoids inrush current. The main goal of this external circuit is to take the VTT buffer out of regulation when EN is low and then slowly bring it back to regulation when EN goes high. This is achieved in the following sequence:

1. As EN is low, the output of the regulator is pulled low through an internal 18- Ω MOSFET as indicated in the TPS7H3301-SP data sheet (SLVSCJ5).
2. EN being low makes M1 to be off, turns Q1 on, and VTTSNS is pulled high. This effectively takes the output buffer out of regulation. The R2 resistor serves the purpose of isolating VTTSNS (high) and VTT/VO (low) as well reducing the emitter current of the BJT.
3. As EN goes high, M1 turns on. As a result, the base voltage of Q1 starts decreasing and VTTSNS starts to decrease as well, bringing the output buffer into regulation in a controlled manner. This results in a soft start at the output voltage with no inrush current. Different rise times at VO/VTT can be achieved by changing the biasing point of the base of Q1. This is implemented by changing the R3 resistor.

The requirements for M1 and Q1 are very relaxed due to the small current and breakdown voltages they will experience. In both cases, the drain and base currents will be in the mA range and the breakdown voltages just need to be higher than the VDD/VIN voltage. In the case of the NMOS, the signal driving the gate will be the enable signal, which based on the datasheet specification has an absolute maximum value of 3.6 V and a minimum V_{ENIH} of 1.7 V.

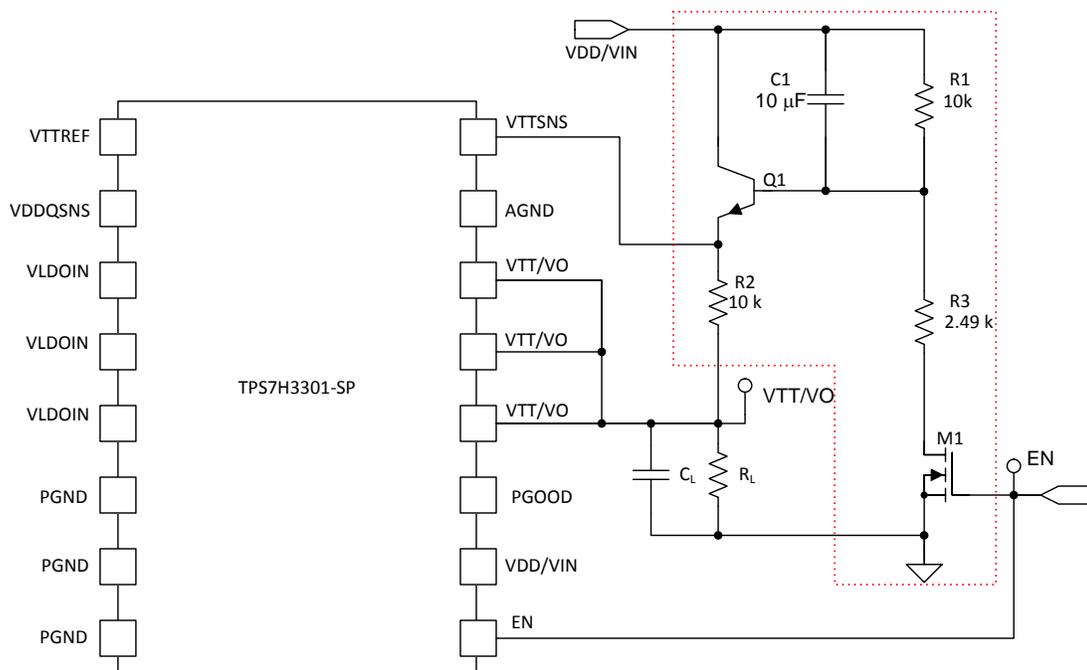


Figure 5. Soft-Start External Circuit for TPS7H3301-SP

3 Results

The circuit in [Figure 5](#) was externally implemented and tested under the same previous conditions using the TI TPS7H3301EVM-CVAL:

- VDDQSNS = VLDOIN = 1.8 V
- VTT/VO = 0.9 V
- VDD/VIN = 2.5 V
- COUT = 3 x 150 μ F and 3 x 4.7- μ F capacitors
- 2N2222 for Q1 and BSS138 for M1
- Resistive load of 1 Ω
- EN toggled using a signal generator

The exact circuit in [Figure 5](#) resulted in an output rise time of about 1.1 ms. [Figure 6](#) shows the toggling sequence applied to the EN pin. The load current and output voltage can be observed as well. [Figure 7](#) shows a zoomed-in section indicating the rise time of the output voltage and the lack of inrush current. The R3 resistor was then replaced by a 5.11-k Ω resistor resulting in a rise time of about 3 ms. These results can also be validated using the PSpice model for the TPS7H3301-SP available in the product folder at <http://www.ti.com/product/TPS7H3301-SP>.

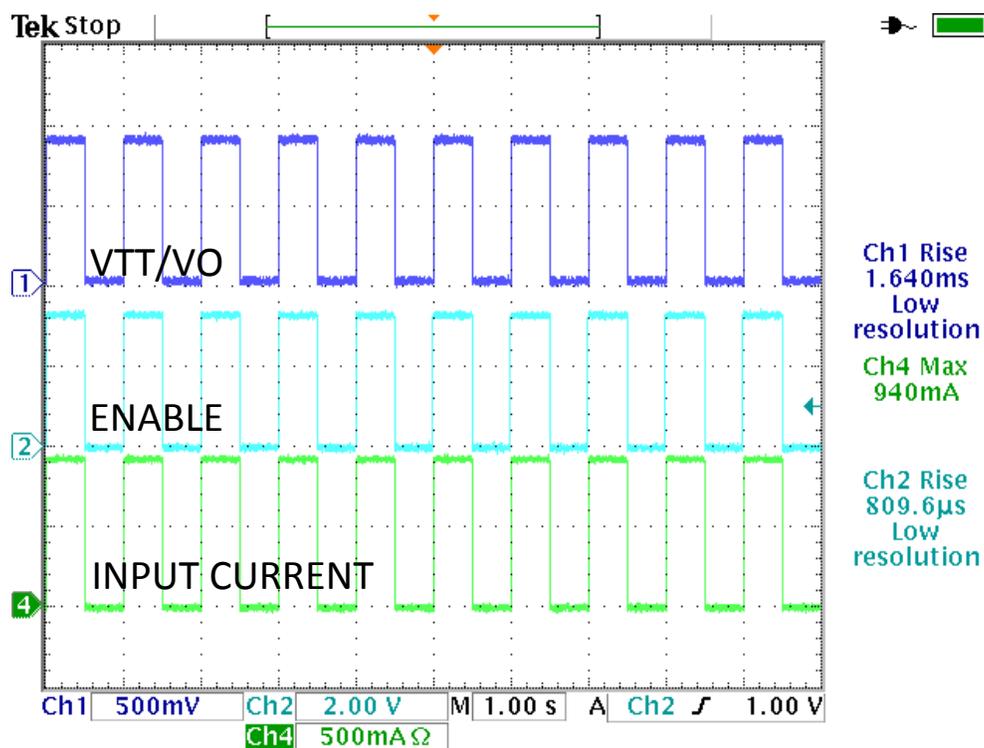


Figure 6. Power Cycling Sequence of the TPS7H3301-SP Using the EN Pin

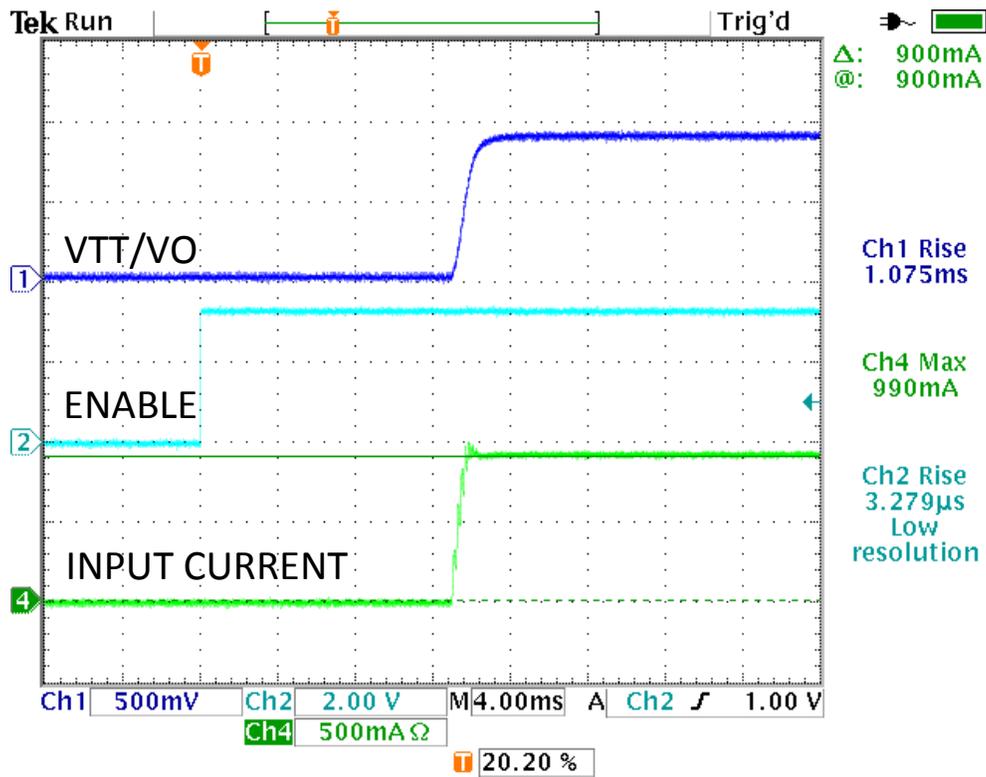


Figure 7. VTT/VO Rise Time of About 1.1 ms Without Inrush Current

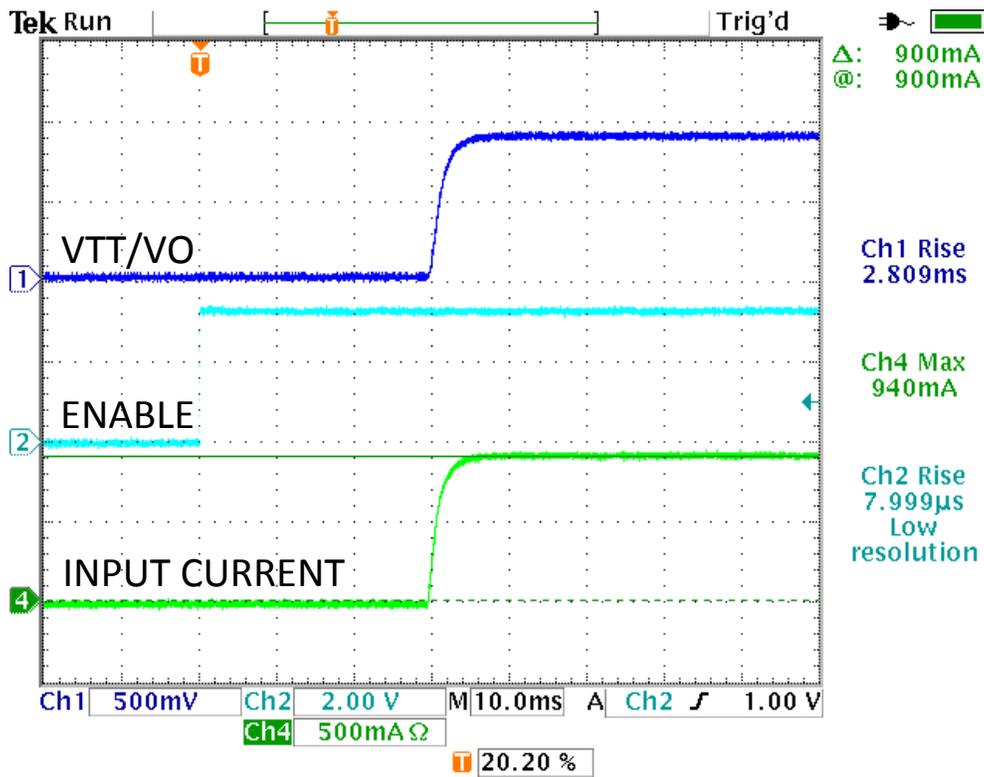


Figure 8. VTT/VO Rise Time of About 3 ms Without Inrush Current

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