Application Report
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Fundamentals of On-Resistance in Load Switches

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ABSTRACT

Two key concerns for any electrical system are power dissipation and proper voltage regulation. However, inherent and parasitic resistances create challenges for both. This application report discusses the fundamentals of load switch On-resistance and how to select a load switch with the right On-resistance depending on the system requirements.

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1 Load Switches Overview

A load switch is used to connect and disconnect power from a series load. This enables better power saving, power sequencing, and safer operation; however, the series load switch inherently adds some On-resistance to the power path. Figure 1 shows the schematic of a basic load switch. Additional information about the operation of load switches can be found in the Basics of Load Switches application report.

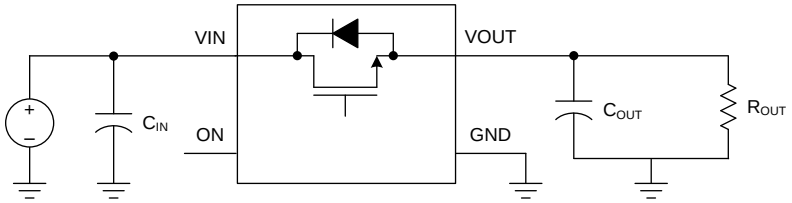

Figure 1. Typical Load Switch Application

In an ideal world, the load switch must have no impedance when the device is on. In reality, there are numerous components in a load switch that inherently have some electrical resistance which prevent the device from performing with no impedance. The combined effect of all the resistive components is referred to as On-resistance (R_{ON}) and is one of the most important parameters when selecting a load switch.

Adding too much resistance to a power path can lead to high power loss and large voltage drops. Too much power dissipation in a load switch can lead to reduced battery life and cause overheating issues. If the voltage drop across the load switch is too large, the load switch may not stay within the specified tolerance, causing faulty or unreliable operation. Using a load switch with low On-resistance counters these effects; however, selecting a device with an On-resistance that is too low causes an unnecessary increase in cost and size.

On-resistance is defined as the total measured resistance from the VIN to VOUT pins of the load switch. As load current (I_{LOAD}) passes through the device, this resistance causes a voltage drop in the power path. The relationship between R_{ON} and the voltage drop ($V_{IN} – V_{OUT}$) is shown in Equation 1:

$$V_{IN} - V_{OUT} = R_{ON} \times I_{LOAD} \quad (1)$$

On-resistance also affects the power loss (P_D) in the load switch as shown in Equation 2:

$$P_D = I_{LOAD}^2 \times R_{ON} \quad (2)$$

As power is dissipated through the load switch, the device junction temperature increases and can affect the performance and lifetime of the device. Equation 3 describes the total power ($P_{D,MAX}$) that can be dissipated in a load switch based upon the maximum operating Junction Temperature ($T_{J,MAX}$), the Ambient Air Temperature (T_A), and the Thermal Resistance from the junction to the ambient air (θ_{JA}).

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\Theta_{JA}} \quad (3)$$

2 Components of On-Resistance in Load Switches

R_{ON} can be summarized into the resistances of the silicon process and the packaging resistances as shown in Equation 4:

$$R_{ON} = R_{silicon} + R_{wire} + R_{lead} \quad (4)$$

Where:

- $R_{silicon}$ = Inherent resistance from silicon process
- R_{wire} = Bond wire resistance
- R_{lead} = Resistance of the lead frame

2.1 Resistance from the Silicon Process ($R_{silicon}$)

The integrated circuit can be generalized as silicon, metal, and dielectric stacked layer on layer to create signal paths for electrical signals to connect the components of the device.

The metal traces connecting the VIN terminal, to the FET, then the VOUT terminal introduces resistance to the device. The design of the device plays a key role in minimizing the On-resistance added by the metal layers. The longer the traces on the metal layer are; the more resistance is added to the device.

The resistance from the FET component is often separated from the total $R_{silicon}$ into a parameter called $R_{DS,ON}$. Typically, this is the largest source of resistance in a load switch and is discussed in greater detail in Section 3.

2.2 Bond Wire Resistance (R_{wire})

The silicon die is electrically connected to the lead frame of the package, typically using either copper or gold bond wires. The bond wires are ball-bonded to the lead frame and die using a combination of heat and pressure to create a solid connection. Figure 2 is an cutout of a QFN package and a visualization showing how each component of the packaging adds additional resistance across the load switch.

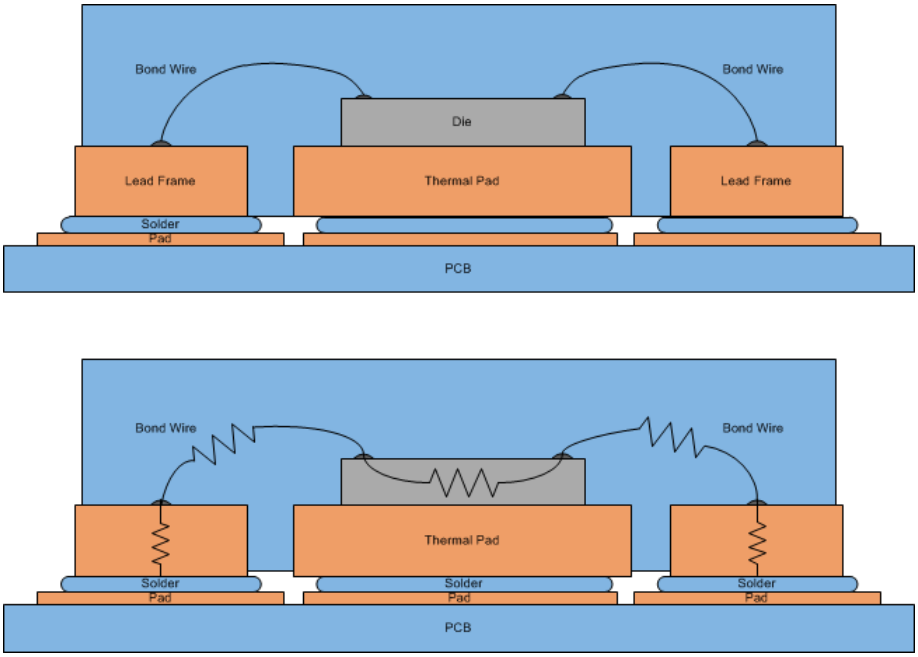

Figure 2. Illustration of a QFN Package

The resistance introduced by the bond wires can be summarized as shown in Equation 5:

$$R = \frac{\rho L}{A} \tag{5}$$

Where:

- R = Resistance of the wire
- ρ = Resistivity of material
- L = Length of the wire
- A = Cross sectional area of the wire

As modern load switches are getting smaller, bond wires also become shorter and thinner. Although having shorter bond wires leads to a lower resistance of the wire, the decreasing cross sectional area of the wire counteracts this. TI emerging package technologies such as the HotRod QFN package seek to completely eliminate wire bonds by attaching the silicon die directly to the lead frame, for a lower total On-resistance.

2.3 Lead Frame Resistance (R_{lead})

Referring back to Figure 2, the bond wires are connected from the die to the lead frame. The lead frame is made of the metal pins that are molded into packaging and is used to physically and electrically connect the device to the PCB. The lead frame is made of metal, and as such introduces some resistance into the device.

Although the bond wire and lead frame resistances are relatively small compared to the silicon resistance, the combined effect can become significant in low voltage applications and affect the system level performance.

3 Factors that Affect On-Resistance

3.1 Effects of Load Current on On-Resistance

A common question asked is whether there is any relationship between On-resistance and the load current through the load switch. While many parameters affect On-resistance, such as temperature, size of the MOSFET, and supply voltage; current does not directly impact On-resistance.

As stated before, the majority of On-resistance originates from the $R_{DS,ON}$ of the MOSFET. To understand the load current vs On-resistance relationship, $R_{DS,ON}$ must be further examined. The resistance of an N-channel FET can be calculated as shown in Equation 6:

$$R_{DS} = V_{DS} / I_{DS} \tag{6}$$

The linear model simulates the drain current (I_{DS}) of a N-channel FET in the linear region when the drain-source voltage (V_{DS}) is much smaller than the gate-source voltage minus the threshold voltage ($V_{GS} – V_T$). This model is shown in Equation 7:

$$I_{DS} = \mu_n \times C_{ox} \times \frac{W}{L}[(V_{GS} - V_T)V_{DS}] \text{ for } V_{DS} << (V_{GS} - V_T) \tag{7}$$

Where:

- μ_n = Electron Mobility
- C_{OX} = Oxide Capacitance
- W = Width of Gate
- L = Length of Gate
- V_{GS} = Gate-source voltage
- V_T = Threshold voltage of MOSFET
- V_{DS} = Drain-source voltage

Plugging Equation 7 into Equation 6, the equation results in Equation 8:

$$R_{DS} = \frac{V_{DS}}{\mu_n \times C_{OX} \times \frac{W}{L}[(V_{GS} - V_T)V_{DS}]} \rightarrow \frac{1}{\mu_n \times C_{OX} \times \frac{W}{L}(V_{GS} - V_T)} \tag{8}$$

When the gate voltage is less than the threshold voltage, there is no drain current. Once the gate voltage is greater than the threshold voltage, the current increases linearly gate voltage. It is because of this behavior that a MOSFET in the linear region can be described as a voltage controlled resistor. So while $R_{DS,ON}$ is influenced by many parameters, current does not directly affect $R_{DS,ON}$. Load current can indirectly effect $R_{DS,ON}$ in cases of high power dissipation. The high power dissipated raises the junction temperature of the device, affecting its performance.

3.2 Effect of Temperature on On-Resistance

As stated before, a load switch has some inherent resistance, which causes power to be dissipated when there is a load current.

The power is dissipated as heat energy from the silicon die to the packaging, printed circuit board, and the air. The heat energy raises the temperature of the silicon die (junction temperature) changing the performance of the device. The power dissipated due to R_{ON} can be calculated using Equation 2, restated below:

$$P_D = I_{LOAD}^2 \times R_{ON} \tag{9}$$

For more information on the thermal considerations when designing a system, see the application report, Load Switch Thermal Considerations.

Looking back at Equation 8, On-resistance is affected by the electron mobility (μ_n). As the electron mobility increases, the $R_{DS,ON}$ decreases. The model known as Matthiessen's Rule expresses electron mobility in terms of thermal lattice scattering and ionized impurity scattering. See Equation 10:

$$\frac{1}{\mu_n} \propto \frac{1}{\mu_{ph}} + \frac{1}{\mu_{ion}} \tag{10}$$

Where:

- μ_n = Electron mobility
- μ_{ph} = Mobility due to thermal lattice scattering
- μ_{ion} = Mobility due to ionized impurity scattering

At temperatures above 200K (about –73°C), mobility from thermal lattice scattering dominates that of ionized impurity scattering. Becuase most semiconductor processes are rated for operation in –40°C minimum environments, thermal lattice scattering is the main contributor to electron mobility in load switches.

3.3 Effect of Temperature on Thermal Lattice Scattering

In an extrinsic semiconductor, the semiconductor is doped to add either more negatively or positively charged particles to the lattice to increase the electron or hole concentrations, respectively. If a semiconductor was doped with an element with more valence electrons than silicon, for example phosphorus, there is a free electron that moves around the silicon lattice and carry current. This is called doping with donors. Doping silicon with a donor is what creates an n-type region. If the semiconductor was doped with an element with fewer valence electrons, that would introduce a hole into the lattice. This is introducing an acceptor into the lattice and is the basis of the p-type region of the semiconductor.

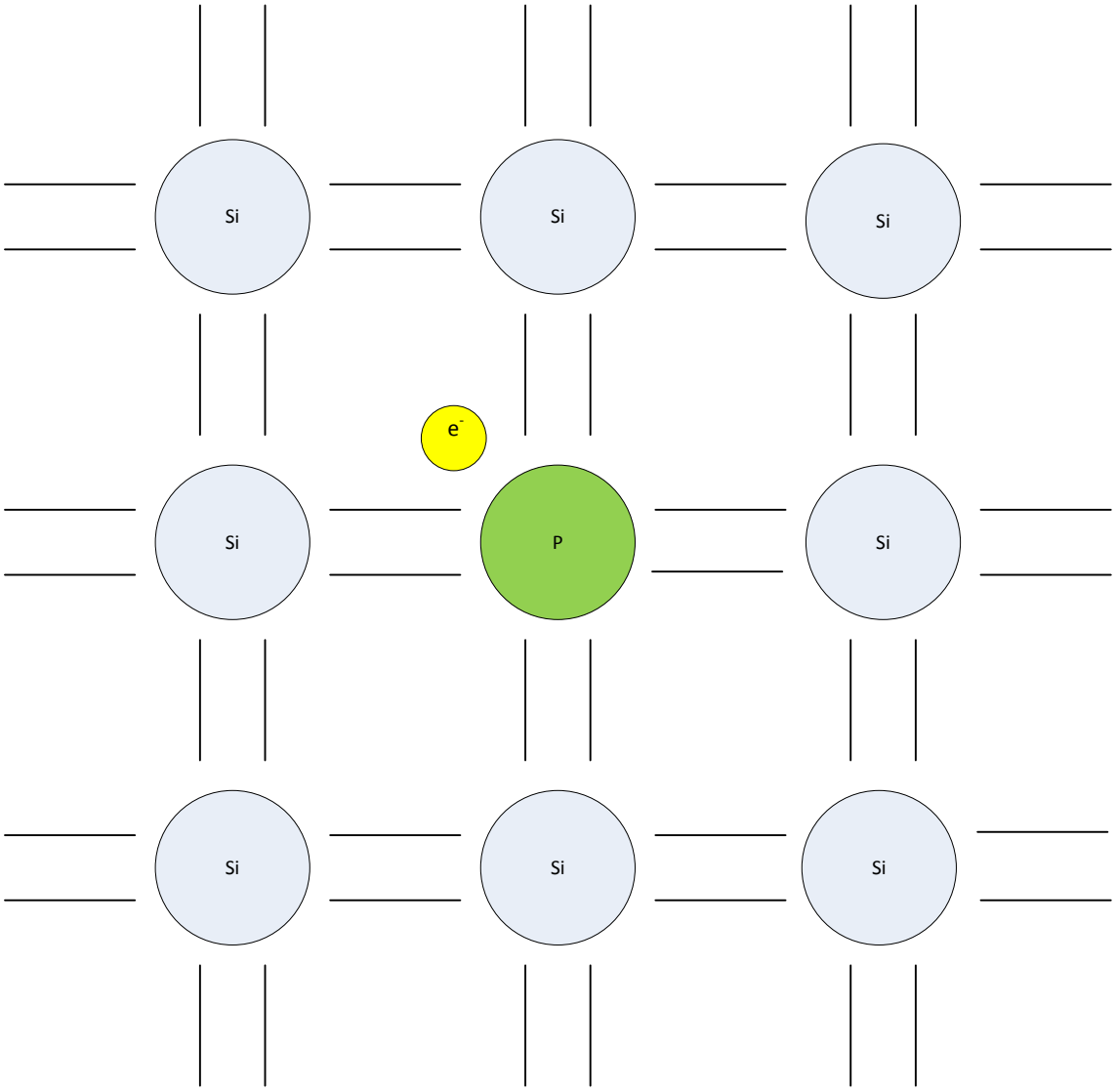

Figure 3. Lattice of Silicon Doped with Phosphorus

As the junction temperature increases, thermal vibrations (phonons) of the lattice of the silicon increase (Imagine the Silicon and Phosphorus particles in Figure 3 rapidly moving back and forth). This increases the possibility that the electrons trying to pass through the lattice collides with the silicon lattice and scatter, lowering the mean time between scattering (τ). As the mean time between scattering decreases, the mobility also decreases as shown in Equation 11:

$$\mu = \frac{q}{m} \times \tau \tag{11}$$

Where:

- μ = Mobility of the electrons
- q = Charge of an electron
- m = Effective mass of an electron
- τ = Mean time between scatterings

As a whole, it can be seen that an increase in temperature decreases the mean time between scattering, leading to a lower mobility, and a higher On-resistance.

3.4 Effects of Supply Voltage on On-Resistance

In some load switches, the device is powered using the main input voltage. This can be seen in the TPS22918 device. In this situation, R_{ON} does not stay constant across the whole VIN range. If the system requires the On-resistance to stay constant across all supply voltages, this can be accomplished through a second higher voltage power supply (VBIAS).

MOSFETs do not instantly switch from OFF to ON. There is a threshold voltage that must be reached by the gate voltage before the resistance of the MOSFET is lowered enough for significant current to pass through. When $V_{GS} > V_T$ and $V_{DS} < V_{GS} – V_T$, this is called the linear region. When $V_{DS} > V_{GS} – V_T$, the device reaches saturation. To keep the device in the linear region, the gate voltage is kept at a high enough voltage so that V_{DS} is always much less than $V_{GS} – V_T$. The secondary bias supply provides all the necessary power to run the internal functions of the device. See Figure 4 and Figure 5.

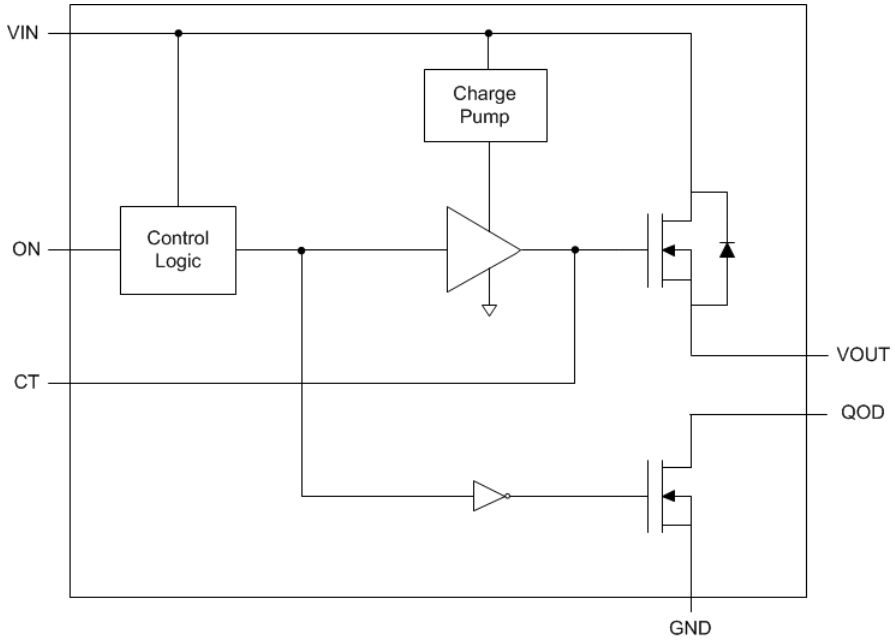

Figure 4. Block Diagram of Load Switch without VBIAS Pin

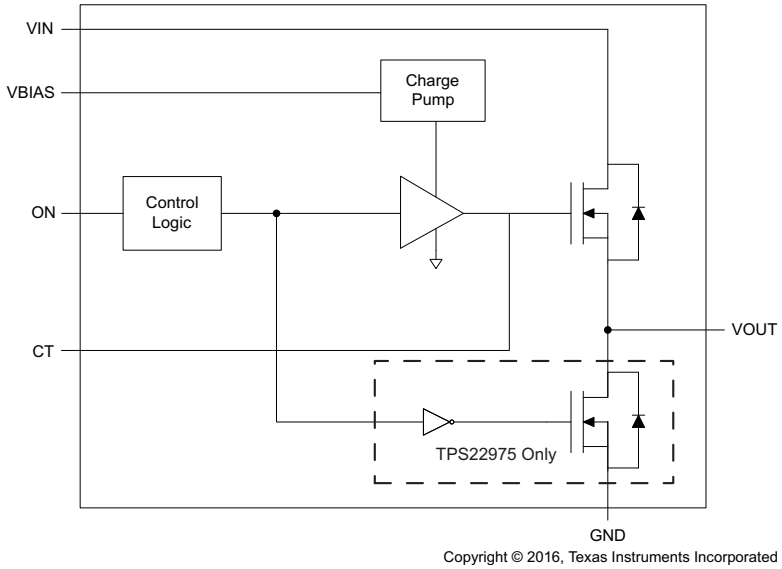

Figure 5. Block Diagram of Load Switch with VBIAS Pin

The VBIAS pin powers the charge pump which provides a constant and high V_{GS} so that the device is always in the linear region.

4 On-Resistance Applications Examples

There are certain key tradeoffs when choosing a load switch. The system requirements must be carefully defined in terms of voltage drop and power dissipation to balance the system cost and performance. While having a low R_{ON} is always beneficial, there are cases where having a low R_{ON} is more critical. For example, low voltage applications can tolerate less of a voltage drop so they need a lower On-resistance. If the voltage drop is too high, this could cause a system to reset.

For example, if the system requires a 5 V, 2 A power rail, and can tolerate 2% voltage difference, the maximum On-resistance the load switch can have is shown in Equation 12:

$$R_{ON,max} = \frac{\Delta V_{max}}{I_{LOAD}} = \frac{.1\,V}{2\,A} = 50\,m\Omega \tag{12}$$

Whereas if the system requires a 1 V , 2 A power rail, the maximum On-resistance the load switch can have is shown in Equation 13:

$$R_{ON,max} = \frac{\Delta V_{max}}{I_{Load}} = \frac{.02\,V}{2\,A} = 10\,m\Omega \tag{13}$$

When considering current, having a low On-resistance is more important when there is a large load current. If the system requires a 5 V, 6 A power rail and can tolerate 2% voltage difference, the maximum On-resistance that the load switch can have is shown in Equation 14:

$$R_{ON,max} = \frac{\Delta V_{max}}{I_{LOAD}} = \frac{.1\,V}{6\,A} = 16\,m\Omega \tag{14}$$

Power dissipation also determines what On-resistance the system is allowed. Say in the first 5 V, 2 A example, the maximum allowed power dissipated needs to be limited to 100 mW. The maximum R_{ON} constrained by power dissipation and the load current can be estimated by using Equation 15:

$$P_{D,MAX} = I_{LOAD}{}^2 \times R_{ON} \rightarrow 100\,mW = 4\,A \times R_{ON} \rightarrow R_{ON} = 25\,\Omega \tag{15}$$

In this case, the maximum On-resistance allowed is constrained by power dissipation, so the required On-resistance must be even lower.

5 Conclusion

On-resistance is influenced by various parameters such as temperature and supply voltage. By understanding what causes On-resistance of a load switch, the device can be selected into a system more effectively. Texas Instruments strives to always provide the highest level system optimization by offering a wide selection of load switches with different On-resistances. To view the TI load switch portfolio, visit ti.com/loadswitches.

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