# Interfacing TPS57xxx-Q1,TPS65320-Q1 Family, and TPS65321-Q1 Devices With Low Impendence External Clock Drivers

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## ABSTRACT

This application report describes methods to interface TPS57xxx-Q1, TPS65320-Q1 Family, and TPS65321-Q1 devices to an external system clock. It proposes a new AC-coupled interface circuit avoiding any DC-bias conditions on the RT/CLK pin. This document also discusses important design details and provides optimizations of existing clock-interface circuits.

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# 1    Introduction

The RT/CLK pin of TPS57xxx-Q1, TPS65320-Q1 Family, and TPS65321-Q1 devices can synchronize the regulators to an external system clock. These devices have a built-in phase-locked loop (PLL), which can track the external clock very accurately. The RT/CLK pin can also set the default or initial switching frequency. A resistor connected to GND determines the switching frequency. Different clock-interface circuits are proposed in different datasheets. This document addresses potential issues with these circuits and proposes a new clock-interface circuit, which can be used with different types of CMOS logic driver/buffer interfaces.

# 2    Device Operation

To implement the synchronization feature, apply a square wave to the RT/CLK pin. The square wave amplitude must meet the datasheet electrical specifications (VIL and VIH). The minimum on/off time and frequency specifications should be met. Design the external synchronization circuit in such a way that the device has the default-frequency set resistor connected from the RT/CLK pin to ground if the synchronization signal turns off. Also, the DC high/low signal on the RT/CLK pin during startup and shutdown could cause regulator output voltage instability.

# 3    Existing Interface Circuits and Their Drawbacks

Typically, the external clock is applied after power up of the device. With the method proposed in the TPS57160-Q1 datasheet, SLVSAP1, (see Figure 1) the device works fine only if the clock source has a high-output impedance or GND during startup. The initial switching frequency is determined by the RT/CLK resistance to GND according to the corresponding datasheet formulas. Usually, CMOS logic drivers/buffers are used, which may start up with low or high DC-voltage levels if no clock is applied. A high DC-voltage level will prevent startup.

Also, with this circuit, there is a possibility of degraded clock-amplitude levels at the RT/CLK pin as standard logic cannot drive the 50-Ω termination resistor. This is more suited for driving with RF-clock sources. The 50-Ω termination resistor can be changed to 1-kΩ if needed.

Bus Buffer Gates, with a 3-State Output like buffer gates, such as SN74LVC1G125-Q1, SN74LVC1G125A-Q1, SN74LVC1G126-Q1, and SN74LVC1G126A-Q1 can be used. These devices ensure a high-impedance state during power up or power down when OE is tied to $V_{CC}$ through a pullup resistor.

The method proposed in the TPS57112-Q1 datasheet, SLVSAL8, (see Figure 2) can also be used with the above buffer-gate logic or guaranteed High-Z driver stage during startup, but it is recommended to use the Figure 1 circuit as a 4-kΩ series resistor helps in reducing the phase jitter in heavy load applications when synchronizing to an external clock and when transitioning from EXTERNAL CLOCK mode to RT/CLK mode.
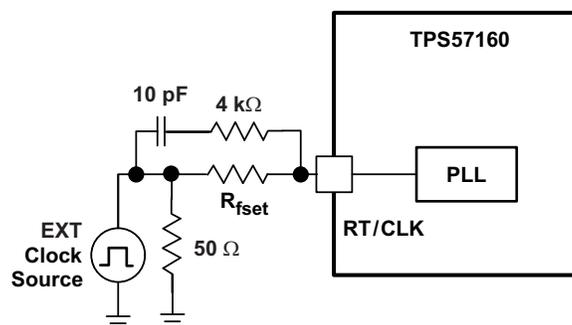


**Figure 1. Synchronizing to an External Clock With a 50-Ω Termination Resistor**
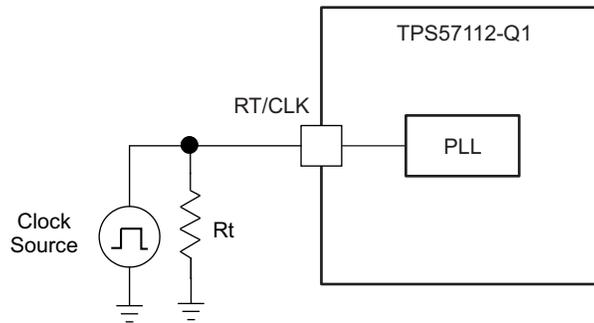
**Figure 2. Synchronizing to an External Clock With a High-Impedance Clock Source**

An AC-coupling to the external-clock driver is necessary to avoid any DC-bias conditions on the RT/CLK pin. The example circuit in Figure 3 is not recommended. Due to the AC-coupling effect, +Vclk/2 and –Vclk/2 are generated on the device side and the negative side (–Vclk/2 ) gets clamped due to the device internal-ESD clamping-diode structure. Therefore, at the device pin, around –0.6 V is seen, which is a violation of the datasheet absolute maximum rating specification of –0.3 V on this pin. This injects as well current/energy through the internal-ESD clamping-diode structure present on the RT/SYNC pin, which might be tolerable if $C_C$ is small enough and Rser is used to limit the current. But the allowed current is not specified in the datasheet, thus there is no assurance of this.
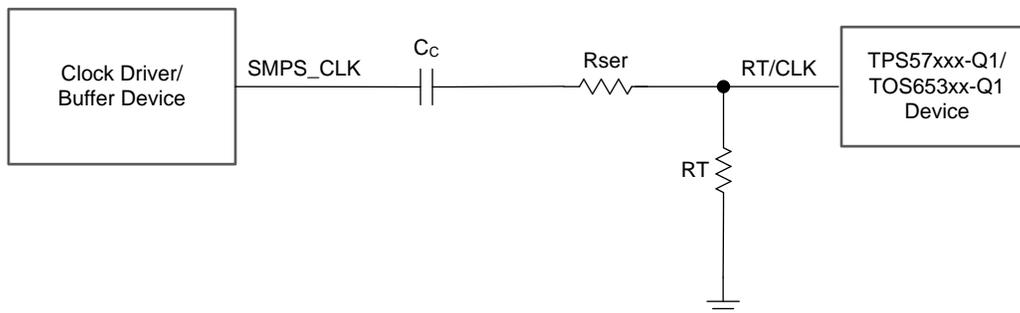


**Figure 3.** *Not Recommended* **- Interfacing an External Clock With an AC-Coupling Capacitor and Series Resistor**

## 4 Proposed Clock Interface Circuit

Figure 3 is modified by splitting the series resistor and adding a Schottky diode as shown in Figure 4, so a negative voltage below -0.3 V at RT/CLK pin can be avoided. A very-low forward voltage (less than 0.3 V) and a fast-switching Schottky diode must be used. Resistor Rser1 (500 Ω) limits current through this diode and Rser2 (1.5 KΩ) ensures that the internal ESD diode will not conduct as it offers a higher resistance compared to the external Schottky diode. Additionally, Rser2 makes a low-pass filter with the RT/CLK-pin parasitic capacitance and during transient conditions the external Schottky diode conducts before the internal ESD diode. The Schottky diode also shifts the RT/CLK voltage level by around 0.2 V, which helps achieve the VIH level quickly.
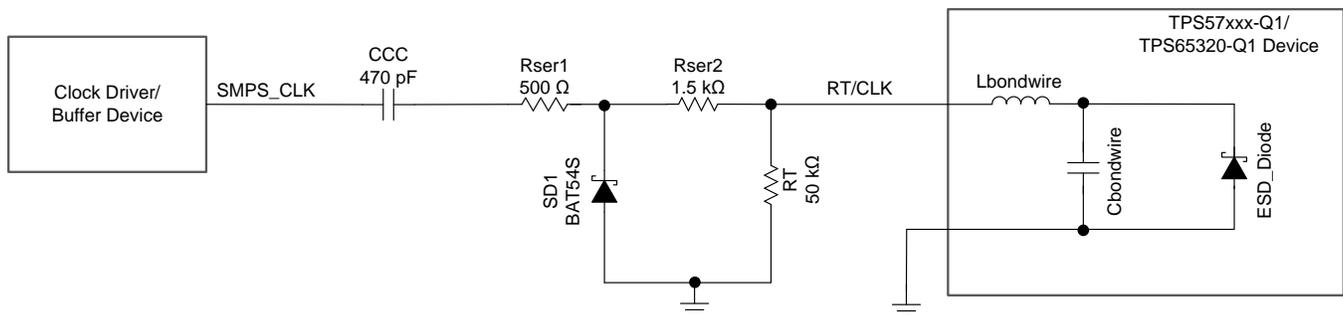


**Figure 4. Interfacing an External Clock With an AC-Coupling Capacitor, Series Resistor, and Schottky Diode**

A very-low forward-voltage Schottky with low-leakage current and fast-transient response must be used. A Schottky diode with large forward-voltage drop may not solve the issue of a negative voltage of −0.3 V at the RT/CLK pin and a Schottky diode with higher-leakage current may impact the startup behavior with INTERNAL CLOCK mode. The BAT54 diode has been verified in the lab and is found to work fine for the test conditions. A BAS40 diode may be slightly better as it has a lower-leakage current compared to the BAT54 device.

# 5    Measurement Results

The TPS57160EVM was used to perform the measurements in the lab to verify the functionality of the circuits in Figure 3 and Figure 4. Though the testing is done only on the TPS57160-Q1 device, these results can be applied to other TPS57xxx-Q1, TPS65320-Q1, and TPS65321-Q1 devices, because the clock interface is similar for these devices. See for the tests and corresponding waveforms.

**Table 1. Measurement Results**

| TEST | COMPONENTS | FIGURE REFERENCES | RESULTS |
|---|---|---|---|
| Case 1: Show the effect of AC coupling without the external Schottky diode (as in Figure 3). | No Schottky diode, CCC = 470 pF, Rser1 = 1.5 kΩ, and RT = 120 kΩ | Figure 5 and Figure 6 | Voltage at RT/CLK pin is around –0.6 V. |
| Case 2: Show results for two different clock frequencies. | Schottky diode, RT = 50 kΩ, CCC = 470 pF, Rser1 = 1 kΩ, and Rser2 = 3 kΩ | Figure 7 and Figure 8 | This circuit has poor amplitude levels at the RT/CLK pin. |
| Case 3: Show the results for three different clock frequencies. | Schottky diode, RT = 50 kΩ, CCC = 1 nF, Rser1 = 1 kΩ, and Rser2 = 3 kΩ | Figure 9 and Figure 10 | This circuit has poor amplitude levels at the RT/CLK pin |
| Case 4: Show the results for three different clock frequencies. | Schottky diode, RT = 50 kΩ, CCC = 470 pF, Rser1 = 500 Ω, and Rser2 = 1.5 kΩ | Figure 11, Figure 12, and Figure 13 | This circuit has good results and is the proposed new circuit. |
| Case 5: Shows the results using a higher value of CCC. | Schottky diode, RT = 50 kΩ, CCC = 1 nF, Rser1 = 500 Ω, and Rser2 = 1.5 kΩ | Figure 14 | Shows the results with and this shows a slightly higher-clamp voltage due to a higher value of CCC. |

## 5.1    Case 1 Test Results
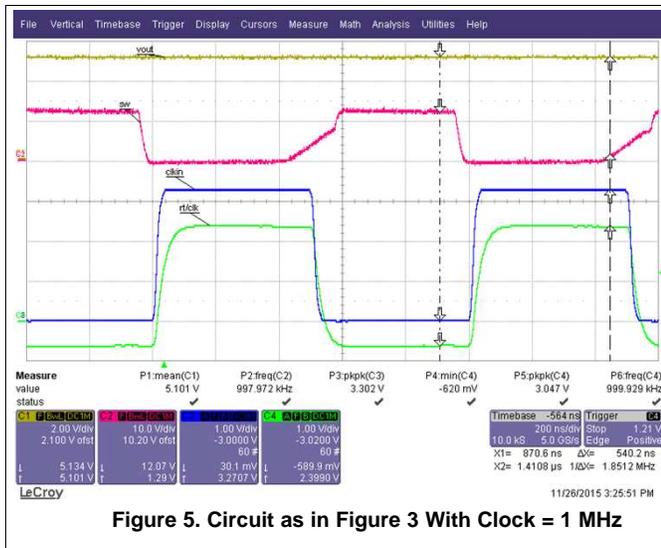


Figure 5. Circuit as in Figure 3 With Clock = 1 MHz
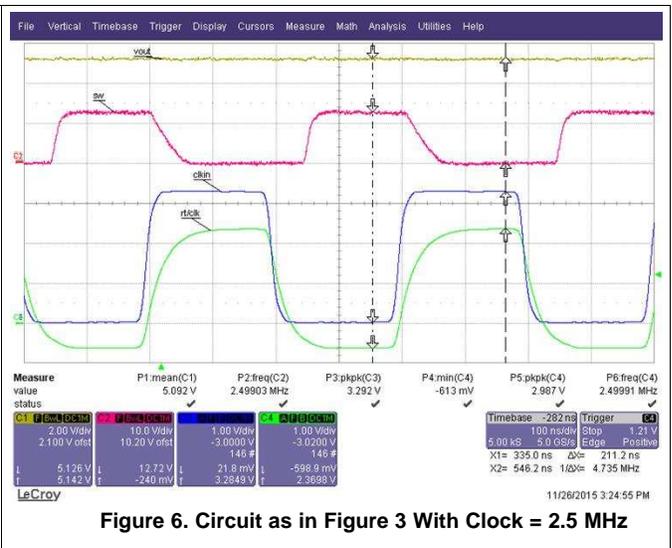
Figure 6. Circuit as in Figure 3 With Clock = 2.5 MHz
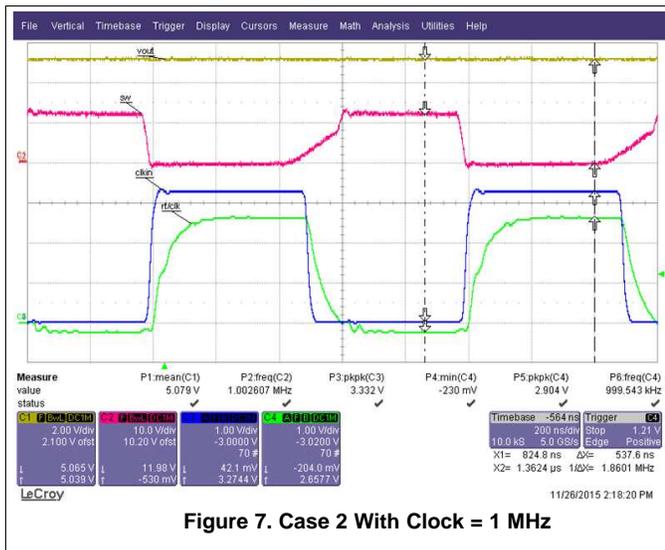
## 5.2 Case 2 Results
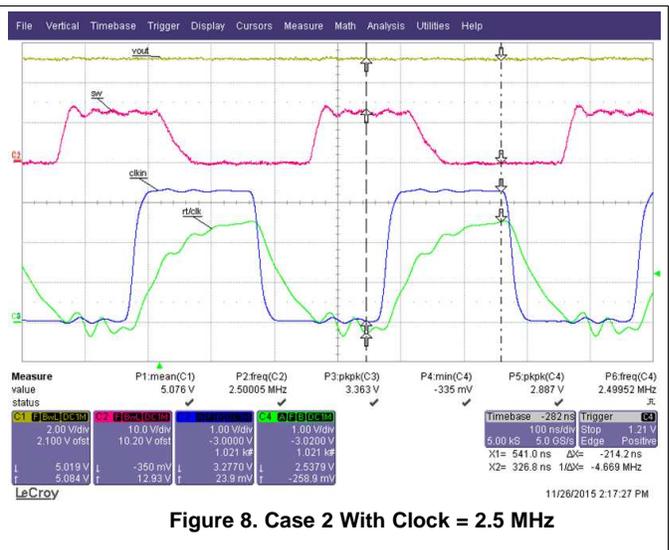


Figure 7. Case 2 With Clock = 1 MHz



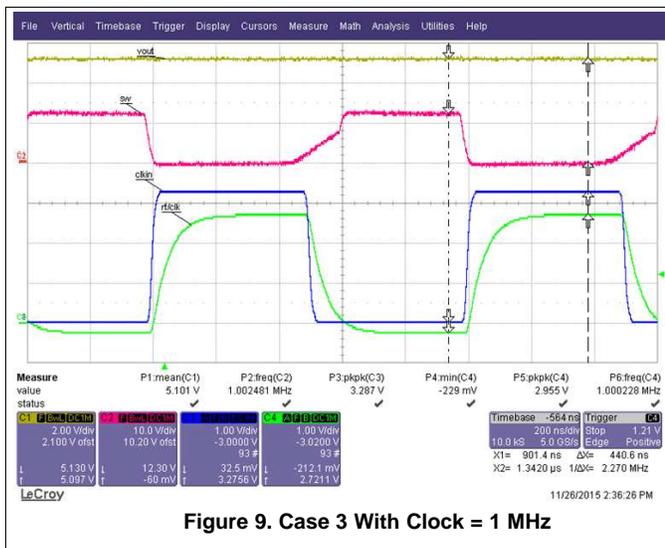Figure 8. Case 2 With Clock = 2.5 MHz

## 5.3 Case 3 Results



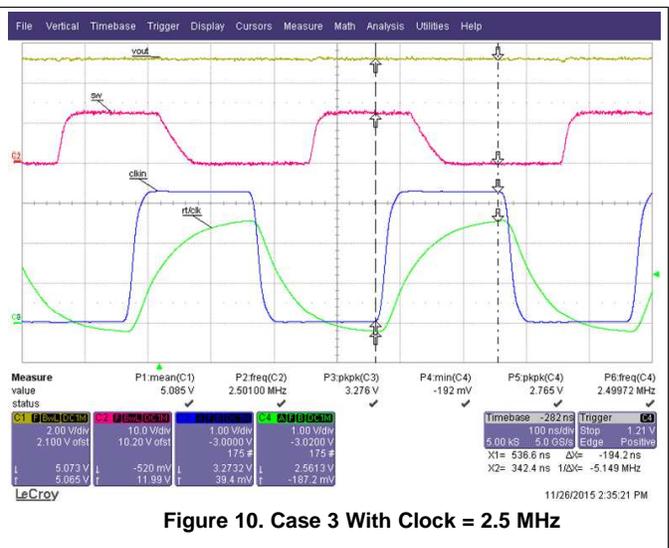Figure 9. Case 3 With Clock = 1 MHz



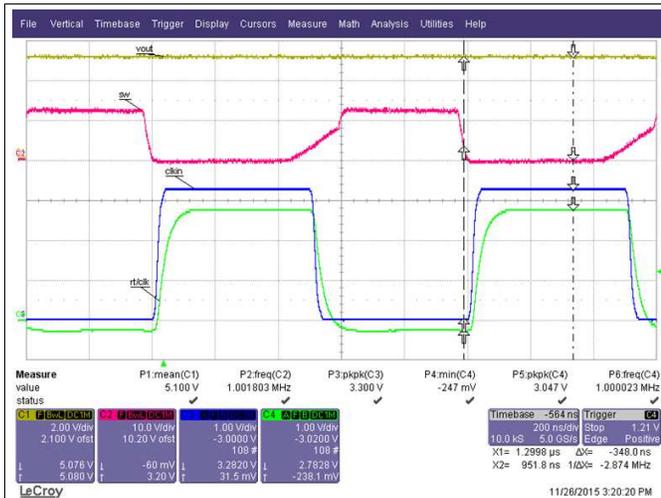Figure 10. Case 3 With Clock = 2.5 MHz

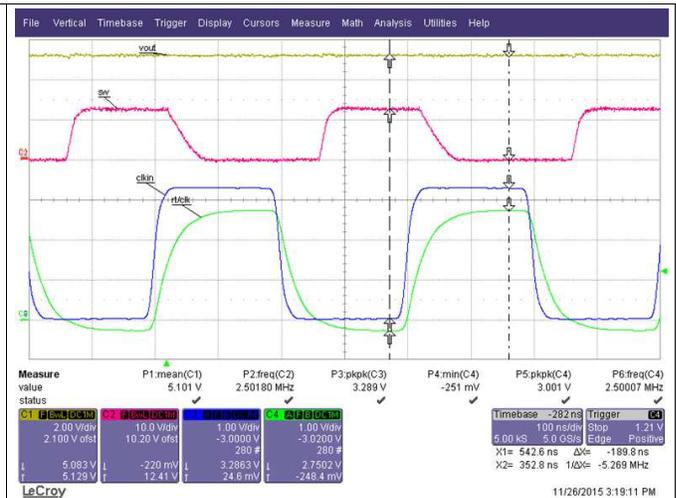## 5.4    Case 4 Results



**Figure 11. Case 4 With Clock = 1 MHz**
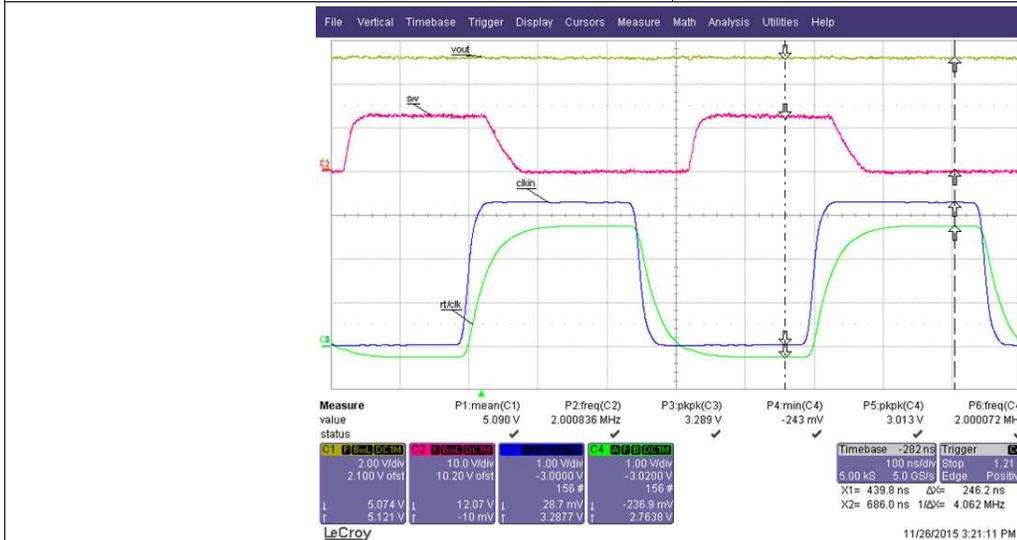


**Figure 12. Case 4 With Clock = 2.5 MHz**



**Figure 13. Case 4 With Clock = 2.0 MHz**

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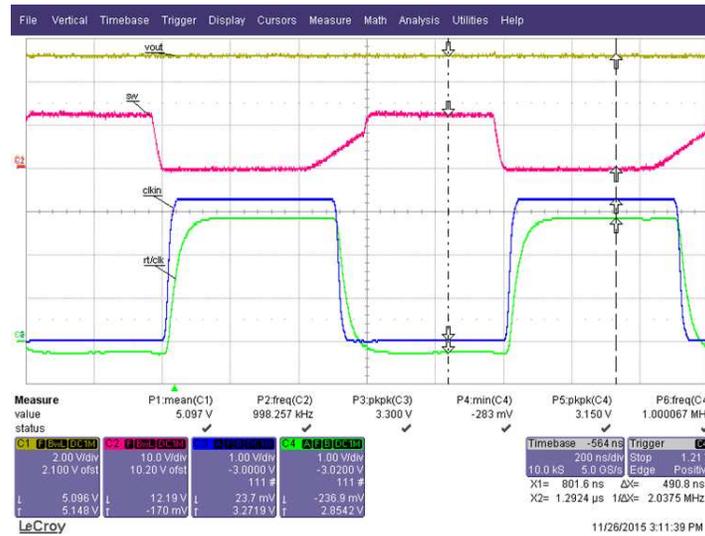
## 5.5 Case 5 Results



**Figure 14. Case 5 With Clock = 1.0 MHz**

## 6 Conclusion

Based on the measurement results, using an external Schottky diode and current limiting resistors (Figure 4), the RT/CLK pin can be interfaced to external clock sources, which are not high impedance during start up and shutdown. Results shown are based on one measurement taken on one device at room temperature. Customers need to take measurements on their board and adjust the external components accordingly to avoid the violation of datasheet specifications, as results may vary depending on the external components and also on PCB parasitics. A very-low forward-voltage Schottky with low-leakage current and fast-transient response must be used and place this diode close to the clock source for better performance.

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