Functional Safety Information

TPS7B4253-Q1
Functional safety FIT rate, FMD and Pin FMEA

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1 Overview

This document contains information for the TPS7B4253-Q1 (DDA 8-pin SO PowerPAD™ and PWP 20-pin HTSSOP (with exposed thermal pad) integrated circuit packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure modes and effects analysis (pin FMEA)

Figure 1-1 shows the device functional block diagram for reference.

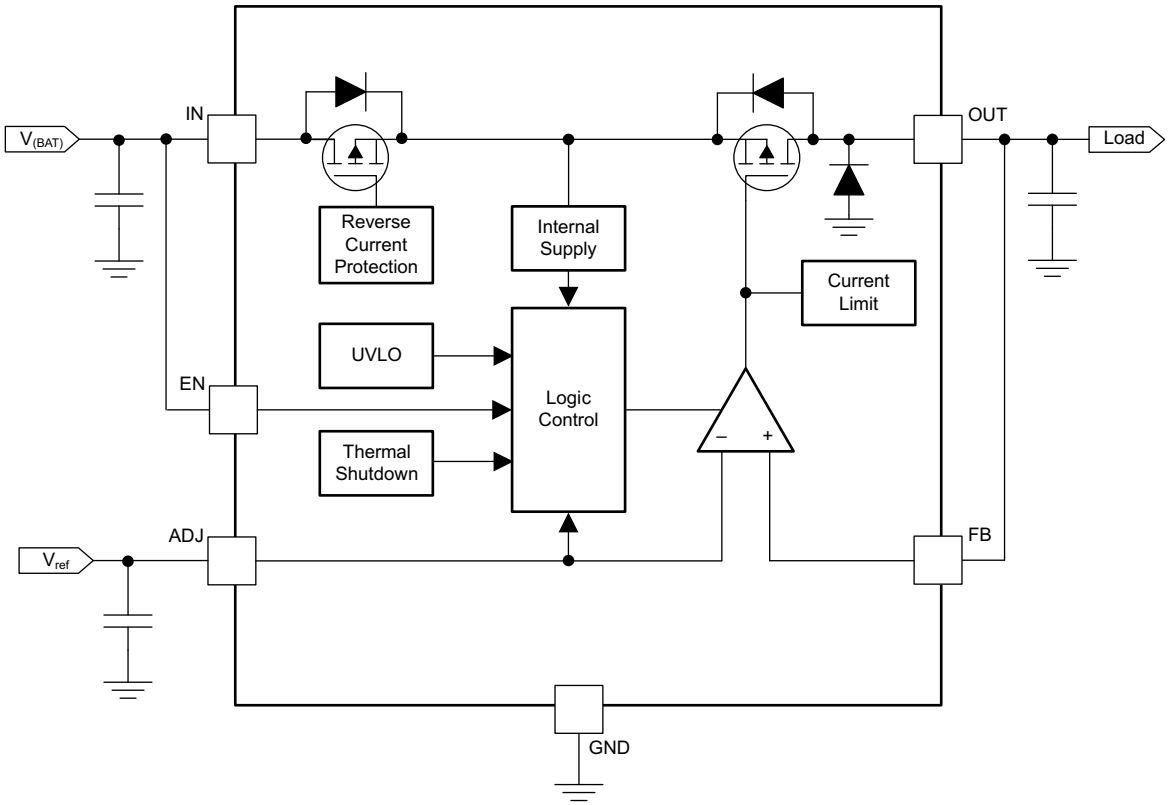

Figure 1-1. Functional Block Diagram

The TPS7B4253-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DDA 8-pin SO PowerPAD™ Package

This section provides functional safety failure in time (FIT) rates for the DDA 8-pin SO PowerPAD™ package of the TPS7B4253-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	5
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: world-wide table 8 or figure 13
- Package factor (lambda 3): table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power Amplifier and Regulator ≤ 1Watt - (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 PWP 20-pin HTSSOP (with exposed thermal pad) Package

This section provides functional safety failure in time (FIT) rates for the PWP 20-pin HTSSOP (with exposed thermal pad) package of the TPS7B4253-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	21
Die FIT rate	5
Package FIT rate	16

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: world-wide table 8 or figure 13
- Package factor (lambda 3): table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power Amplifier and Regulator ≤ 1Watt - (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B4253-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output (output low)	45
Output high (following input)	45
Short any two adjacent pins	5
Output not in specification	5

4 Pin Failure Modes and Effects Analysis (Pin FMEA)

This section provides a failure modes and effects analysis (pin FMEA) for the pins of the TPS7B4253-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V_{IN} (see Table 4-5 and Table 4-9)
- Pin short-circuited to car battery voltage (see and)

Table 4-5 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMEA in this section:

- Device operates at free-air temperatures between –40°C and 150°C.
- The ADJ and EN pins are driven from external sources.
- Device operates at an input voltage of at least 4V and no more than 40V.
- Device operates according to all recommended operating conditions and the absolute maximum ratings in the device data sheet are not exceeded.

4.1 DDA 8-pin SO PowerPAD™ Package

Figure 4-1 shows the TPS7B4253-Q1 pin diagram for the DDA 8-pin SO PowerPAD™ package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4253-Q1 data sheet.

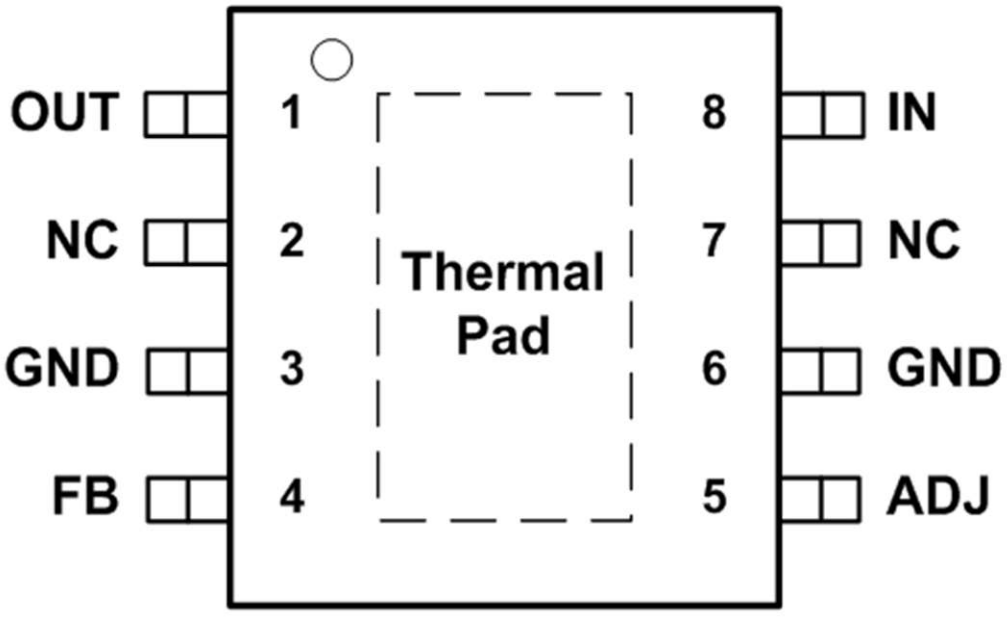

Figure 4-1. Pin Diagram (DDA 8-pin SO PowerPAD™) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
FB	4	If FB is directly connected to OUT, regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. If FB is connected by a resistor divider, V_{OUT} tracks V_{IN} minus the dropout voltage.	B
ADJ	5	The device is disabled, resulting in no output voltage.	B
GND	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC	2	No effect. Normal operation.	D
GND	3	Ground loop parasitics are increased and transient performance can be degraded.	C
FB	4	The error amplifier input is not connected. Output voltage is indeterminate.	B
ADJ	5	The device state is unknown. If the device is on, the output voltage is indeterminate.	B
GND	6	Ground loop parasitics are increased and transient performance can be degraded.	C
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC	No effect. Normal operation.	D
NC	2	GND	No effect. Normal operation.	D
GND	3	FB	If FB is directly connected to OUT, regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. If FB is connected by a resistor divider, V_{OUT} tracks V_{IN} minus the dropout voltage.	B
ADJ	5	GND	The device is disabled, resulting in no output voltage.	B
GND	6	NC	No effect. Normal operation.	D
NC	7	IN	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$.	B
NC	2	No effect. Normal operation.	D
GND	3	Power is not supplied to the device. System performance depends on upstream current limiting.	B
FB	4	Device channel is closed. If FB is tied to OUT, then $V_{OUT} = V_{IN}$. If FB is connected with a resistor divider, V_{OUT} equals V_{IN} if there is no loading on the device. If the loading on the device exceeds the leakage through the top feedback resistor, V_{OUT} is pulled to 0V.	B
ADJ	5	V_{OUT} tracks V_{IN} minus the dropout voltage.	B
GND	6	Power is not supplied to the device. System performance depends on upstream current limiting.	B
NC	7	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	8	No effect. Normal operation.	D

4.2 PWP 20-pin HTSSOP (with exposed thermal pad) Package

Figure 4-2 shows the TPS7B4253-Q1 pin diagram for the PWP 20-pin HTSSOP (with exposed thermal pad) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4253-Q1 data sheet.

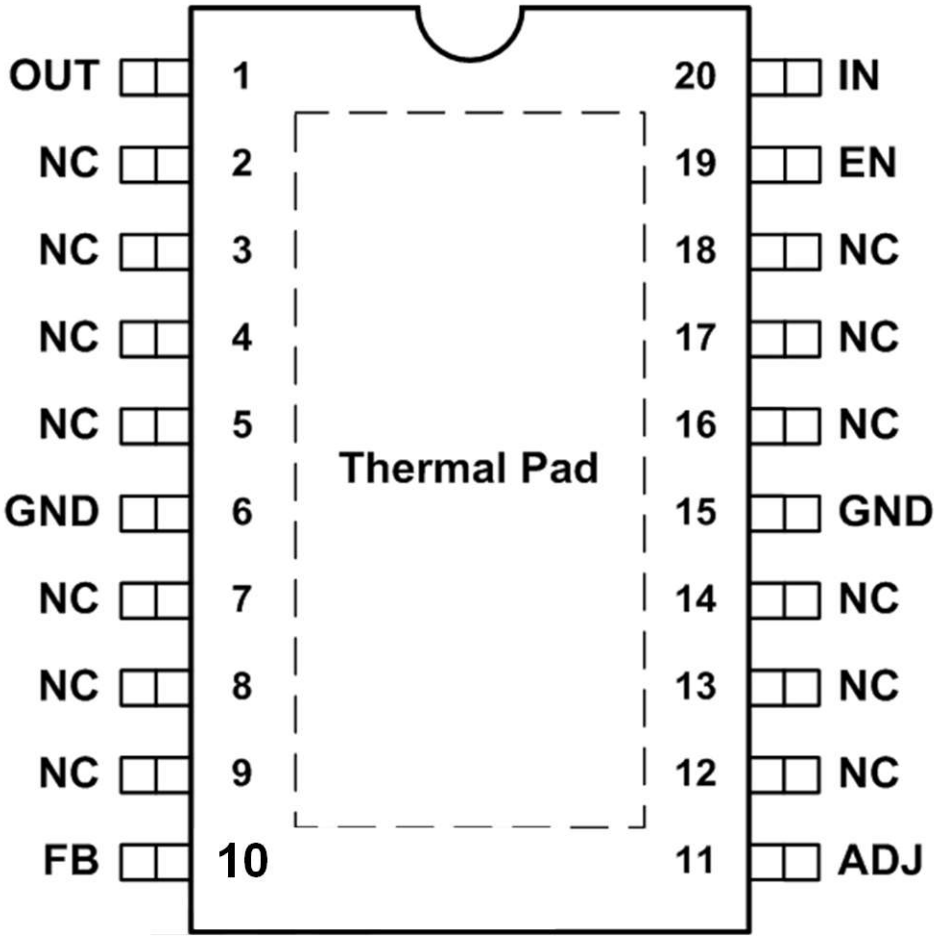

Figure 4-2. Pin Diagram (PWP 20-pin HTSSOP (with exposed thermal pad) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
NC	5	No effect. Normal operation.	D
GND	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
FB	10	If FB is directly connected to OUT, regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. If FB is connected by a resistor divider, V_{OUT} tracks V_{IN} minus the dropout voltage.	B
ADJ	11	Device is disabled, resulting in no output voltage.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	12	No effect. Normal operation.	D
NC	13	No effect. Normal operation.	D
NC	14	No effect. Normal operation.	D
GND	15	No effect. Normal operation.	D
NC	16	No effect. Normal operation.	D
NC	17	No effect. Normal operation.	D
NC	18	No effect. Normal operation.	D
EN	19	Device is disabled, resulting in no output voltage.	B
IN	20	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
NC	5	No effect. Normal operation.	D
GND	6	Ground loop parasitics are increased and transient performance can be degraded.	C
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
FB	10	The error amplifier input is not connected. Output voltage is indeterminate.	B
ADJ	11	The device state is unknown. If the device is on, the output voltage is indeterminate.	B
NC	12	No effect. Normal operation.	D
NC	13	No effect. Normal operation.	D
NC	14	No effect. Normal operation.	D
GND	15	Ground loop parasitics are increased and transient performance can be degraded.	C
NC	16	No effect. Normal operation.	D
NC	17	No effect. Normal operation.	D
NC	18	No effect. Normal operation.	D
EN	19	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
IN	20	Power is not supplied to the device.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC	No effect. Normal operation.	D
NC	2	NC	No effect. Normal operation.	D
NC	3	NC	No effect. Normal operation.	D
NC	4	NC	No effect. Normal operation.	D
NC	5	GND	No effect. Normal operation.	D
GND	6	NC	No effect. Normal operation.	D
NC	7	NC	No effect. Normal operation.	D
NC	8	NC	No effect. Normal operation.	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	9	FB	No effect. Normal operation.	D
ADJ	11	NC	No effect. Normal operation.	D
NC	12	NC	No effect. Normal operation.	D
NC	13	NC	No effect. Normal operation.	D
NC	14	GND	No effect. Normal operation.	D
GND	15	NC	No effect. Normal operation.	D
NC	16	NC	No effect. Normal operation.	D
NC	17	NC	No effect. Normal operation.	D
NC	18	EN	No effect. Normal operation.	D
EN	19	IN	Device is always enabled.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
NC	5	No effect. Normal operation.	D
GND	6	Power is not supplied to the device. System performance depends on upstream current limiting.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
FB	10	Device channel is closed. If FB is tied to OUT, then $V_{OUT} = V_{IN}$. If FB is connected with a resistor divider, V_{OUT} equals V_{IN} if there is no loading on the device. If the loading on the device exceeds the leakage through the top feedback resistor, V_{OUT} is pulled to 0V.	B
ADJ	11	V_{OUT} tracks V_{IN} minus the dropout voltage.	B
NC	12	No effect. Normal operation.	D
NC	13	No effect. Normal operation.	D
NC	14	No effect. Normal operation.	D
GND	15	Power is not supplied to the device. System performance depends on upstream current limiting.	B
NC	16	No effect. Normal operation.	D
NC	17	No effect. Normal operation.	D
NC	18	No effect. Normal operation.	D
EN	19	Device is always enabled.	B
IN	20	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2015) to Revision A (February 2025) **Page**

- Updated document to current TI technical writing standards and template....2
- Removed *Abstract* section....2
- Added *Overview*, *Functional Safety Failure In Time (FIT) Rates*, and *Failure Mode Distribution (FMD)* sections and pertinent data....2

- Updated the *Pin FMEA* and *Pin Configuration and Functions* sections to the *Pin Failure Modes and Effects Analysis (Pin FMEA)* section..... 2

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