Application Report
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TPS23861 Power-On Considerations

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ABSTRACT

TPS23861 is an IEEE 802.3at compliant PSE controller containing both analog and digital circuits as well as an embedded processor. The VPWR pin supplies power to the internal analog circuits while the VDD pin supplies power for the digital circuitry and processor. Each power supply pin monitors input voltage and creates an internal power on reset for the internal circuits. Additionally, the $\overline{\text{RESET}}$ pin forces all internal registers to their default power on state. It is important for any integrated circuit with digital content to power on in a well-controlled and consistent manner in order to prevent erratic operation. This principle also applies to TPS23861 and this report discusses several proven power on methods for TPS23861.

1 TPS23861 Basic Power-on

TPS23861 under-voltage lockout (UVLO) threshold at power on is 18.5 V maximum (V_{UVLOPW_R}) for VPWR and 2.8 V maximum (V_{UVDD_R}) for VDD. It is good engineering practice to hold the $\overline{\text{RESET}}$ pin in a low state until both VPWR and VDD have exceeded their respective UVLO rising thresholds. An example of this is shown in Figure 1.

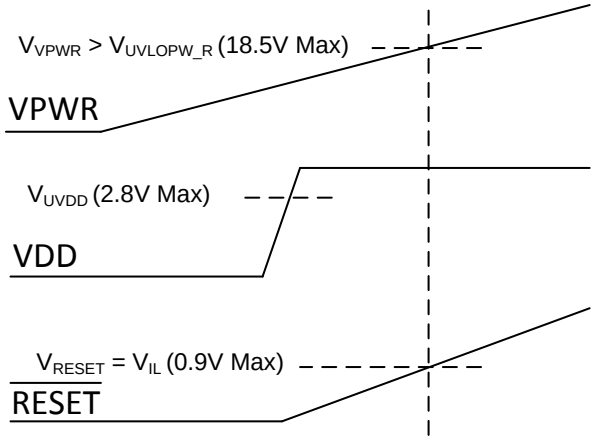

Figure 1. TPS23861 Power On Sequence

In Figure 1, VPWR starts rising before the VDD rail which is the typical case because the VDD rail is usually derived from the VPWR rail. The VDD rail will turn on when VPWR reaches the externally programmed or internal UVLO of the VDD rail. Also of note in Figure 1 is that $\overline{\text{RESET}}$ starts rising when VDD starts rising because the $\overline{\text{RESET}}$ pin is pulled up to the VDD pin (either externally or internally using the TPS23861 internal pullup).

2 TPS23861 Power-on using VDD regulator UVLO > V_{UVLOPW_R}

Figure 2 illustrates how the VDD regulator can be configured so that it ramps up VDD after VPWR exceeds V_{UVLOPW_R}. Resistors R_{UP} and R_{DOWN} are chosen accordingly based on the turn on threshold of the VDD regulator internal reference threshold (VREF).

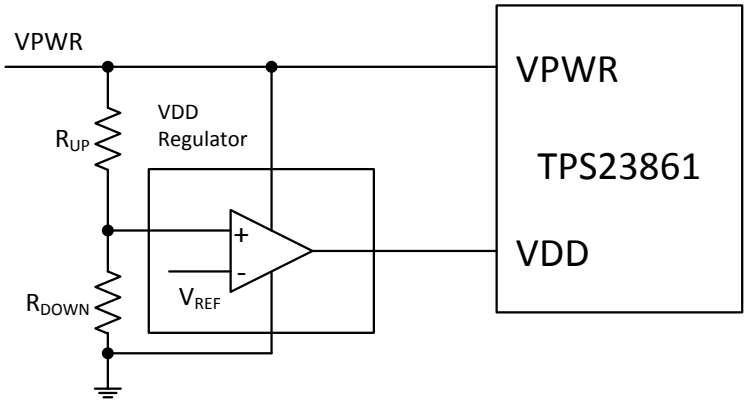

Figure 2. VDD Rail Turns On When VPWR > V_{UVLOPW_R}

LM5019MRX can be used with R_{UP} = 200 kΩ and R_{DOWN} = 13.3 kΩ for a UVLO of 19.65 V and hysteresis of 4 V. Alternatively if only a single TPS23861 is used in the system then a TPS7A4001 (LDO) can be used with R_{UP} = 825 kΩ and R_{DOWN} = 32.4 kΩ.

3 TPS23861 Power-on Using Delayed RESET

Figure 3 illustrates the use of an external capacitor (C_{RST}) and the internal $\overline{RESET}$ pullup resistor (R_{PULLUP}) to implement the required delay, T.

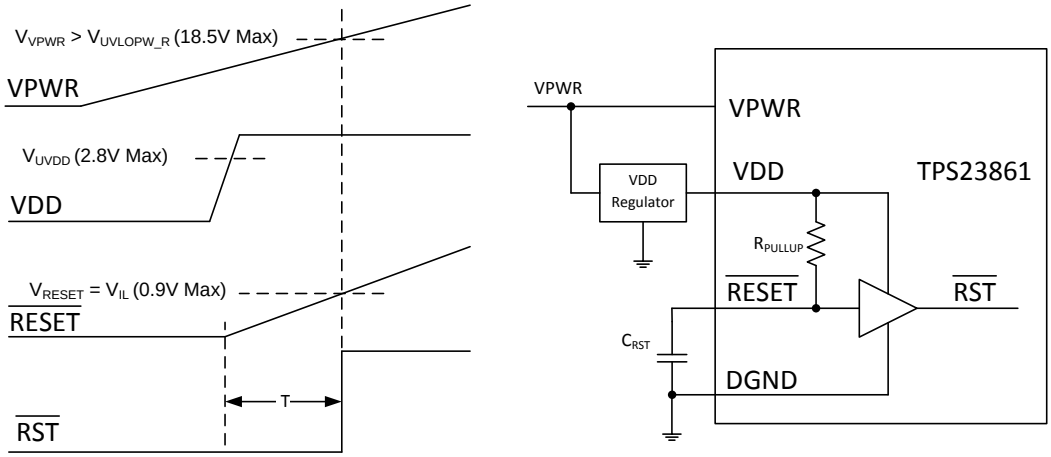

Figure 3. Using C_{RST} for Delay

The required value for C_{RST} can be calculated using Equation 1.

$$C_{RST} = \frac{-T}{R_{PULLUP} \times LN\left(1 - \frac{V_{RESET}}{V_{VDD}}\right)} \quad (1)$$

For example, for T = 5 ms, R_{PULLUP} = 30 kΩ ($R_{PULLUP\text{-}MIN}$), V_{RESET} = 0.9 V, V_{VDD} = 3.3 V, the required C_{RST} = 523 nF. Choosing C_{RST} = 560 nF yields T with some additional margin (5.35 ms).

When more than one TPS23861 shares the same $\overline{RESET}$ signal, the internal pullup resistors act in parallel resulting in a lower equivalent R_{PULLUP}. The required value of C_{RST} must be multiplied by the number of devices sharing the $\overline{RESET}$ signal to yield the desired delay, T.

4 Host Managed RESET Using a Digital Isolator

Figure 4 illustrates host side control of the $\overline{\text{RESET}}$ pin sequence through a digital isolator. The isolator can be either a simple photo-coupler or a high performance device such as the ISO72XX family of digital isolators.

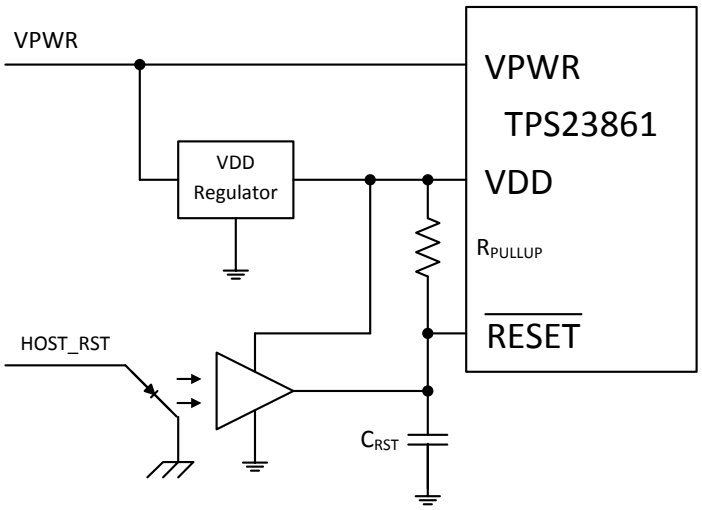

Figure 4. Host Side $\overline{\text{RESET}}$ Control

The TI recommended system power up sequence starts with the host side first so that control of the HOST_RST signal can ensure that the $\overline{\text{RESET}}$ signal is held low before VPWR and VDD power on. Host management of the $\overline{\text{RESET}}$ pin delay depends on the isolator type. Several isolator types and delay methods are described.

- Simple “photo-coupler” such as CEL PS8821-1 with open collector outputs: Since the photo-transistor does not require power from VDD, $\overline{\text{RESET}}$ can be kept low (optically) by the host until TPS23861 is powered. If additional delay is required, then C_{RST} can be added.
- High performance isolator powered by VDD such as CEL PS9821-1 with open collector outputs: Since the $\overline{\text{RESET}}$ pin may not be held low until VDD is powered, the isolator cannot respond to the HOST_RST signal. For this case, C_{RST} should be used to implement the required delay.
- High performance isolator powered by VDD such as TI ISO7241C with push-pull outputs and enable inputs: Delaying the $\overline{\text{RESET}}$ pin is possible if the isolator enable and $\overline{\text{RESET}}$ driver are delayed using capacitors. For this case, a capacitor, C_{EN2} is required on the ISO7241C EN2 pin along with C_{RST} on the $\overline{\text{RESET}}$ pin to implement the overall delay. A VDD regulator with programmable UVLO is a simpler solution when using this isolator type.
- High performance isolator powered by VDD such as TI ISO7221B with push-pull outputs: Delaying the $\overline{\text{RESET}}$ pin is ineffective with a push-pull type output because the high side driver strength overcomes the R_{PULLUP}. If this isolator type is used, then a VDD regulator with programmable UVLO must be used.

5 I²C Command Initialization at Power On

At power on, TPS23861 goes through an initialization sequence. This sequence starts after both VPWR and VDD have exceeded their respective UVLO rising thresholds. The initialization sequence is shown in Figure 5.

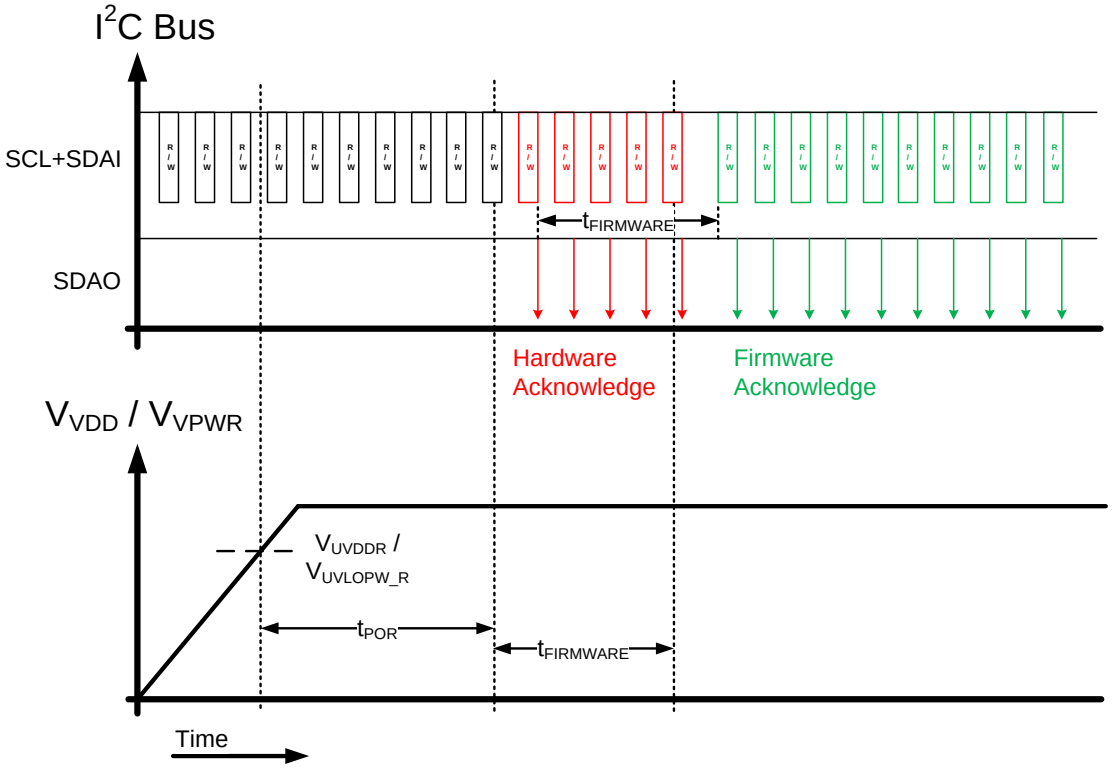

Figure 5. Internal Power On Initialization

After both VPWR and VDD have exceeded their respective UVLO rising thresholds, the TPS23861 device hardware initializes for t_{POR} (23 ms maximum). During t_{POR}, TPS23861 does not respond (ACK or acknowledge) to I²C commands. After t_{POR} TPS23861 accepts and acknowledge commands but does not process the commands until the internal firmware has initialized ($t_{FIRMWARE}$). Firmware initialization typically takes about 20 ms.

TI recommends that the host I²C controller waits for > 43 ms after power on before sending the TPS23861 initialization command sequence for the particular application. Alternatively, the host I²C controller can ping the TPS23861 during power on (assuming that the host side controller is powered on and functional before TPS23861 is powered on) and implement a delay between the first ACK and sending the formal command sequence.

6 Conclusion

Several methods of TPS23861 power up have been discussed. The simplest method (#1) uses a VDD regulator with programmable UVLO so that $\overline{\text{RESET}}$ does not require delay management.

If the VDD regulator UVLO cannot be programmed then $\overline{\text{RESET}}$ delay management using method 2 or 3 is sufficient.

1. C_{RST} without host control, OR
2. C_{RST}, plus an open collector isolator plus host control

7 References

1. Data Sheet: *TPS23861 IEEE 802.3at Quad Port Power-over-Ethernet PSE Controller* (SLUSBX9)

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