Application Report
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Handling System Transients in Hot Swap Applications

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ABSTRACT

Hot Swap circuits are critical for inrush management and fault protection in high availability systems. To protect the bus and ensure system availability, Hot Swaps are designed to quickly shut off in case of faults with a downstream load. It is also typical for the bus to experience various transients from adjacent card insertion/removal and faults on adjacent cards. These transients can appear as an over-current condition to the Hot Swap circuit and can cause undesired shut downs that are often referred to as a nuisance trips.

This report provides theoretical analysis and experimental results of this phenomenon. In addition, application level solutions are proposed to ensure robust designs.

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1 Transients Experienced by Hot Swaps in a Backplane

1.1 General System Overview

To understand the typical transients experienced by a Hot Swap, the typical backplane should be considered. Figure 1 provides a simplified diagram to demonstrate the key parameters that relate to the Hot Swap. For most systems the following is true:

- C_{BULK} is the input to the DC/DC converters and is large. The Hot Swap manages the inrush current to C_{BULK} by gradually turning on the Hot Swap FET.
- C_{IN} is generally quite small and combines the effect of real and parasitic capacitance that is “hot-plugged” into the bus.
- The backplane has little capacitance and the cards are far away from the DC source (V_{BUS}), which results in significant inductance from V_{BUS} to input of the cards (L_{SUPPLY}).
- The card to card inductance ($L_{CARD-CARD}$) is small, because the cards are close to each other.
- Since $L_{CARD-CARD}$ << L_{SUPPLY} the transients caused by insertion/removal/faults on card B translates into a voltage and/or current transient on card A.

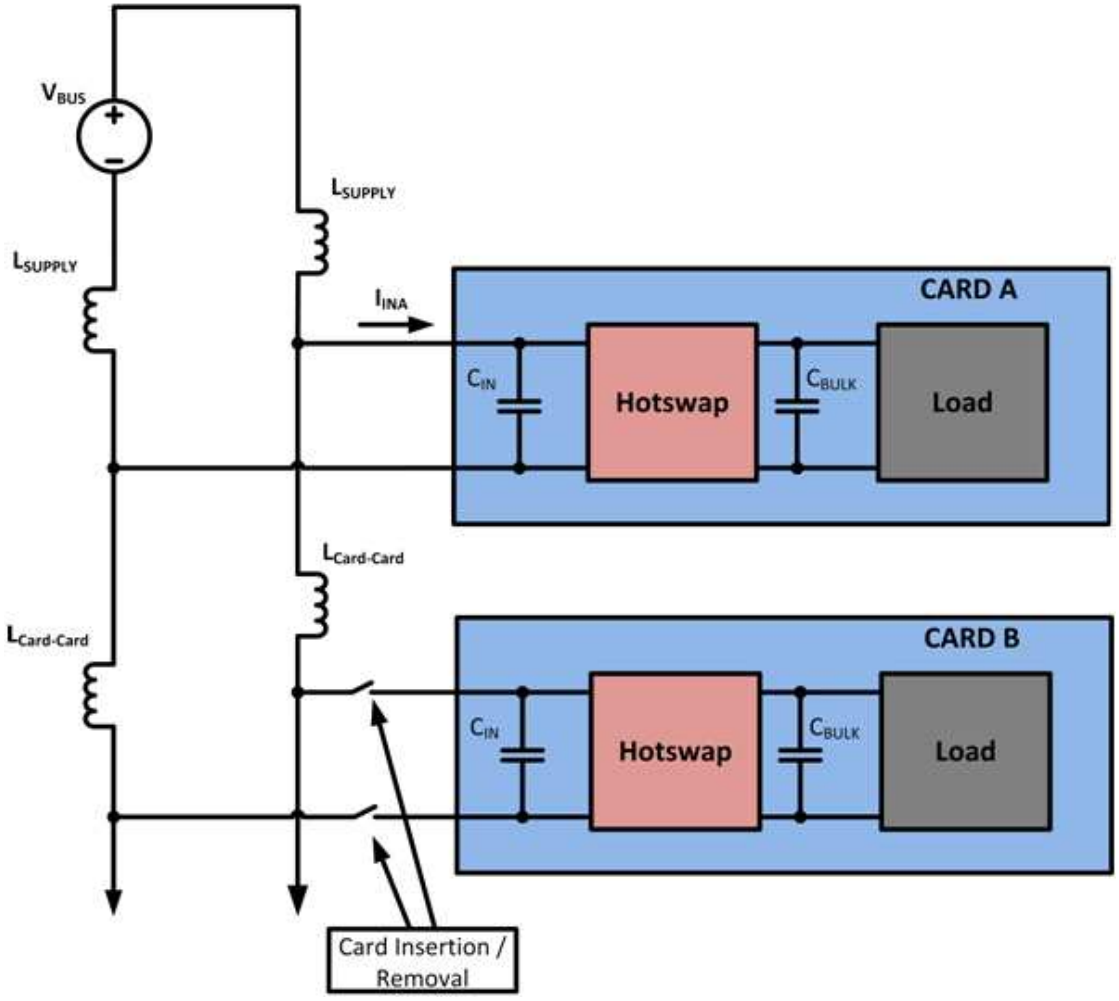

Figure 1. Key System Considerations for Hot Swap Design

1.2 Experimental Set-up for Exploring Card to Card Interactions

To better understand the nature of the transients present in a typical backplane, lab experiments were performed using two LM5066 EVMs. To best mimic a real system, the shortest available cables were used to connect the two EVMs. Long cables were connected to a low impedance source provided by the bulk cap on the output of the power supply as shown in Figure 2.

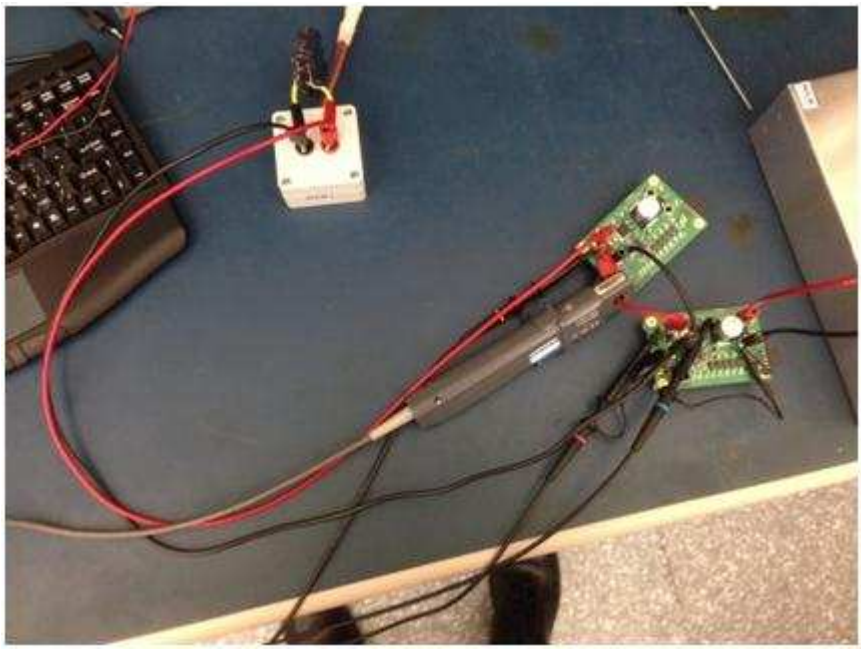

Figure 2. Experimental Set-up for Understanding Card-to-Card Interactions

Unless otherwise noted, the experiments were performed with the setting summarized in Table 1.

Table 1. Settings for Exploring Card-to-Card Interactions

Category	Value	Comments
R_{SNS}	3 mΩ	EVM setting
COUT	220 µF	EVM setting
CL setting	26 mV	Current limit of ~8 A
CB setting	~50 mV	Circuit breaker limit of ~16 A
L_{SUPPLY}	>1 µH	Inferred from test results
$L_{CARD-CARD}$	~250 nH	
C_{IN} (with parasitics)	3 nF	
Filtering?	no	

1.3 Adjacent Card Insertion

When a card is inserted, its input capacitor is charged to V_{BUS}, pulling charge out of the bus and causing an LC ring. This results in transients on adjacent cards, which could cause a nuisance trip. The following occurs when card B is "hot-plugged" and card A is ON with no load:

- Since L_{SUPPLY} >> $L_{CARD-CARD}$, C_{IN} of card B is charged from card A, resulting in negative I_{INA}.
- There is an LC ring of both V_{INB}, and I_{INA}, which dampens out due to parasitic resistance.
- The transient on VINA is much smaller than the transient on V_{INB}, because $L_{CARD-CARD}$ along with C_{BULK} provides filtering.
- I_{INA} does not exceed the CB threshold of ~16 A and the gate voltage of card A stays high.

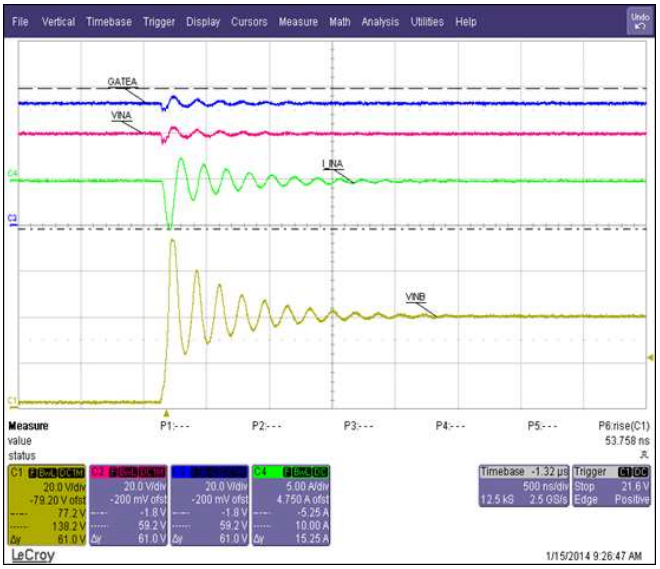

Figure 3. Adjacent Card Insertion, $I_{LOAD,A}$ = 0 A

Finally, the total input capacitance of the EVM (C_{IN}) can be estimated from Figure 3. The period of the ring is ~ 200 ns. C_{IN} is charged from 0 V to 40 V in the first ¼ of the period and the peak current from card A to card B is 5 A. Using Equation 1, C_{IN} is estimated to be 3 nF. Given that the real input capacitor is 1 nF, the other 2 nF can be attributed to the parasitics of the board, the Hot Swap FET, and the input TVS.

$$C_{IN} \times \Delta V_{IN} = \int i \times dt \geq C_{IN} = \frac{50\ ns \times 5A / 2}{40\ V} \sim 3\ nF \tag{1}$$

The behavior is similar when there is a load on card A, but this moves the $I_{IN,A}$ waveform by the load current. Using maximum current is the worst case, because the maximum $I_{IN,A}$ comes closest to the circuit breaker threshold.

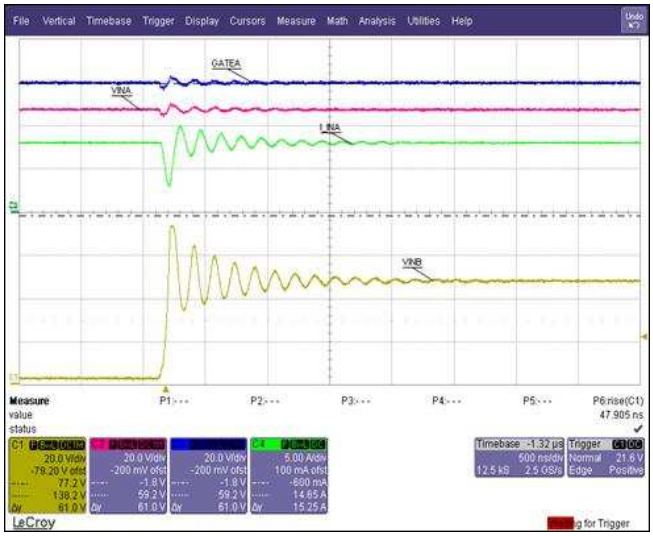

Figure 4. Adjacent Card Insertion, $I_{LOAD,A}$ = 7.5 A

These tests were performed for several other conditions listed in the Table 2. Note that a lower $L_{CARD-CARD}$ would result in ringing on $V_{IN,A}$ that is higher amplitude and higher frequency. This could result in a maximum current going above the CB threshold and causing a nuisance trip.

Table 2. Test Results for Adjacent Card Insertion

V_{IN}	CL Setting	LOAD A	Gate Tripped?
48	50 mV	0 A	No
65	50 mV	0 A	No
40	50 mV	0 A	No
48	50 mV	8 A	No
48	26 mV	0 A	No
40	26 mV	8 A	No

1.4 Adjacent Card Removal

Removal of a card can also cause a transient on an adjacent card. Several test conditions were evaluated and are summarized in the table below.

Table 3. Test Results for Adjacent Card Removal

V_{IN}	CL Setting	LOAD A	LOAD B	Gate Tripped?
48	26 mV	0 A	8 A	N
48	26 mV	8 A	8 A	N
48	26 mV	0 A	11 A	N
48	26 mV	8 A	12 A	Y

Figure 5 shows the waveform for a typical case. Here both cards are running close to full load (a little under current limit) and card B is removed. The following occurs:

- Since L_{SUPPLY} >> $L_{CARD-CARD}$, I_{SUPPLY} continues to be ~ 16 A
- Most of the I_{SUPPLY} goes into card A and I_{INA} rises up to 14 A.
- 14 A is below the circuit breaker threshold and the gate of the FET stays high.
- I_{INA} slowly returns to the original 8 A level. The di/dt is low, because L_{SUPPLY} is large and the $V_{L,Supply}$ is small (< 1 V).

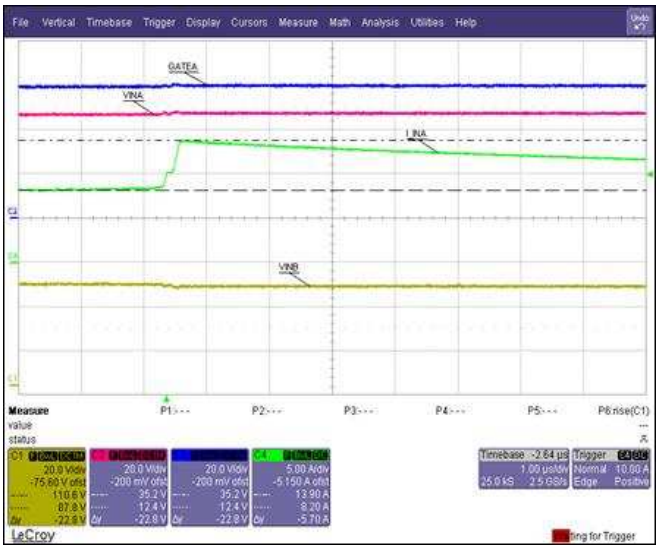

Figure 5. Adjacent Card Removal ($I_{LOAD,A}$ = $I_{LOAD,B}$ ~8 A)

Figure 6 shows the waveform for an atypical case. Here the load current of card B is 13A, which is above the current limit of card A. This is not the case in most systems, but serves as a good example. The following occurs:

- Since L_{SUPPLY} >> $L_{CARD-CARD}$, I_{SUPPLY} continues to be ~ 21 A.
- All of the I_{SUPPLY} goes into card A and I_{INA} rises up to 21 A.
- 21 A is above the circuit breaker threshold and the gate of the FET is quickly pulled down.
- When the gate is turned off, this causes a sudden interruption in $I_{IN,A}$ and the voltage on V_{INA} spikes up followed by a ring.

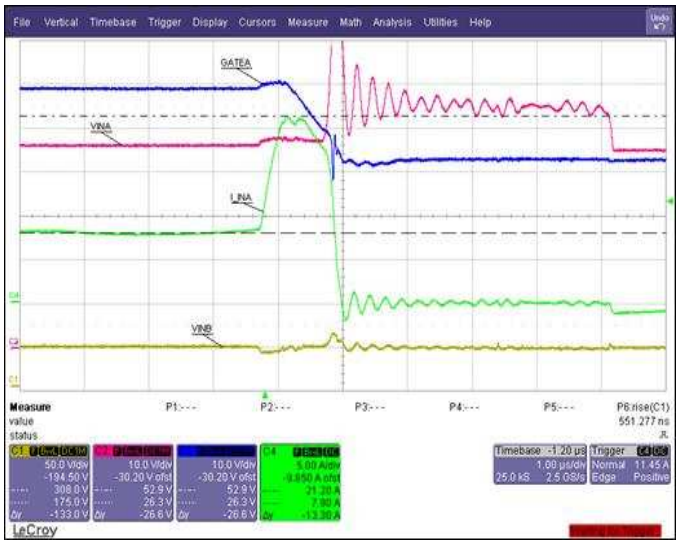

Figure 6. Adjacent Card Removal ($I_{LOAD,A}$ = 8 A, $I_{LOAD,B}$ ~12 A)

2 The Response of LM5066 EVM to Transients

Section 1 focused on identifying the typical transients that can be seen by a Hot Swap in a backplane. In this section arbitrary transients are applied to the EVM to check its behavior.

2.1 Set-up for Transient Testing

Two types of transient injection methods were used. The first one shown in Figure 7 relies on a power MOSFETs that is connected to a function generator. Since an electrical signal is used to generate the transient, this method is referred to as “Electrical Glitching”.

V_{BIAS} determines the amplitude of the transient injected into V_{GLITCH}. For example, if V_{BIAS} = 10 V when the FET turns ON, the lower node of the capacitor goes to zero (a 10-V step), which results in a 10-V step on the V_{GLITCH} node. The frequency of the transient is determined by the LC time constant. Thus different glitch capacitors generate transients of a different frequency. With this set-up a variety of transients can be injected onto the EVM to find out which ones would make it “trip”. The wire from V_{GLITCH} to V_{IN} was ~2” so that a current probe can be used in order to measure I_{INA}.

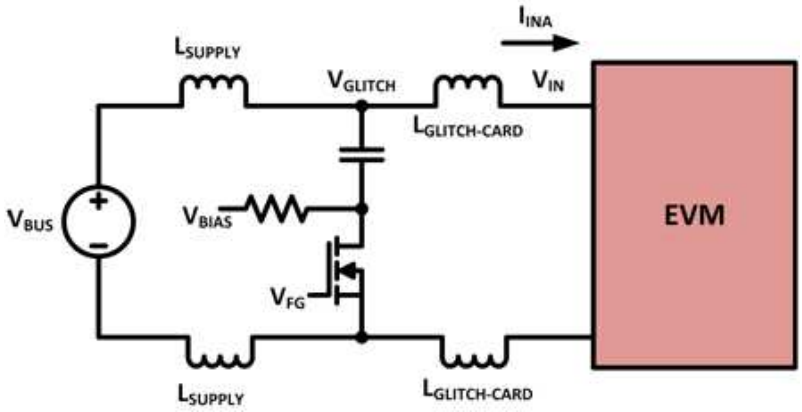

Figure 7. Set up for Electrical Glitching

The second method relies on simply shorting a cap onto V_{IN}. A resistor is used to pre-bias the capacitor to 0 volts. The capacitor is connected directly on the V_{IN} of the EVM, which prevents the measurement of I_{INA}. However, this removes the $L_{GLITCH-CARD}$ allowing for faster transients to be injected on the EVM. Since the transient is injected by physically connected the positive side of the cap to V_{IN}, this is referred to as “Mechanical Glitching”.

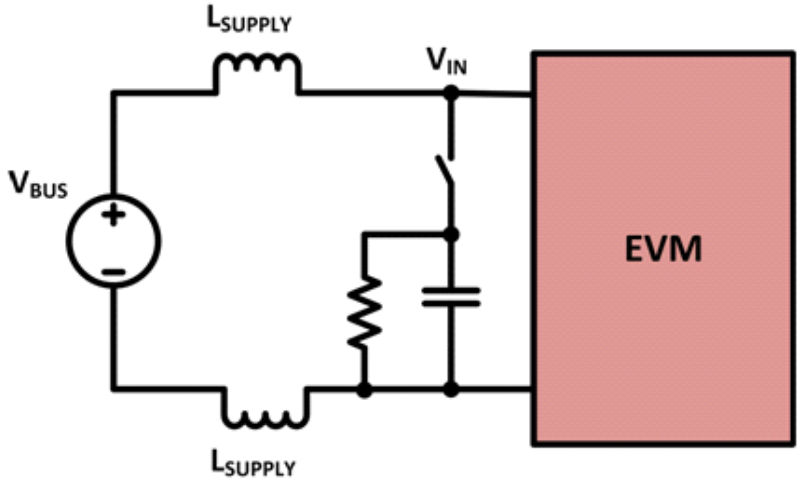

Figure 8. Set up for Mechanical Glitching

2.2 Transient Testing Results with the EVM

Table 4 summarizes the results of the “Electrical Glitching” that was performed on the LM5066 EVM. The experiments were performed with a maximum load, since that is the worst case, because the transient adds on top of the DC input current. In general, a gate trip occurred when the maximum input current was around or above the circuit breaker threshold. Note that the threshold is lower for higher frequency transients that were generated with a lower size capacitor. This can attributed to the inductance of the sense resistors and some sensitivity of the part to common mode and will be described in the following sections.

Table 4. Electrical Glitching Test Results on the EVM

V_{IN}	CL Setting	C_{GLITCH}	LOAD A	V_{BIAS}	Gate Tripped?	$I_{IN,MAX}$
48 V	26 mV	10 nF	8 A	35 V	N	12.5 A
48 V	26 mV	10 nF	8 A	40 V	Y	12.6 A
48 V	26 mV	100 nF	8 A	20 V	N	15 A
48 V	26 mV	100 nF	8 A	25 V	Y	19 A
48 V	26 mV	600 nF	8 A	15 V	N	19 A
48 V	26 mV	600 nF	8 A	20 V	Y	22 A

The waveform in Figure 9 is an example of the response of the LM5066 EVM to a transient generated with a 100 nF glitch capacitor and V_{BIAS} = 25 V. The voltage glitch on V_{GLITCH} results in a current transient on I_{INA} due to C_{BULK}. $I_{IN,A}$ exceeds the CB threshold, which results in the gate falling.

Figure 9. V_{IN} Transient Generated by V_{BIAS} = 25 V and C_{GLITCH} = 100 nF

2.3 Mechanical Glitching

To test the EVM with very fast transients the $L_{GLITCH-CARD}$ has to be minimized. To accomplish this, a capacitor was directly hot-plugged on the V_{IN} as shown in Figure 8. Unfortunately, the input current cannot be measured with this set-up. A 1-µF ceramic capacitor was added on the output. As a result this helps to limit the transient on V_{IN}, because 1 µF >> 3 nF.

Note that every comparator has some susceptibility to high amplitude and fast common mode transients. The 1-µF output capacitor serves to limit the common mode seen by comparator. Note that the V_{IN} transient is not completely squashed due to impedance between V_{IN} and C_{OUT}. The theory is discussed further in the next section.

The result is shown in Figure 10. Note that there was no load current for this experiment and the voltage transient is roughly 7 V.

Figure 10. Mechanical Glitch With a 1-µF C_{OUT}

Additional experiments were performed and are shown in Table 5. Note that gate trips were observed when there was a load current present. This is consistent with previous results. Note that the addition of C_{OUT} does generate a current transient through R_{SENSE} creating a differential voltage which can result in the circuit breaker tripping. This is analyzed further in *Section 3*.

Table 5. Mechanical Glitching Test Results on the EVM

V_{IN}	CL Setting	C_{GLITCH}	LOAD A	C_{OUT}	Gate Tripped?
48	26 mV	3 nF	0 A	1-µF ceramic	N
48	26 mV	3 nF	8 A	1-µF ceramic	Y
48	26 mV	8 nF	0 A	1-µF ceramic	N
48	26 mV	8 nF	8 A	1-µF ceramic	Y

3 Mitigating Nuisance Trips in Hot Swap Circuits

Managing the common mode and differential signal across V_{IN_K} and V_{SENSE} is the key to preventing nuisance trips in Hot Swap circuits. This section provides further theoretical insight along with experimental results to show how this can be accomplished.

3.1 Understanding Key Parasitics in the Hot Swap Circuit

Figure 11 shows the key components and parasitic elements that need to be considered when evaluating the differential and common mode signal seen on $V_{IN,K}$ and V_{SENSE}. The designer should keep the following in mind:

- $L_{GLITCH,VIN}$ is the inductance between the source of the transient (ie adjacent card) and the board under test. Larger $L_{GLITCH,VIN}$ helps decouple the transients between cards. It is a combination of parasitic inductance and the inductance of a series inductor (if added).
- The sense resistor has an inductance between 1 nH and 5 nH, which could add significantly to $V_{IN\_K} – V_{SENSE}$, when large di/dt is present.
- C_{OUT} is quite large and reduces the common mode seen on $V_{IN,K}$ and V_{SENSE}. However, the series inductance from C_{OUT} to V_{SENSE} reduces its impact. It is effectively an inductor divider with $L_{GLITCH,VIN}$.
- Since the FET is ON, its resistance is very small and it is essentially a short. The FET inductance is not specified on all FETs, but is ~12 nH for a FET in a D2PACK (IRLR3110).

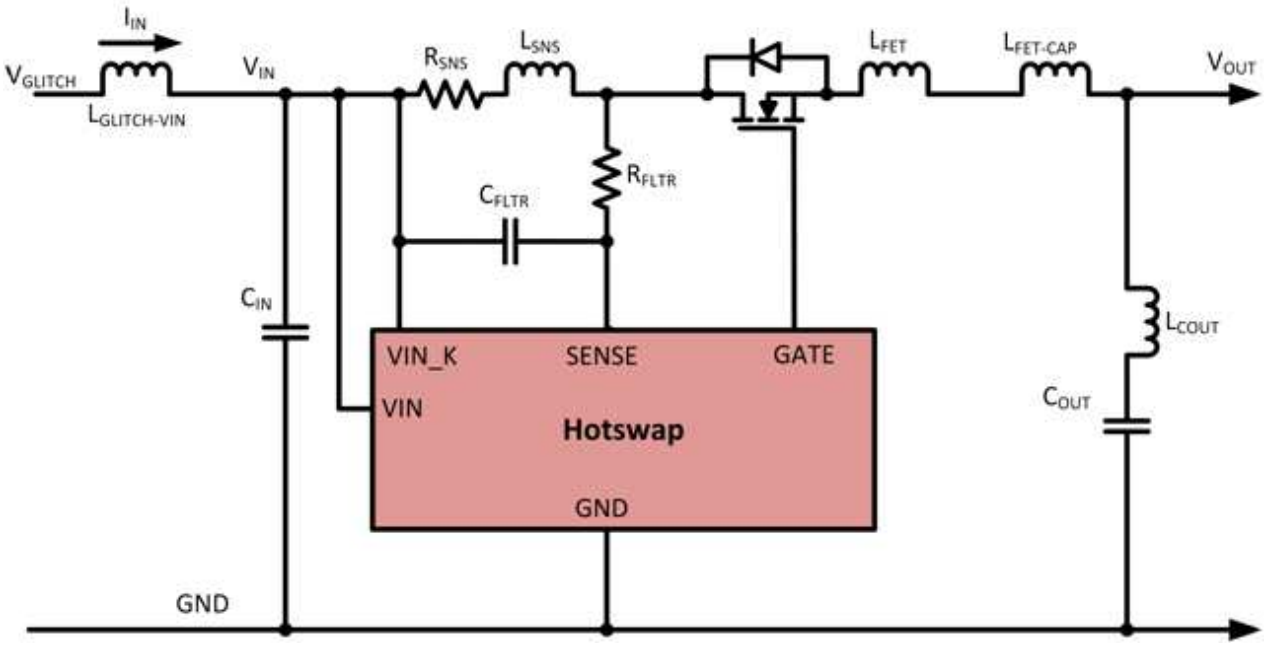

Figure 11. Hot Swap Circuit With Key Parasitics

3.2 Controlling the Differential Signal ($V_{IN\_K} – V_{SENSE}$)

To work around the differential signal that appears across R_{SNS}, use an RC filter as shown in Figure 11. Note that the SENSE pin will draw ~25 µA of current, which introduces a voltage offset into current monitoring. However, as long as a low R_{FLTR} is used this offset can be minimized.

Also note that adding a differential filter increases the response time of the Hot Swap to a short circuit. The RC value has to be tuned to optimize the short circuit response and the immunity to nuisance trips.

3.3 Controlling the Common Mode on V_{IN_K} and V_{SENSE}

Controlling the common mode signal is trickier than the differential signal. It is tempting to use an RC network to filter the common mode. However, any mismatch in the filtering of V_{IN_K} and SENSE would result in a common mode to differential mode conversion exacerbating the problem.

For a given transient, using a larger C_{IN} would definitely reduce the perturbation on V_{IN} and SENSE. However, C_{IN} is hot-plugged so increasing its value would result in larger perturbations.

The following would help avoid nuisance trips from common mode signal on V_{INK} and V_{SENSE}:

- Minimize $L_{FET-CAP}$, by placing the C_{OUT} next to the FET.
- Minimize L_{CAP}, by using a ceramic 1-µF capacitor on C_{OUT} in addition to any bulk electrolytic capacitor that is already used. Note that 1 µF >> C_{IN}, so it should absorb the transient introduced from an adjacent card insertion.
- Keep the sense resistor close to the FET to avoid additional parasitic inductance.
- Add a real inductor to increase $L_{GLITCH-VIN}$. The saturation current of the inductor should be larger than the maximum load current to avoid saturation.
- Using a higher CB threshold by setting the CB/CL ratio bit to 1 (CB/CL ratio ~3.9) or using a CL = 50 mV.

3.4 Experimental Results

To test the proposed solutions the following settings were used on a TI evaluation board:

- C_{OUT} = 1 µF. Ceramic capacitor was used to improve response to fast transients
- R_{FLTR} = 0.3 Ω and C_{FLTR} = 1 µF for a 300 ns time constant on the circuit breaker.
- Sense resistor of 2 mΩ (standard setting)
- CL setting of 26 mV and a load current of 11 A (close to max)

Then several tests were performed to evaluate the worst case conditions as shown in Table 6.

Table 6. Test Results with C_{OUT} and Differential Filtering

Glitch Type	V_{IN}	C_{GLITCH}	Gate Tripped?
Mechanical	48	3 nF	N
Mechanical	48	8 nF	N
Electrical – V_{BIAS} = V_{IN}	48	10 nF	N
Electrical – V_{BIAS} = V_{IN}	48	100 nF	N
Electrical – V_{BIAS} = V_{IN}	48	600 nF	Y

The gate did not trip for neither of the mechanical glitches, which would be considered the worst case. The gate trip did occur when a 600 nF C_{GLITCH} was used. Note that hot-plugging a 600-nF capacitor on the bus is not a real system usage case, because the typical C_{IN} of the board is < 10 nF.

3.5 Considerations For Systems with Multiple Cards

Note that most systems will have more than 2 cards plugged in at a time. In this case, a transient caused by a card insertion/removal/fault is split up amongst the nearby cards. It is split based on the parasitic inductance of each card to the one that had an insertion/removal/fault. Therefore, the experiments shown in this report can be considered as “worst case condition” and a typical system would exhibit better performance.

3.6 Ensuring that a Hot Swap Design Passes with Margin

Since nuisance trips are dependent on the system and layout Parasitics, it is hard to ensure that a given board design will pass all of the conditions desired by the user. The design needs to be tested in a real system and tweaked as necessary.

Many designers will want to ensure there is margin in their design. This can be accomplished with the procedure outlined in Table 7. In a typical usage case, the input capacitance of card A and card B is matched and could equal 3 nF. Also, the designer may set R_{FLTR} x C_{FLTR} = 0.6 µs. The margin can be checked by performing a test in the right column. By doubling the C_{INB} the transient seen by card A is increased and by reducing the filtering time constant the sensitivity of card A to transients is also increased. Thus if the board passes this test, the designer will have confidence that the design is robust.

Table 7. Example Test to Ensure Margin with Adjacent Card Insertion

	Standard Usage Case	Checking Margin
C_{INA}	3 nF	3 nF
C_{INB}	3 nF	6 nF
Differential RC filter time constant	0.6 µs	0.3 µs

Some systems may require that a short circuit fault on a card does not cause a nuisance trip on any of the adjacent cards. Note that this is tough to pass and may require an input inductor. A similar procedure can be used to check margin for this test condition. This is shown in Table 8. The hot-short is applied to card B and using a longer time constant results in a slower response time of card B and a more severe transient on the bus. Using a shorter time constant on card A makes it more sensitive to transients. Again, passing this test case provides the designer with confidence that the design is robust.

Table 8. Example Test to Ensure Margin with Adjacent Card Hot-Short

	Standard Usage Case	Checking Margin
C_{INA}	3 nF	3 nF
C_{INB}	3 nF	3 nF
Differential RC filter time constant on Card A	0.6 µs	0.3 µs
Differential RC filter time constant on Card B	0.6 µs	1.2 µs

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