Application Report
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Voltage-Level Translation With the LSF Family

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ABSTRACT

This document discusses applications for the LSF family of devices when used as bidirectional voltage translators. It includes theory of operation, example applications, example schematics, component sizing guidelines, and performance plots.

Topic **Page**

1 LSF Theory of Operation

This application report discusses the LSF family. This family of devices consists of passive FET switches that use external pullup resistors to translate between voltage levels. The engineer controls the switching threshold of the device by changing Vref_A. Vref_B must be ≥0.8 V higher than Vref_A, tied to EN (for LSF010x only), and pulled up to its supply voltage through a 200-kΩ resistor (for LSF010x only). The LSF devices are best suited for translating signals with fast edge rates, and perform well at frequencies up to 200 MHz (down translation) and 100 MHz (up translation).

Applications for the LSF010x family:

- Simple unidirectional voltage translation
- Bidirectional I^2C translation
- Systems that require multiple levels translated. Example: An LSF0102 can translate from 1.8 to 3.3 V on one channel and 3.3 to 5 V on another channel.

LSF devices work by allowing their FET switches to conduct during the low pulse of an input signal and shutting them off during the high pulse. This allows the pullup resistor on the output to pull up the signal to the user's desired voltage level during the high pulse. Because LSF devices are passive FET switches, they do not have any output current drive strength. The drive strength is determined by external supplies.

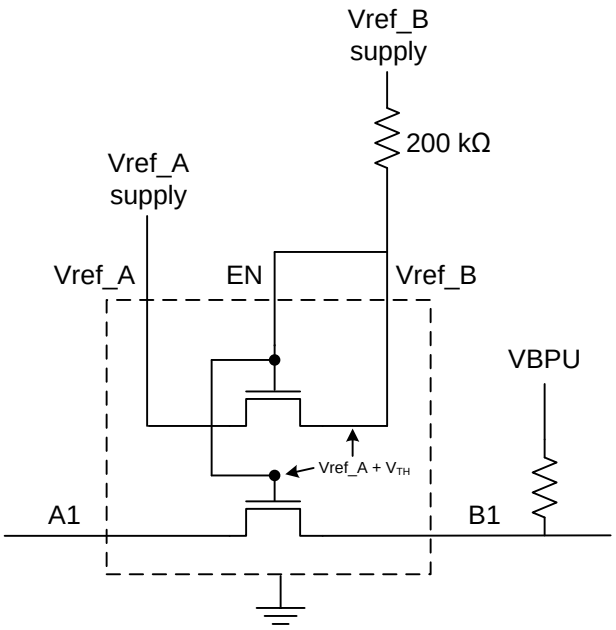


Figure 1. Basics of LSF010x Theory of Operation

Remember that the LSF device acts **as a passive switch when the input signal is below Vref_A – 0.5 V**. In the previous example, suppose the input was a 1-V peak-to-peak square wave centered at 0.5 V. Because that wave never exceeds Vref_A – 0.5 V, it passes through the switch without translation.

The 200-kΩ resistor allows Vref_B to pull the other side of the reference FET to Vref_A + V_{TH}. The EN and Vref_B pins are required to be tied together on the LSF010x. For LSF020x, this 200-kΩ is integrated into the device, and the EN pin can be controlled separately from Vref_B. The connection between the reference FET gates and the channel FET gates allow the gates of every switching FET in the LSF device to have a voltage equal to Vref_A + V_{TH}. When translating down from B to A, this allows the A-side voltage to equal Vref_A + V_{TH} – V_{TH} = Vref_A without any pullups. The reason this is possible is because V_{GS} must exceed V_{TH} for N-channel MOSFET devices to produce an output. They are said to produce a strong 0 and a weak 1. The presence of output voltage without pullups demonstrates the weak 1. During the weak 1 condition, TI recommends only high-impedance loads because very small amounts of current will cause the output voltage to drop significantly. Pullups to Vref_A are not required but allow heavier loads on the low side and help with signal integrity issues that may arise. Pullups on the low side (typically A-side) are only required if translating down to a voltage different than Vref_A.

2 Generic Translation Application Using the LSF0101

Designers can test this example using the LSF010xEVM-001 (see EVM tool page).

In this example, the goal is to translate a 1.8-V square wave to a 3.3-V square wave.

Considerations:

- When the input voltage exceeds Vref_A – 0.5 V, the FET turns off and the pullup resistor on the B-side determines the output voltage. Therefore, the designer needs to pull up the B-side to 3.3 V.
- The FET begins to turn off when the input voltage exceeds Vref_A – 0.5 V. As discussed earlier, the FET should be on during the input low pulse and off during the input high pulse. Therefore, set Vref_A to 1.8 V.

Figure 2 shows the schematic for our application using the LSF0101. The B-side pullup resistors should be sized according to signal frequency and current limits. In this example, because Vref_B and our pullup voltage are both 3.3 V, the designer could have tied VBPU to the supply of Vref_B. To translate to 4 V instead, the designer could pull VBPU to 4 V.

Figure 3 shows the input and output voltages of a low-frequency square wave translated by the LSF0101.

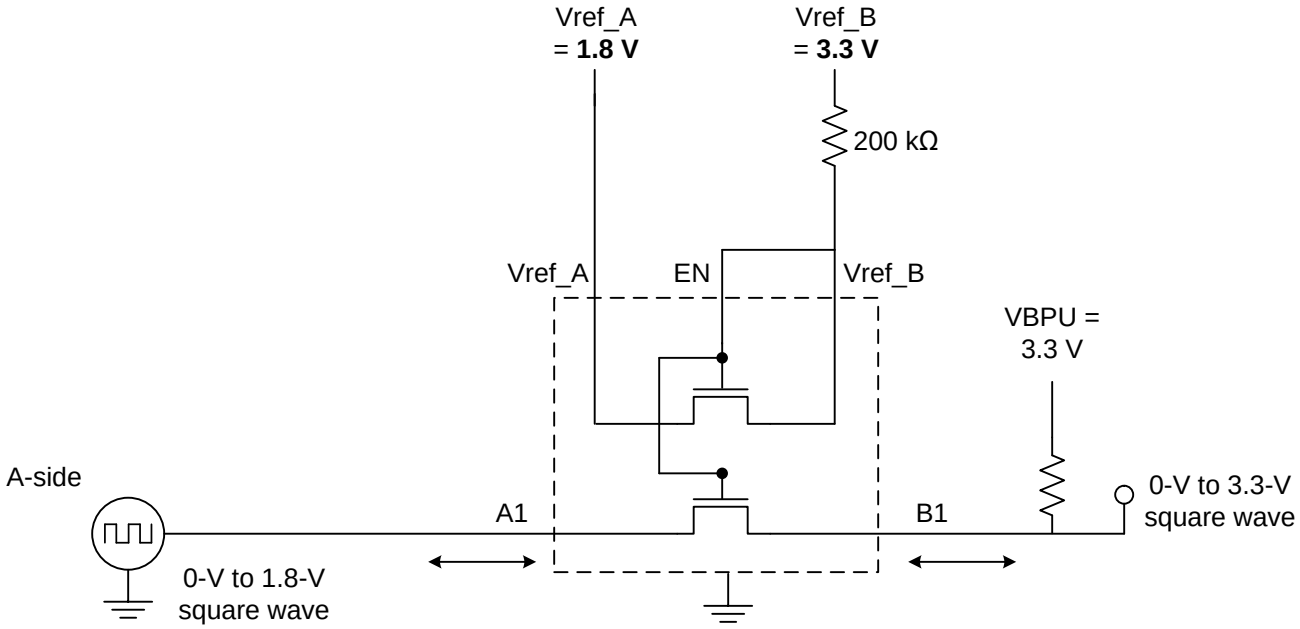
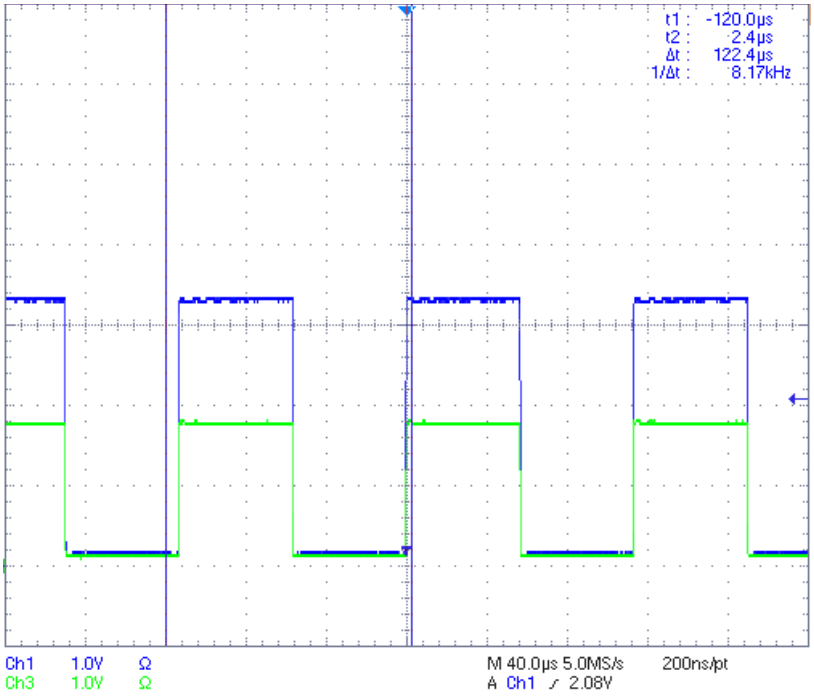


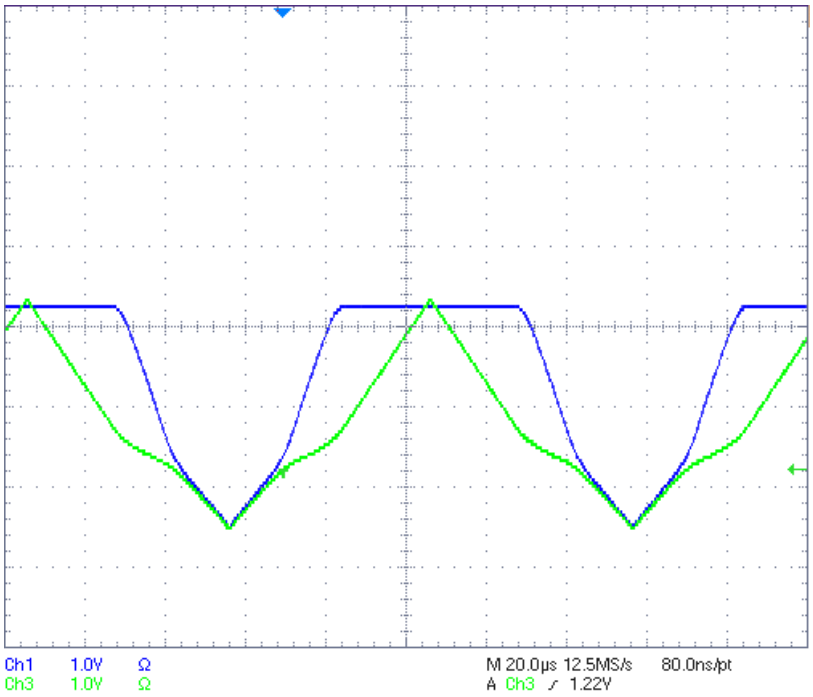
Figure 2. LSF0101 Translation Example Schematic



A CH1 (blue) = B1 output

B CH3 (green) = A1 input

Figure 3. Translation from 1.8 to 3.3 V



A CH1 (blue) = Output

B CH3 (green) = Triangle wave input

Figure 4. Behavior Across Input Voltage With Vref_A = 1.8 V

Figure 4 shows the behavior across input voltage when Vref_A = 1.8 V. Notice that the output starts to rise (FET starts switching off) when the input reaches Vref_A - 0.5 V. This waveform is not a typical input signal for the LSF device. Instead, it illustrates the switching behavior of the LSF across the input voltage range. The waveform shows both states of the LSF device on the same graph: the low-impedance mode during a low input pulse, and the high-impedance mode during a high pulse with the pullup resistor driving the output up to 3.3 V.

3 LSF0101 Translation Application for a PWM Circuit

Some systems require an analog input voltage instead of a digital high or low. In these applications, the driving controller (usually a microcontroller) outputs a pulse-width modulated (PWM) signal with a duty cycle percentage equal to the level of analog signal needed between the high and low states. A filter converts these rectangular pulses into a smooth DC signal at a voltage between the MCU's high and low level output voltages.

In this example, consider a MCU which outputs 0 or 3.3 V, but the filter requires a 5-V PWM signal. The filter smoothes the digital PWM into an analog voltage, and the MCU provides the 3.3-V digital PWM signal. The LSF0101 translates the 3.3-V PWM signal to a 5-V PWM signal for the filter. See Figure 5 for a PWM application schematic.

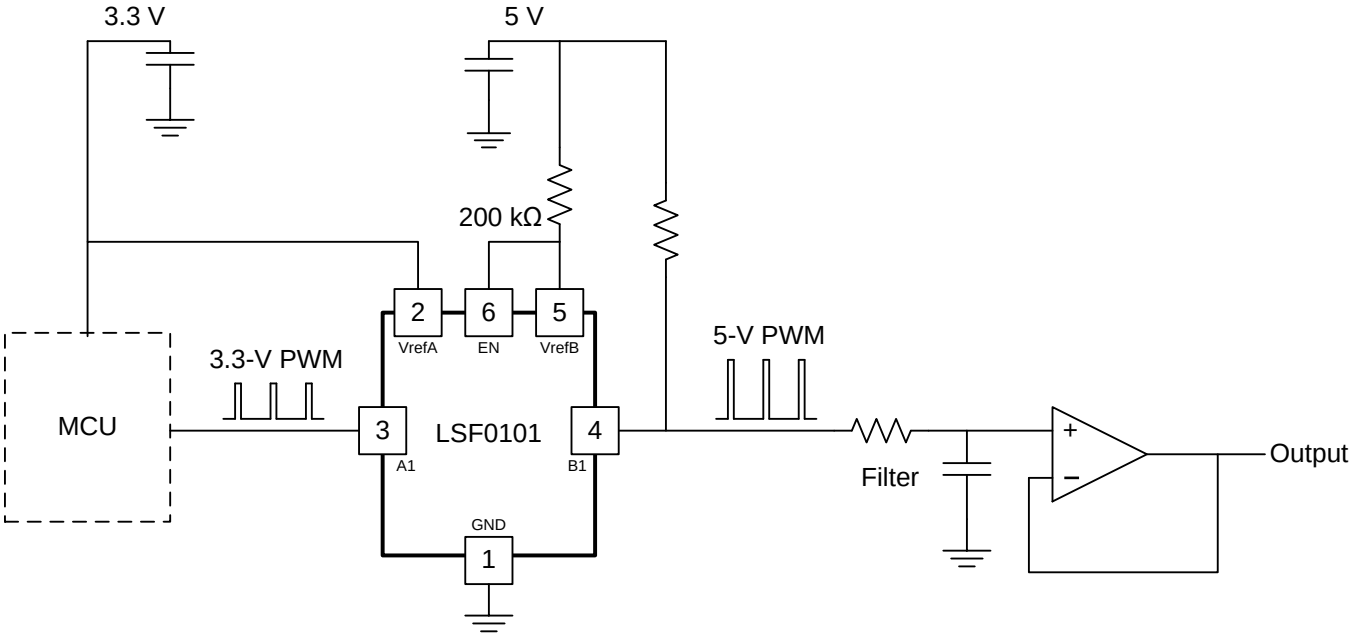


Figure 5. PWM Application With LSF0101

The filter component values can vary depending on the application. If the PWM frequency is very high, the B-side pullup should be small (about 150 Ω) to allow for fast edge rates. Designers should test different B-side pullup values to optimize edge rates, overshoot, and power consumption. To limit the current through the FET to 15 mA, select a pullup resistor equal to $R_{PU} = (V_{PU} – 0.35\ V) / 0.015\ A$. See the LSF data sheet for more guidance on pullup resistor sizing.

NOTE: Consider the V_{OL} of the output driver when designing a PWM circuit. Example: If the V_{OL} is 0.2 V in this case, the 0.2 V passes through the LSF0101 because it is lower than Vref_A – 0.5 V. The input and output are 0.2-V to 3.3-V input to the A-side and a 0.2-V to 5-V output on the B-side. If this V_{OL} is too high for a specific PWM application, consider using a translating logic buffer or CMOS peripheral sink driver instead.

4 Design Differences With LSF020X

The LSF0204 and LSF0204D are 4-channel LSF devices, but they are designed in a slightly different way. The following is a list of application considerations for the LSF020X devices:

- There is an integrated 200-kΩ resistor connected to the Vref_B pin. An external 200 kΩ is not needed.
- The EN pin enables/disables the reference FET's gate connection to the channel FETs. EN is not required to be tied to Vref_B as in the LSF010x. Instead, EN is treated as a logic control input with V_{IH} and V_{IL} referenced to Vref_A. The LSF0204 and LSF0204D have opposite-polarity EN inputs. The EN pin must not be left floating; make sure it is pulled up to Vref_A or pulled down to GND through a resistor that can be driven high or low by an external GPIO.

5 LSF Translation - Frequently Asked Questions

5.1 How does the LSF translate?

The LSF family allows external pullups to translate. The LSF acts as a closed circuit during a low input pulse and an open circuit during a high input pulse. When it is an open circuit, the external pullups take over.

5.2 When are pullups on the A-side and B-side needed?

TI recommends pullups on the low side (typically the A-side) when one of these conditions is met:

- The low side (typically A-side) is used as an output or a bidirectional port, and it is translating to a voltage not equal to Vref_A.
- The low side (typically A-side) is used as an output or a bidirectional port, is translating to Vref_A, and there are signal integrity problems.
- The low side (typically A-side) is used as an input or bidirectional port, and is being driven by an open-drain device.

TI recommends pullups on the high side (typically B-side) when one of these conditions is met:

- The high side (typically B-side) is used as an output or a bidirectional port.
- The high side (typically B-side) is used as an input or bidirectional port, and is being driven by an open-drain device.

Pullups are not required on inputs driven by push-pull devices.

5.3 The data sheet says Vref_B must be 0.8 V higher than Vref_A. How do I translate across a small range, like 1.2 V to 1.8 V?

Set Vref_A to 1.2 V and Vref_B between 2 V and 5.5 V. Add a B-side pullup to 1.8 V. As long as Vref_B ≥ Vref_A + 0.8 V and Vref_B is within the *recommended operating conditions* range, the level of Vref_B does not affect the output signal. Only the B-side pullups affect the output signal level.

5.4 What is the frequency range of the LSF?

The LSF family can translate up at 100 MHz and down at 200 MHz with reasonably good signal integrity. Signal integrity for translation depends on many factors, including line capacitance, output load, and pullup resistor sizes. Generally, smaller pullup resistors allow faster translation, but at the expense of power.

5.5 What happens if the input signal goes below GND?

If the input goes below GND, the FETs turn on and conduct the negative voltage. If the inputs drop below –0.5 V, there is a risk of turning on a clamp diode and drawing excessive current from GND to the input, damaging the device. See the *Absolute Maximum Ratings* in the data sheet for more details.

5.6 What happens if either Vref_A or Vref_B is grounded?

If either Vref_A or Vref_B are grounded, the switch behaves as an open circuit.

5.7 What pullup voltages are allowed on the A-side and B-side?

On either the A-side or B-side, resistors can pull up to any voltage between Vref_A and 5 V. Therefore, it is possible to translate down to the B-side.

Revision B History

Changes from A Revision (February 2015) to B Revision	Page
• Made references to LSF010x, LSF020x, and "LSF" family where appropriate throughout document	1
• Updated *Section 1* with additional information to address down-translation without pullups	2
• Updated pullup resistor requirements and recommendations in *Section 5.2*	6

Revision A History

Changes from Original (December 2014) to A Revision	Page
• Added *Section 4*	6
• Updated *Section 5.2* with additional information	6

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