Design of UVLO for LM27313

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ABSTRACT

This application note describes a novel and economic design of an undervoltage lockout (UVLO) for LM27313. The UVLO is designed to prevent switching current from increasing beyond the maximum rated limit, hence, preventing the device from overheating.

Contents

List of Figures

List of Tables

1 Introduction

The LM 27313 is a boost converter with a fixed switching frequency of 1.6 MHz. The design illustrated in Figure 1 is for a mobile charging application. The charging is being performed with an output current of 500 mA.

V_{IN} = 3 V to 5 V, V_{OUT} = 5V, I_{OUT} = 500 mA
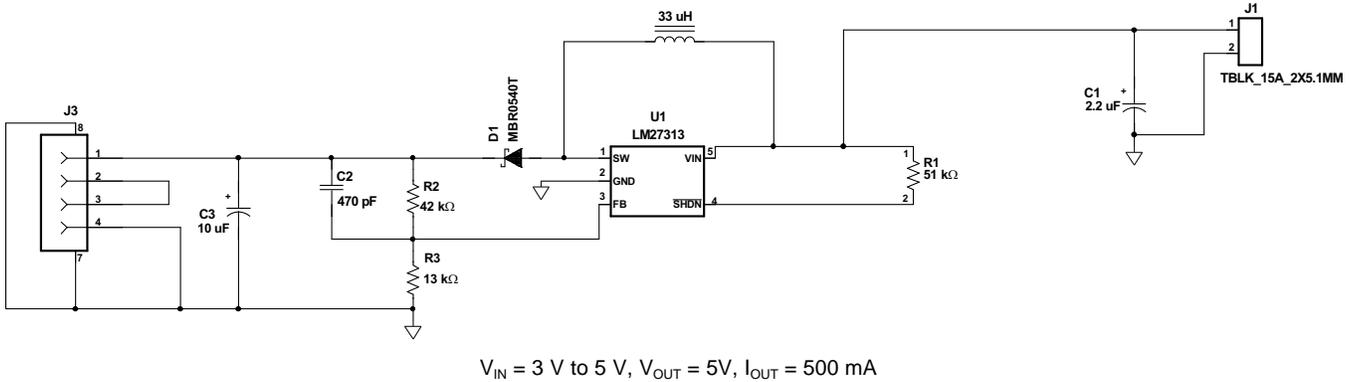
Figure 1. Initial Boost Converter Design

2 Need for Undervoltage Shutdown

Now observations on efficiency for variations in input voltages were made on this design and are listed in Table 1.

Table 1. Design Efficiency

V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	P_{IN}	P_{OUT}	Efficiency
2.989	0.99	4.799	0.398	2.95911	1.910002	64.546502
3.464	0.71	4.915	0.41	2.45944	2.01515	81.935319
3.766	0.62	4.922	0.411	2.33492	2.022942	86.6386
4.025	0.57	4.927	0.411	2.29425	2.024997	88.264008
4.234	0.54	4.931	0.411	2.28636	2.026641	88.640503

From the observations in Table 1, it is evident that the input current increases above 700 mA for an input voltage below 3.5 V. Also, the efficiency of the same reduces rapidly to as low as 64.5% at V_{IN} = 3 V.

This increase in input current exceeds the current limit of the device (1.25 A – peak current) and causes the device to heat up, therefore, the IC must be shut down when the input voltage falls below 3.5 V. This can be achieved by utilizing the characteristics of the shutdown pin of LM27313.

3   Characteristics of the Shutdown Pin

The device's state of operation (ON/OFF) can be decided by the voltage at the shutdown pin (V_{SHDN}).

Table 2 shows its characteristics:

Table 2. Operating State at the Shutdown Pin

V_{SHDN}	Operating State	Units
≤ 0.5	OFF	Volts
≥ 1.5	ON	Volts

Hence, a circuit is to be designed such that the V_{SHDN} ≤ 0.5 V for V_{IN} ≤ 3.5 V and V_{SHDN} > 1.5 V for V_{IN} > 3.5 V.

4   UVLO Circuit

Figure 2 shows a UVLO circuit.
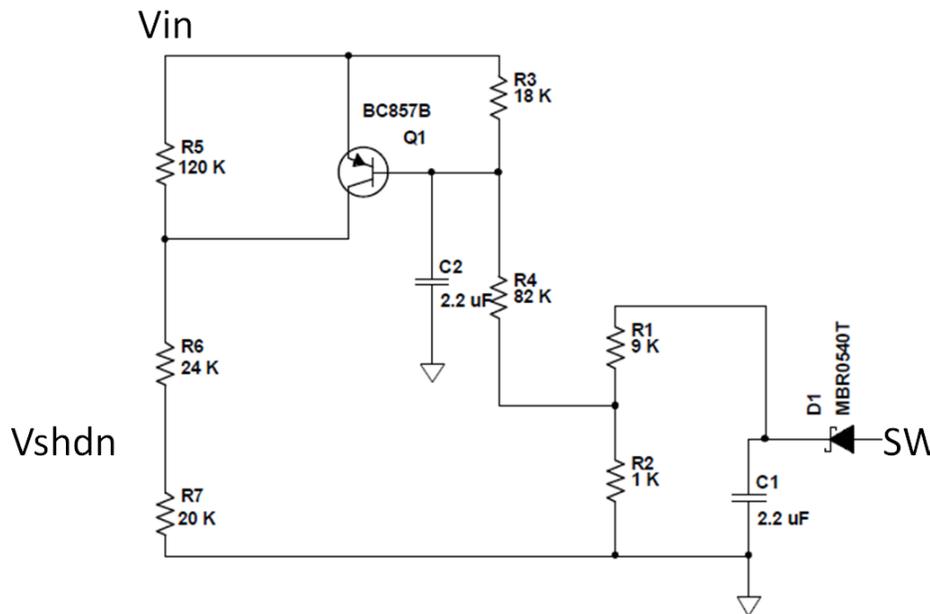
Figure 2. UVLO Circuit

4.1   *Circuit Behavior*

When the voltage across V_{IN} ≥ 3.6 V, the transistor T1 turns on, hence bypassing resistor R5. This causes the voltage at the SHDN pin to go above 1.5 V, turning the IC on. But when V_{IN} ≤ 3.5 V, the device turns OFF.

4.2 Design Procedure

The design procedures are listed in following steps:

1. For the transistor to turn on, $V_{be} \geq 0.6$ V. So, according to the requirement, the voltage at the base of the transistor should be less than 3 V.

2. This only happens if the potential difference across R3 and R4 is greater than 3 V.

3. The voltage divider values are decided with the following equation:

$$0.5 = \frac{5 \times R2}{R1 + R2} \tag{1}$$

4. Based on the potential difference between R3 and R4, the values of R3 and R4 are calculated to be:

$$\frac{3.1 \times R3}{R3 + R4} = 2.9 \tag{2}$$

Figure 3. Final Circuit with UVLO

5 Conclusion

The design of the UVLO allows us to limit the switching current and gives access to a wider range of applications in which the LM27313 can be used. Furthermore, this method can be used with other similar devices, some of which are listed here:

- LM2735
- TPS61170
- LMR62014
- LMR64010
- LMR62421
- TPS61260
- TPS61261
- LM3310
- LM4510

6 References

1. LM27313 datasheet (SNVS487)

Revision History

Changes from Original (April 2014) to A Revision   **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

Changes from A Revision (April 2014) to B Revision   **Page**

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