Using the TPS3700 as a Negative Rail Over- and Undervoltage Detector

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ABSTRACT

The TPS3700 is a wide voltage window comparator that can be used in overvoltage (OV) and undervoltage (UV) detection. This application note describes a simple approach to use the TPS3700 for negative voltage monitoring applications such as the negative rail on op amps, DACs, ADCs, and other high-precision analog circuitry that may need UV or OV protection.

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1 Negative UV, OV Detection Solution

Figure 1 shows a typical circuit for monitoring a negative rail. Resistors R1, R2, and R3 are calculated to set the overvoltage and undervoltage threshold. R_{p1a}, R_{p1b}, R_{p2a}, and R_{p2b} are used with D1 and D2 to clamp the logic level LOW to approximately 0 V and provide a proper logic level HIGH to the VPU voltage.

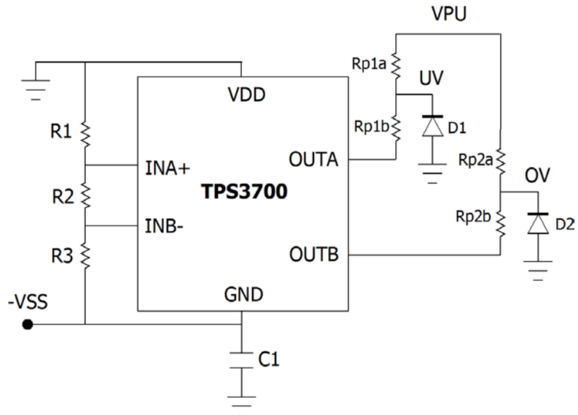

Figure 1. Monitoring a Negative Voltage Rail Using the TPS3700

2 Setting the OV, UV Thresholds using R1, R2, and R3

This section discusses the design calculations for setting the OV and UV thresholds. The TPS3700 Resistor Divider Calculator (SLUC425) in the TPS3700 product page is also a helpful tool in calculating R1, R2, and R3.

$$R3(\Omega) = \frac{V_{thp}}{|I_{Divider}|} \times \frac{|V_{Mon}|}{|V_{OV}|} \quad (1)$$

Where:

V_{thp} = Positive-going input threshold voltage in volts (0.4 V typical).
V_{Mon} = Nominal-sensed rail voltage in volts.
$I_{Divider}$ = Current through the resistor divider in amperes.
V_{OV} = Overvoltage threshold for OUTB triggering LOW in volts.

$$R2(\Omega) = \left(\frac{V_{thn}}{|I_{Divider}|} \times \frac{|V_{Mon}|}{|V_{UV}|} \right) - R3(actual) \quad (2)$$

Where:

V_{thn} = Negative-going input threshold voltage in volts (0.3945 V typical).
V_{UV} = Undervoltage threshold for OUTA triggering LOW in volts.

$$R1(\Omega) = \left(\frac{|V_{Mon}|}{|I_{Divider}|} \right) - R2(actual) - R3(actual) \quad (3)$$

3 Setting the Appropriate Output Logic Levels

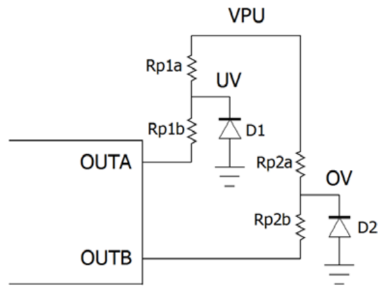

Figure 2. Output Circuit Configuration

Figure 2 shows the output circuit used to set the appropriate output logic levels during an overvoltage and undervoltage condition. During an undervoltage or overvoltage condition, OUTA/OUTB is asserted to –VSS and D1/D2 turns ON to its forward voltage Vf1/Vf2. D1/D2 and Rp1b/Rp2b should be chosen such that their forward voltage and sinking current is small enough to ensure a logic level LOW to the load the signal it is driving. Note the datasheet characterizes this device with I_{OL} = 5 mA (max) of sinking current. I_{OL} can be higher at the expense of a higher V_{OL} voltage.

$$Rpxb(\Omega) = \frac{|-V_{SS}| - |V_{fx}|}{I_{OL}} \tag{4}$$

When –VSS is at its nominal voltage, OUTA and OUTB are released, Dx is OFF, and OV, UV is pulled up to VPU voltage. VPU must be chosen as shown in Equation 5 such that the +20-V absolute maximum on V_{OUTA} and V_{OUTB} is not violated.

$$V_{PU}(Max) = +20\ V + (-V_{SS}) \tag{5}$$

The pullup resistor Rpxa is chosen depending on the desired minimum V_{OH} and rated output leakage current. Leakage current for the TPS3700 is rated for 300 nA (max). Equation 6 does not include possible current paths to and from the load.

$$Rpxa(\Omega) = \frac{V_{PU} - V_{OH}}{I_{Leakage}} \tag{6}$$

D1 and D2 should be chosen such that the operating conditions do not exceed what it is rated for. That is:

$V_f \leq V_{OL}$ (maximum)
$V_r > V_{PU}$
$I_o > I_{OL}$

3.1 Wired-OR Configuration

Because the TPS3700 utilizes open-drain outputs, it can be arranged in a wired-OR configuration to trigger an output LOW when there is either an OV or UV condition. Figure 3 shows this configuration. With this circuit, Equation 4 and Equation 5 still hold.

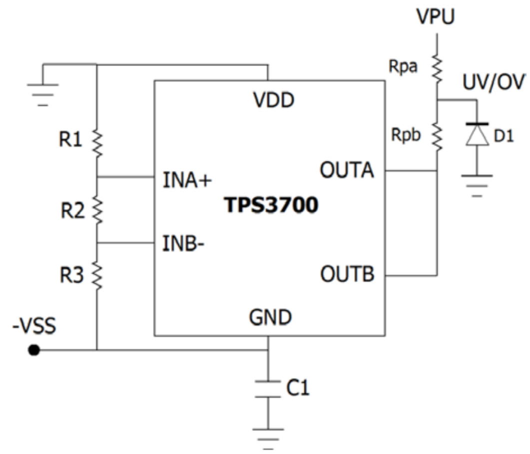

Figure 3. Wired-OR Output Configuration

4 Design Example

The following design example uses the TPS3700 under the following conditions for monitoring a –12-V rail and triggers a reset when the rail falls below 10% or rises above 10% of –12 V.

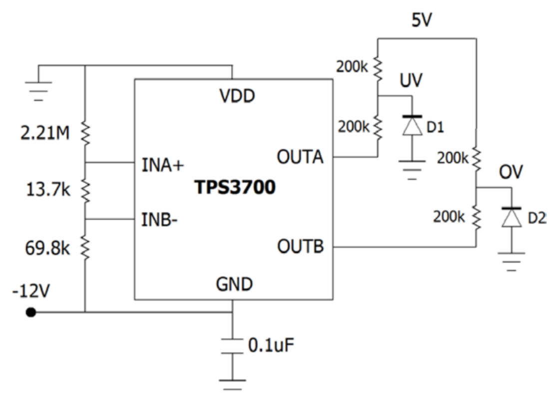

Figure 4. TPS3700 Negative Monitoring Design Example

As shown in Figure 5 and Figure 6, OUTA will trigger LOW during a –10% drop (–10.8 V) while OUTB will trigger LOW during a +10% rise (–13.2 V). In between this window, the outputs are pulled up to VPU.
Yellow: VSS-5V/div
Pink: UV-5V/div
Blue: OV-5V/div

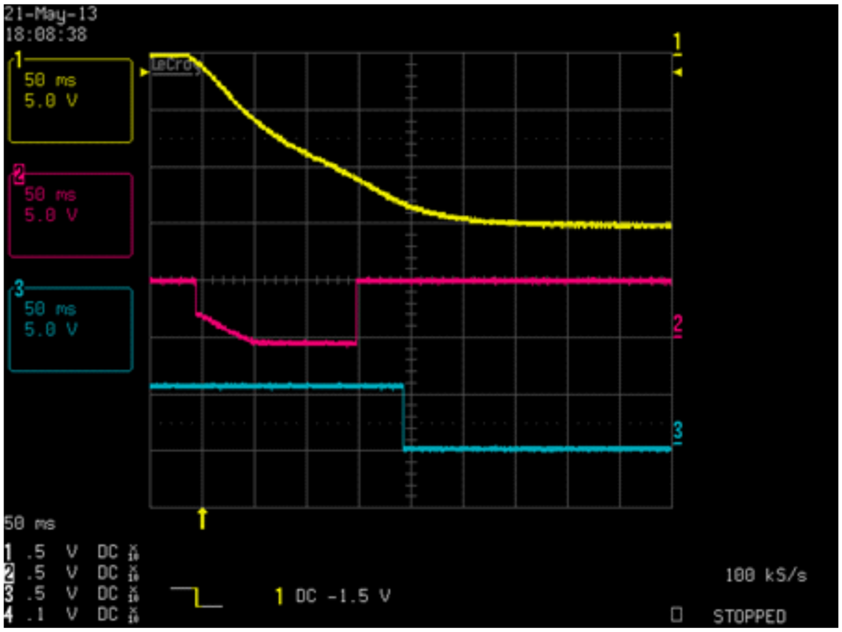

Figure 5. OUTA and OUTB Response for VDD Voltage Rising

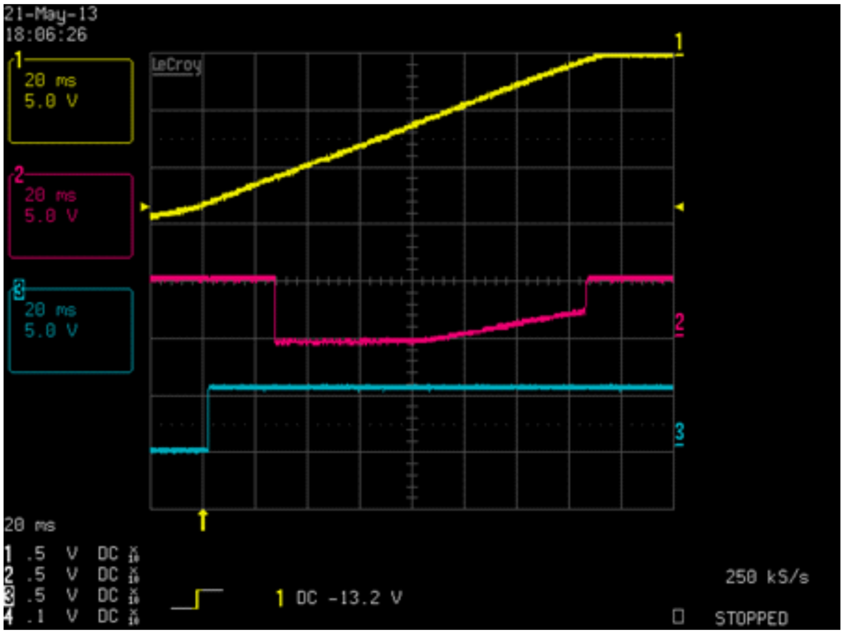

Figure 6. OUTA and OUTB Response for VDD Voltage Falling

5 Conclusion

This application report has demonstrated simple circuit and design considerations for using the TPS3700 to monitor negative voltage rails and output the appropriate logic levels.

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