Creating an Inverting Power Supply Using a Synchronous Step-Down Regulator

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ABSTRACT

Some applications require negative output voltage to be generated from a positive input voltage. This application report presents a solution for creating an inverting power supply using the TPS54061 synchronous buck converter in an inverting buck-boost topology. This device features a wide input range of 60V and synchronous rectifier diode emulation for improved efficiency at light loads.

The solution schematic is provided along with component selection criteria and equations to scale the design as needed. Also included are captured waveforms from the TPS54061 design example. This design procedure is also applicable to other synchronous step down peak current mode control regulators.

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1   Description of Application

This application report presents the design procedure for creating an inverting power supply using a synchronous step-down regulator. A negative output voltage is generated from a positive input voltage. Applications that may require a negative output voltage from a positive input voltage include double-ended sensors and audio amplifiers to name a few.

A synchronous topology has certain advantages over a nonsynchronous topology including higher efficiency at low voltages and a smaller solution size. The synchronous regulator uses an internal rectifying MOSFET instead of an external rectifying Schottky diode reducing the solution size. The TPS54061 features a wide input voltage range of 60V to withstand input voltage transients and supply negative output voltages of -5V, -12V, -24V or more. Unlike typical synchronous regulators, the TPS54061 also features synchronous rectifier diode emulation allowing it to enter DCM (discontinuous conduction mode) at light loads improving efficiency.

Using a synchronous buck regulator in an inverting buck-boost topology simply requires redefining the output voltage (Vout) and device ground (GND) connections. In a standard buck topology Vout is connected to the inductor and the return is connected to GND shown in Figure 1.
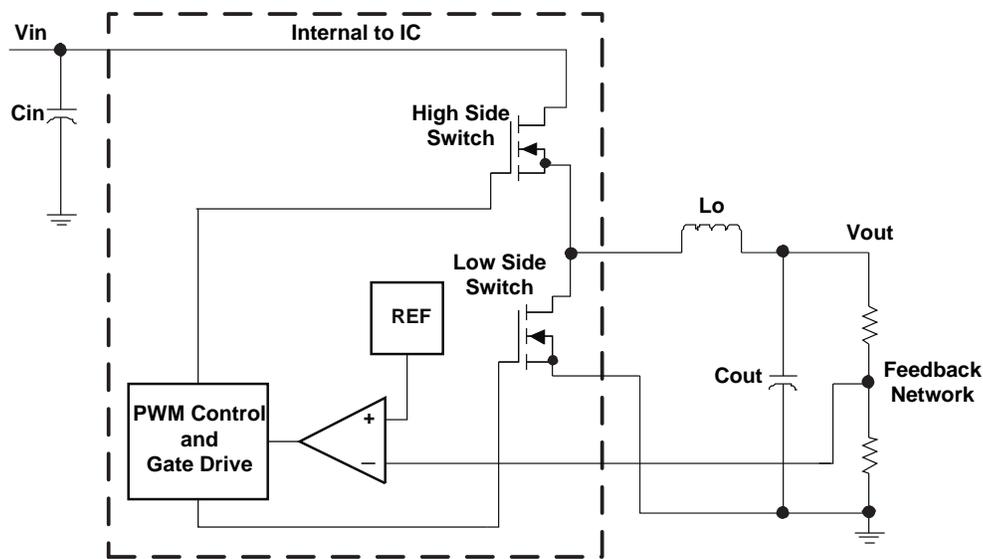

Figure 1. Buck Topology

In the inverting buck-boost GND is connected to the inductor and the return is connected to Vout shown in Figure 2.
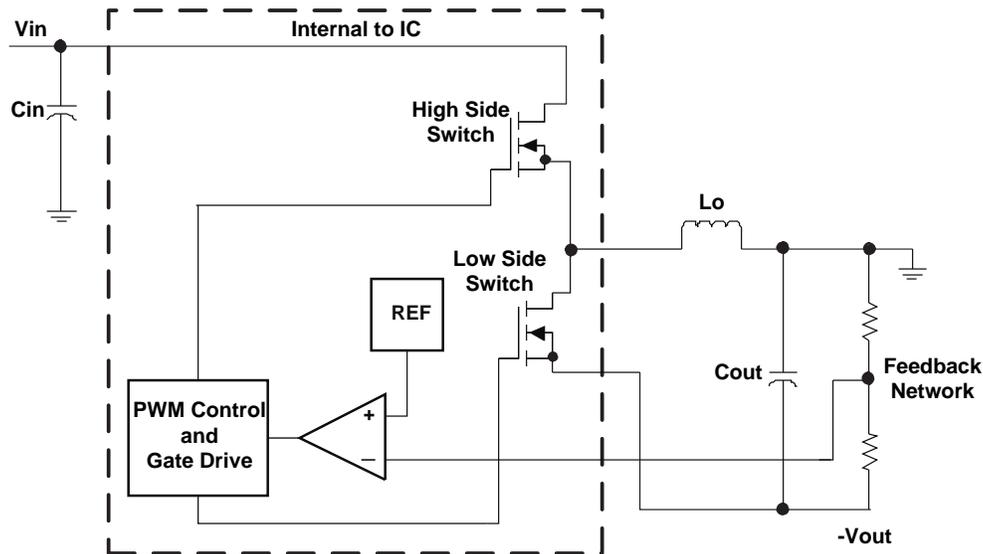

Figure 2. Inverting Buck-Boost Topology

The electrical requirements of the design example are listed in Table 1.

Table 1. Inverting Power Supply Requirements

VARIABLE	DESCRIPTION	VALUE / RANGE
Vin	Input Voltage	24 V nominal 12 V to 48 V
Vout	Output Voltage	–12 V
ΔVout	Output Voltage Ripple	<0.5%
Iout	Output Current	100 mA
$f$sw	Switching Frequency	400 kHz

2 Design Considerations

Some important requirements which must be considered for the application are listed in Table 2. To power up the supply, the input voltage must be greater than the minimum required voltage for the device (4.7V). After the output is in regulation the device is referenced to the negative output and a much lower input voltage is needed to turn the supply off. Turn off typically occurs when the peak inductor current limit is exceeded and the output voltage approaches 0V. The maximum allowable output voltage is limited by the maximum operating input voltage of the TPS54061 (60V). The voltage difference between Vin and Vout must never exceed the Vdev(max). Because the MOSFETs are internal to the IC, the maximum load current will depend on the minimum peak current limit of the internal switches (Icl) which limits the peak current of the inductor (ILpeak).

Table 2. Electrical Characteristics for the Inverting Power Supply

Inverting Power Supply Restrictions		Synchronous Device Used	TPS54061
Vin(min)	>	Vdev(min)	4.7 V
Vin(max) - Vout	<	Vdev(max)	60 V
ILpeak(min)	<	Icl(min)	250 mA

3   Design Procedure
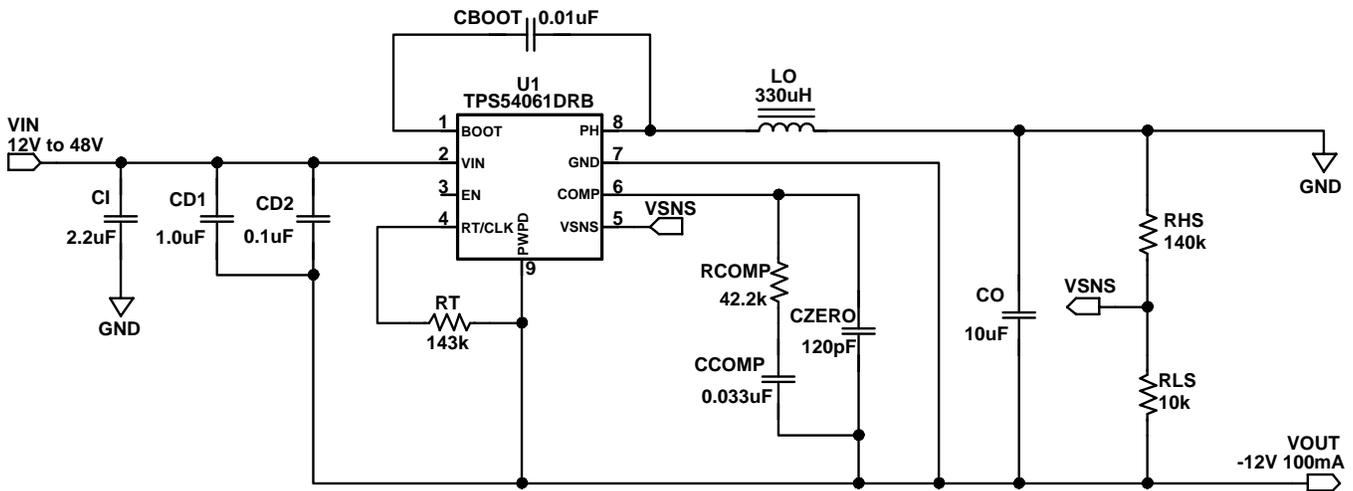
3.1   Schematic

Figure 3. Inverting Power Supply Schematic

3.2   Maximum Input Voltage and Output Voltage

The difference in the maximum input voltage, Vin(max), and the output voltage, Vout, must not exceed the maximum operating device voltage of the regulator. For the TPS54061, the maximum operating device voltage, Vdev(max), is 60V.

$$Vin(max) \leq Vdev(max) + Vout \tag{1}$$

$$RHS = RLS \times \left(\frac{-Vout}{Vref} - 1 \right) \tag{2}$$

The Vout for the sample design is –12V so using Equation 1, the input voltage for the power supply can be as high as 48V which supports the 48-V maximum input requirement in Table 1. Equation 2 determines RHS for the desired output voltage. Assuming RLS is 10 kΩ and Vref is 0.8V for the TPS54061, RHS equals 140 kΩ (140-kΩ standard value).

3.3   Minimum Input Voltage

The operating input voltage, Vin(min) of the power supply must be greater than the minimum device voltage, Vdev(min). For TPS54061, the Vdev(min) is 4.7V. The minimum input voltage requirement for the power supply is 12V, thus, satisfying Equation 3.

$$Vin(min) \geq Vdev(min) \tag{3}$$

3.4   Duty Cycle

The steady-state duty cycle for the inverting power supply is shown in Equation 4, neglecting the losses of the power switching and inductor. The output voltage, Vout, is negative and the input voltage, Vin, is positive, yielding a positive result for Equation 4.

$$D = \frac{-Vout}{Vin - Vout} \tag{4}$$

The maximum duty cycle, Dmax, is calculated using the minimum input voltage, Vin(min), for the input voltage Vin in Equation 4. Assuming 12V for Vin(min) and Vout of -12V, the maximum duty cycle, Dmax, is 0.50. Similarly, Dmin is evaluated by using maximum input voltage, Vin(max) of 48V for Vin, is calculated to be 0.20.

3.5 Output Current

To estimate whether the selected switching regulator is capable of delivering the required output current, use Equation 5. The user must know the device's (TPS54061) minimum peak current limit, Icl(min), maximum duty cycle, Dmax, and estimate the inductor ripple current value, ILripple. Assuming the minimum current limit is 250mA and the ILripple is 50% of the minimum current limit (ILripple = 0.5 x Icl(min)), the estimated maximum output current supported by the TPS54061 is 100mA which satisfies the design requirements of Table 1. The inductor current ripple impacts the maximum output current. Higher current ripple produces lower output current but allows the use of smaller inductors. Also note the maximum output current depends on the full load efficiency in the final design.

$$\text{Iout (max)} \leq \left(\text{Icl(min)} - \frac{\text{ILripple}}{2} \right) \times \left(1 - \text{Dmax} \right)$$

(5)

3.6 Operating Frequency

Choosing the switching frequency for the regulator is a tradeoff between higher efficiency versus smaller size. Higher switching frequencies may produce a smaller solution size using lower valued inductors and smaller output capacitors, compared to a power supply than switches at a lower frequency. However, higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance.

In this design example, a moderate switching frequency of 400 kHz is selected to achieve both a relatively small solution size and high-efficiency operation. The switching frequency is set with a resistor, RT, from the RT/CLK pin to the GND of the TPS54061 device. Using Equation 6, the frequency set resistor is 142 kΩ (143-kΩ standard value).

$$R_T(k\Omega) = \frac{71657}{f_{SW}(kHz)^{1.039}}$$

(6)

The switching frequency must be less than the maximum switching frequency supported by the device which is 1100kHz for the TPS54061. The maximum switching frequency is also limited by the minimum controllable on-time required to support the minimum duty cycle (Dmin). The maximum switching frequency to avoid pulse skipping at Dmin is calculated using Equation 7 to be 1700kHz.

$$f_{SW}(\text{max skip}) = \left(\frac{1}{t_{ON}} \right) \times \left(\frac{-Vout + Rds_{LS} \times Iout + Rdc \times Iout}{Vin(max) - Iout \times Rds_{HS} + Iout \times Rds_{LS} - Vout} \right)$$

(7)

Where:

- T_{ON} = minimum controllable on time, 120ns
- Rds_{HS} = typical high side MOSFET on resistance, 1.5Ω
- Rds_{LS} = typical low side MOSFET on resistance, 0.8Ω
- Rdc = DCR of inductor, 1.15Ω

The TPS54061 also features a frequency shift to avoid over current runaway during an output short circuit. The maximum allowable switching frequency for short circuit protection is calculated using Equation 8 to be 659kHz.

$$f_{SW}(\text{max shift}) = \left(\frac{fdiv}{t_{ON}} \right) \times \left(\frac{-Vosc + Rds_{LS} \times Iout(cl) + Rdc \times Iout(cl)}{Vin(max) - Iout(cl) \times Rds_{HS} + Iout(cl) \times Rds_{LS} - Vosc} \right)$$

(8)

Where:

- Vosc = output voltage during output short circuit, -0.1V
- fdiv = frequency division term, 8 when vosc is less than 25% of the regulation Vout
- Iout(cl) = maximum output current at current limit with maximum input voltage calculated with

Equation 5, 188mA

See the TPS54061 data sheet for more details on frequency shift protection.

3.7 Inductor

To determine the inductor value, calculate the average inductor current, ILavg, at the maximum output current and minimum input voltage using Equation 9. Assuming maximum output current, Iout is 100mA and using maximum duty cycle Dmax, ILavg is 200mA.

The inductor value is calculated with Equation 10 assuming a ripple current that is 50% of the average inductor current. Using the Dmin to calculate the minimum inductance value gives a larger inductance value. Assuming Vin(max) of 48V, Iout of 100mA, and a $f$sw of 400kHz, the Lo is calculated as 384µH. The nearest standard inductor 330µH is chosen for Lo. The inductor saturation current must be greater than the 223mA peak current calculated in Equation 11 and ILpeak should be less than Icl(min) of the TPS54061. Conservative designs use the Icl(typ) as the inductor saturation current to account for any transients. Icl(typ) of the TPS54061 is 350mA. The inductor rms current rating must be greater than 127mA calculated in Equation 12. The selected inductor is the WE 744777233 with 450mA saturation current rating, 390mA rms current rating and 1.15Ω DCR.

$$\text{ILavg} = \frac{\text{Iout}}{1 - \text{Dmax}} \tag{9}$$

$$\text{Lo} = \frac{\text{Vin(max)} \times \text{Dmin}}{(f\text{sw} \times \text{ILavg} \times 0.5)} \tag{10}$$

$$\text{ILpeak} = \frac{\text{Iout}}{1 - \text{Dmax}} + \frac{\text{Vin(min)} \times \text{Dmax}}{2 \times f\text{sw} \times \text{Lo}} \tag{11}$$

$$\text{ILrms} = \sqrt{\left(\frac{\text{Iout}}{1 - \text{D}}\right)^2 + \frac{1}{12} \times \left(\frac{\text{Vin} \times \text{D}}{f\text{sw} \times \text{Lo}}\right)^2} \tag{12}$$

3.8 Output Capacitor

The output capacitor must supply the output current when the high-side switch is on and the inductor current flows from Vin to GND. Use the minimum input voltage to calculate the output capacitance needed which corresponds to the maximum duty cycle and peak-to-peak current in the output capacitor. Using the 0.5% voltage ripple specification in Equation 13, Co(min) is calculated to be 2.1µF. Assuming the 0.5% voltage ripple and maximum duty cycle, the Rc, equivalent series resistance must be less than 269mΩ from Equation 14. The rms current for the output capacitor is 100mA from Equation 15. A single 10µF/25 V X5R is used for the output capacitor because of the low ESR and size. The output capacitor is derated by 20% because of DC bias.

$$\text{Co (min)} \geq \frac{\text{Iout(max)} \times \text{Dmax}}{f\text{sw} \times \Delta\text{Vout}} \tag{13}$$

$$\text{Rc} \leq \frac{\Delta\text{Vout}}{\dfrac{\text{Iout}}{1 - \text{Dmax}} + \dfrac{\text{Vin(min)} \times \text{Dmax}}{2 \times f\text{sw} \times \text{Lo}}} \tag{14}$$

$$\text{Icorms} = \text{Iout (max)} \times \sqrt{\frac{\text{Dmax}}{1 - \text{Dmax}}} \tag{15}$$

3.9 Power Dissipation in Package

The power dissipation in the TPS54061 is dominated by the conduction losses and switching losses of the power switches and must not exceed the limitations of the package. The conduction and switching losses are calculated using Equation 16. The conduction losses are a function of the duty cycle, D, inductor rms current, ILrms, and MOSFET on resistance, Rds$_{HS}$ and Rds$_{LS}$. The switching losses are a function of the rise (tr) and fall times (tf), switching frequency, output current, and input and output voltage. Pdevice is calculated to be 0.661 W assuming a tr and tf of 25 ns.

$$Pdevice = D \times Rds_{HS} \times ILrms^2 + (1-D) \times ILrms^2 \times Rds_{LS} + \frac{1}{2} \times (Vin - Vout) \times \left(\frac{Iout}{1-D}\right) \times (tr + tf) \times f_{SW} \tag{16}$$

3.10 Input Capacitors

The TPS54061 needs closely located 1µF ceramic bypass capacitor connected between the Vin and GND pins of the device which is connected to Vout. Because the device GND is the power supply output voltage, the voltage rating of the capacitor must be greater than the difference in the maximum input and output voltage of the power supply. A single 1µF high is used with an additional 0.1µF for added high frequency bypass (CD1 and CD2).

In some applications an additional bulk input capacitance is needed between the Vin and the system ground to limit voltage ripple on the input supply. Equation 17 through Equation 20 are used to estimate the capacitance, maximum ESR, and current rating for the input capacitor, Ci, limiting the ripple to 10% of Vin(min). Using Equation 17, the estimated average input current is 100mA. Using Equation 18 and Equation 19, the minimum required input capacitance is 2.1µF and the maximum ESR is 1.20Ω. Using Equation 20, the input capacitor needs at least 112-mA current rating. A single 2.2µF/100 V X7R is used for the input capacitor because of the low ESR and size.

$$Iin\,(avg) = \frac{Iout \times Dmax}{(1 - Dmax)} \tag{17}$$

$$Ci = \frac{Iin(avg)}{f\text{sw} \times 0.01 \times Vin\,(min)} \tag{18}$$

$$ESRci \le \frac{0.01 \times Vin\,(min)}{Iin\,(avg)} \tag{19}$$

$$Icirms = \sqrt{\left(\left(ILpeak - Iin(avg)\right)^2 + \frac{\left(\frac{Vin(min) \times Dmax}{Lo \times f\text{sw}}\right)^2}{12}\right) \times Dmax + Iin(avg)^2 \times (1 - Dmax)} \tag{20}$$

3.11 Slow-Start Time

The TPS54061 has an internally fixed 2.36 ms typical slow-start time eliminating the need for an external capacitor.

3.12 Frequency Response of the Inverting Regulator

A buck-boost regulator to generate a negative output voltage has a different feedback loop characteristic than a buck power supply. Therefore, a different design method is needed. The inverting power supply transfer function has two zeroes and a pole. Equation 21 is a simplified transfer function of an inverting power supply. The ESR zero, $f z1$, is the same as in a buck regulator (Equation 22) and is a function of the output capacitor and its ESR. The other zero is a right half plane zero, $f z2$. The frequency response of the $f z2$ results in increasing gain and decreasing phase. The $f z2$ frequency is a function of the duty cycle, output current, and the inductor. Equation 23 calculates the minimum frequency of the $f z2$ which is used to determine the crossover frequency. The dominant pole, $f p1$, is a function of the load current, output capacitor, and duty cycle (Equation 24). Kbb is the dc gain and is used to calculate the frequency compensation components. The gmps variable is the transconductance of the power stage, which is 1 A/V for the TPS54061.

The $f z1$ is calculated to be 3980 kHz. The output capacitor is derated by 20% because of the dc bias and the ESR is assumed to be 5 mΩ. The $f z2$ is calculated to be 28.9 kHz assuming resistance of the inductor (Rdc) is 1.15Ω. The $f p1$ is estimated to be 199 Hz assuming the maximum duty cycle. Kbb is calculated as 40.0 V/V using Equation 25, assuming minimum input voltage.

$$T(s) = Kbb \times \frac{\left(1 + \frac{s}{2 \times \pi \times fz1}\right) \times \left(1 + \frac{s}{2 \times \pi \times fz2}\right)}{\left(1 + \frac{s}{2 \times \pi \times fpl}\right)}$$

(21)

$$fz1 = \frac{1}{(Rc \times Co \times 2 \times \pi)}$$

(22)

$$fz2 = \frac{(1 - Dmax)^2 \times \left(\frac{-Vout}{Iout}\right) + Rdc \times \left((1 - Dmax) - Dmax\right)}{Dmax \times Lo \times 2 \times \pi}$$

(23)

$$fp1 = \frac{1 + D}{\left(\left(-\frac{Vout}{Iout}\right) \times Co \times 2 \times \pi\right)}$$

(24)

$$Kbb = \frac{Vin \times \left(-\frac{Vout}{Iout}\right)}{\left(Vin + 2 \times (-Vout)\right)} \times gmps$$

(25)

The crossover of the power supply must be set between the $fp1$ and 1/3 of $fz2$ frequencies. It is recommended to start with the crossover frequency, fco, given by Equation 26. The fco is estimated to be 2.4kHz.

$$fco = (fp1 \times fz2)^{0.5}$$

(26)

The compensation resistor, Rcomp, needed to set the compensation gain at the fco frequency is calculated using Equation 27. The Vref is 0.8 V and gmea is 108 µA/V for the TPS54061.

$$Rcomp = \left(\frac{fco}{Kbb \times fp1}\right) \times \left(\frac{-Vout}{Vref \times gmea}\right)$$

(27)

Rcomp is calculated using Equation 27 to be 41.9 kΩ. Use the nearest standard value of 42.2-kΩ. The compensation zero is set to ½ of the dominant pole, $fp1$. Using Equation 28 to calculate the compensation zero capacitor, Czero, gives 0.38µF. Use the nearest standard value which is 0.33µF. The compensation pole is set to equal the RHP zero, $fz2$. Use Equation 29, to calculate the frequency compensation pole, Cpole, which gives 130pF. The nearest standard value is 120pF.

$$Czero = \frac{1}{\left(\frac{fp1}{2}\right) \times 2\pi \times Rcomp}$$

(28)

$$Cpole = \frac{1}{fz2 \times 2\pi \times Rcomp}$$

(29)

3.13 *Synchronizing to an External Clock and Adjustable UVLO*

The TPS54061 has a CLK pin that can be used to synchronize the switching frequency to an external system clock. A level shift circuit must be used to translate a system ground reference clock signal to the device's ground (Vout). For the same reason a similar circuit is needed to interface with the EN pin for on/off control or for adjustable Vin UVLO.

4   Evaluation Results

Figure 4 to Figure 17 show the experimental test results of the Figure 3 design. The discontinues conduction mode (DCM) to continuous conduction mode (CCM) boundary is at an output current of 12mA. The pulse skipping boundary is at an output current of 0.2mA. The input current at no load at 24V input voltage is 1.08mA.
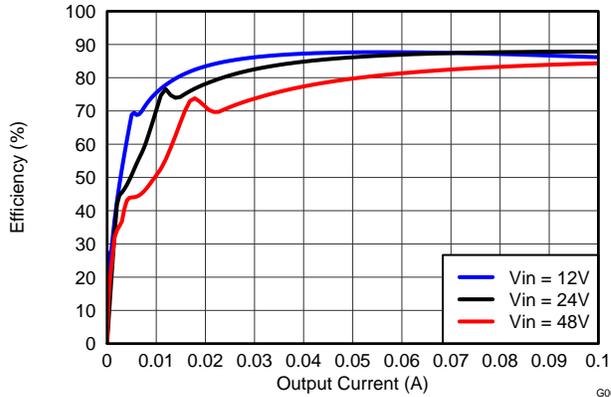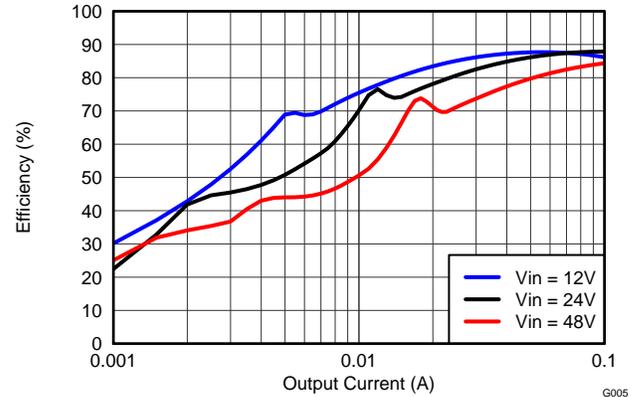
Figure 4. Efficiency
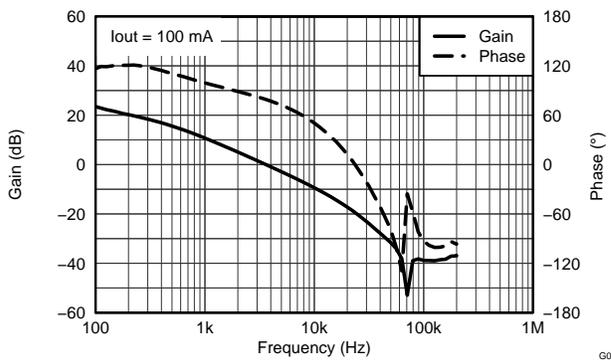

Figure 5. Light Load Efficiency
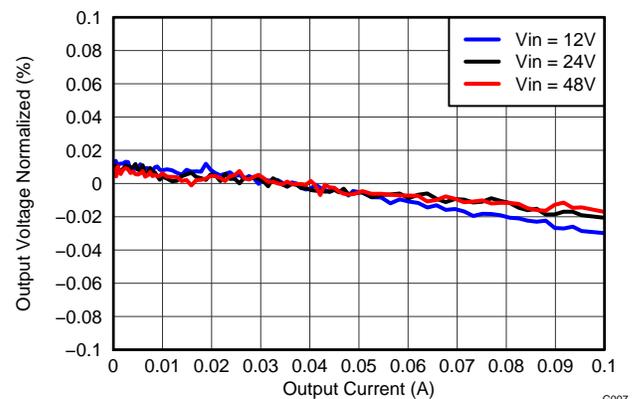

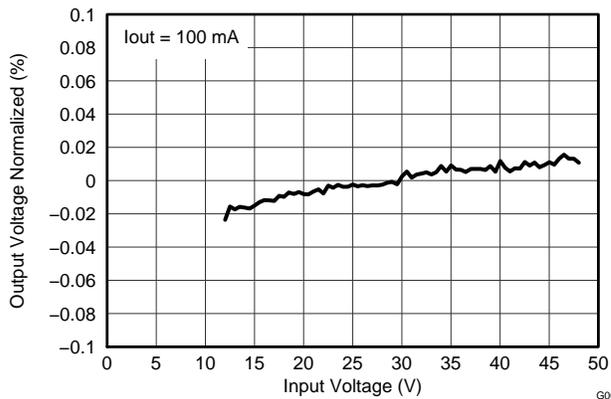**Figure 6. Loop Response**

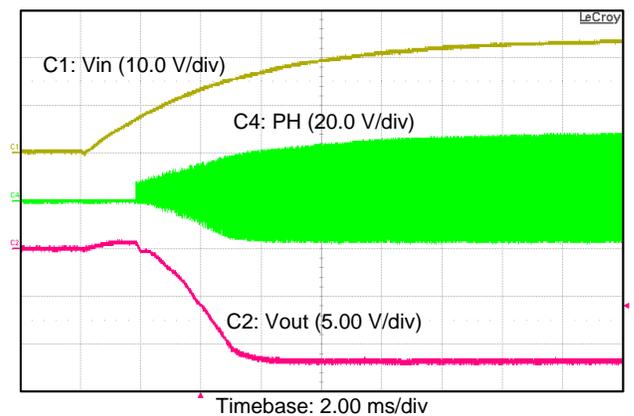**Figure 7. Load Regulation**

Figure 8. Line Regulation

Figure 9. Startup Waveform with 100 mA Load

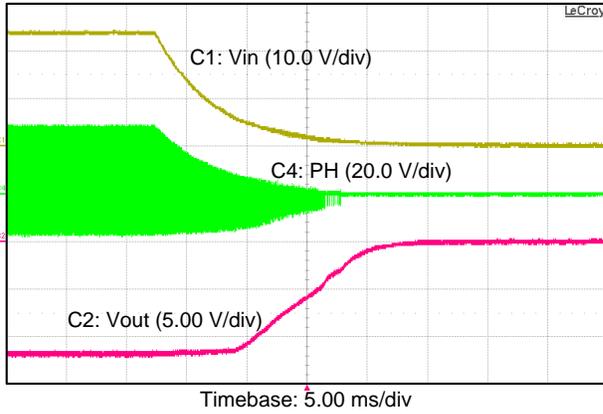Copyright © 2012, Texas Instruments Incorporated

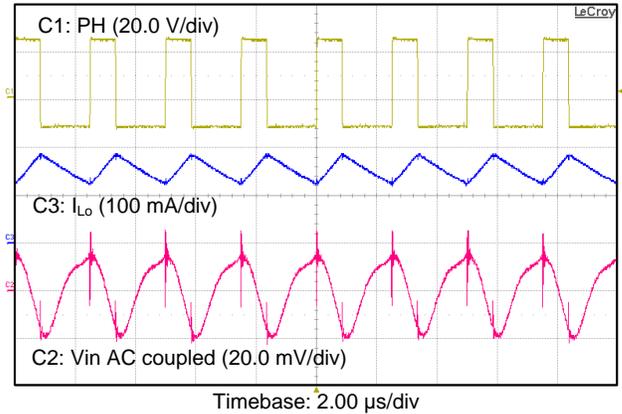**Figure 10. Shutdown Waveform with 100 mA Load**

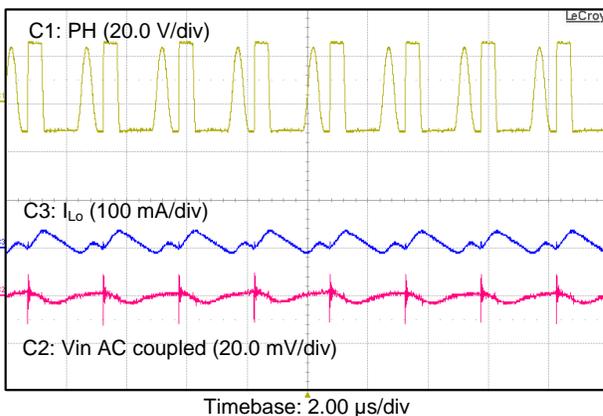**Figure 11. CCM Input Voltage Ripple**
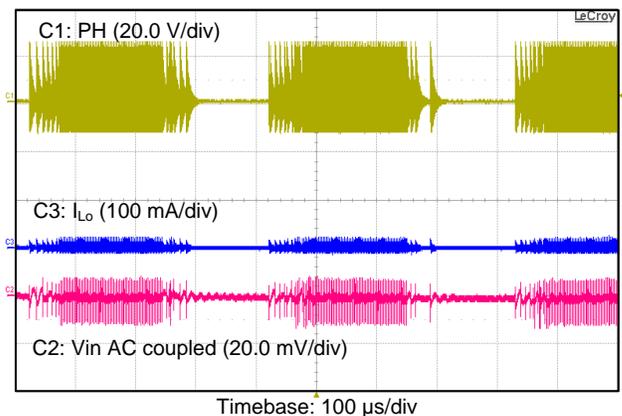

Figure 12. DCM Input Voltage Ripple

Figure 13. Pulse Skipping Input Voltage Ripple
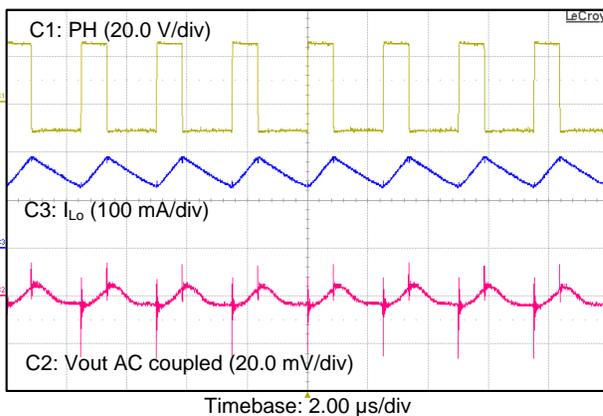
Figure 14. CCM Output Voltage Ripple

Figure 15. DCM Output Voltage Ripple

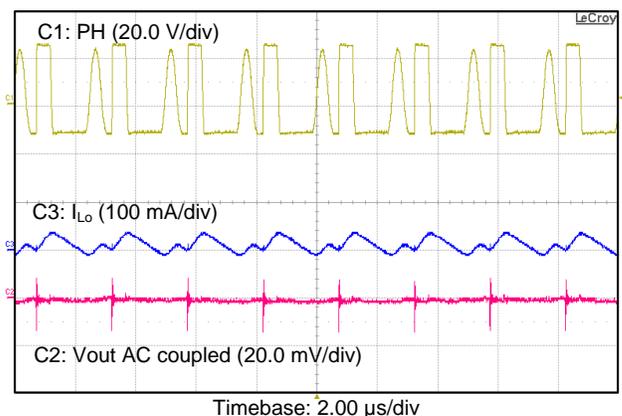Figure 16. Pulse Skipping Output Voltage Ripple

Figure 17. Output Voltage Load Transient Response
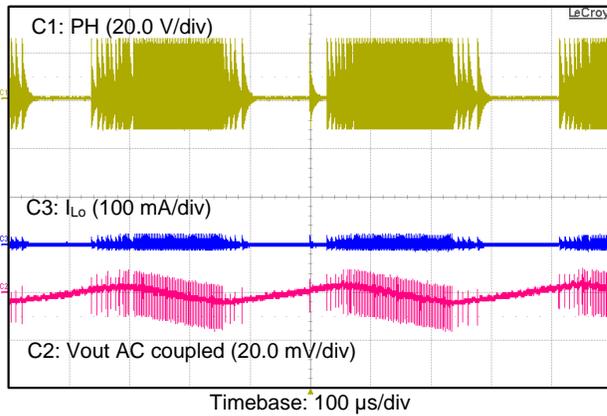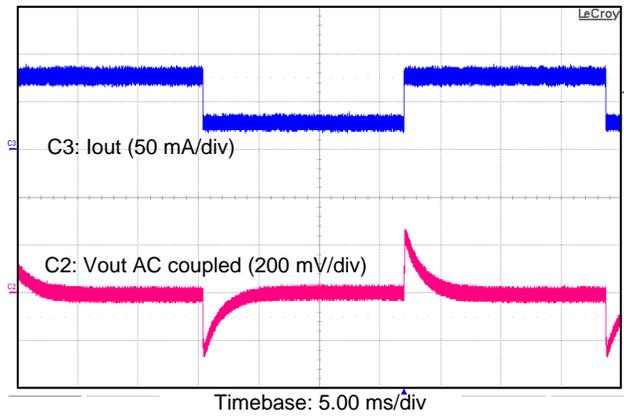
5 References

1. *Create an Inverting Power Supply From a Step-Down Regulator*, David Daniels, Application Report, Literature Number (SLVA317)
2. *Create an Inverting Power Supply Using a Synchronous Step-Down Regulator*, Sureena Gupta, Application Report, Literature Number (SLVA458)

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