Application Report
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Powering the OMAP-L132/OMAP-L137/OMAP-L138 Processors with the TPS650061 Power Management IC

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ABSTRACT

The OMAP-L13x series is a family of low-power DSP+ARM® applications processors geared for portable applications. These processors require a specific power-on and power-off sequence for reliable operation. This sequence is described and an inexpensive, discrete sequencing solution is provided that uses the TPS650061 Power Management IC. This circuit can be adapted for other Power Management ICs and processors as well.

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1 TPS650061 Overview

The TPS650061 is a versatile, high-efficiency Power Management IC that is designed with portable applications in mind. It incorporates a single 2.25 MHz step-down switching regulator and two low-dropout regulators in a compact 3x3 mm QFN package.

Power-sequencing with the TPS650061 is simplified since the switching regulator and LDOs have independent voltage inputs and enable controls. The device further extends functionality by adding a Supply Voltage Supervisor (SVS) circuit, which can be used to release the Reset pin of the load processor when the supply rails have reached their final voltage levels.

2 OMAP-L13x Power Requirements

The OMAP-L132, L137, and L138 processors have slightly different power supply requirements due to differences in peripherals and features. Some of these power requirements are also dependent on the processor operating frequency and user preference (for example, the DVDD3318_x supply can operate at 1.8V or 3.3V). Further information on voltage tolerance and maximum current requirements can be found on the TI Power Management website at www.ti.com/processorpower.

The OMAP-L132, L137, and L138 have similar power-on and power-off sequencing requirements, and the sequencing circuit presented in this document can be used for any of these processors. The power-on and power-off sequences have been summarized below. Keep in mind that some power supply names (ex. SATA_VDD) will only apply for certain OMAP-L13x devices.

2.1 Power-On Sequence

In general, the voltage rails must be powered on from lowest to highest voltage before the processor can be taken out of reset mode. The L13x processors should be powered-on in the following order:

1. The real-time clock supply (RTC_CVDD) may be powered from an external device (such as a battery) prior to all other supplies being applied, or it can be powered-up at the same time as CVDD since they are the same voltage.

2. Core logic supplies:
   (a) All variable 1.0V - 1.3V core logic supplies (CVDD)
   (b) All static core logic supplies (RVDD, PLLx_VDDA, USB_CVDD, SATA_VDD). If voltage scaling is not used on the device, groups 2a) and 2b) can be controlled from the same power supply and powered up together.

3. All static 1.8V I/O supplies (DVDD18, DDR_DVDD18, USBx_VDDA18, SATA_VDDR) and any of the I/O supply groups used at 1.8V nominal (DVDD3318_x).

4. All analog 3.3V PHY supplies (USBx_VDDA33) any of the I/O supply groups used at 3.3V nominal (DVDD3318_x).

5. A Power-On Reset (POR) must be asserted until all power supplies have reached minimum regulation. Power-On Reset is asserted by bringing the processor RESET and TRST pins low. Note that the L132, L137, and L138 have internal pulldown resistors on TRST.

There is no required voltage ramp-up rate for any of the supplies. However, the supplies operated at 3.3V (DVDD3318_x) must never exceed the static 1.8V supplies by more than 2 volts.

The general power-up requirements are summarized in the table below. Consult the specific processor data sheet for Recommended Operating Conditions and Absolute Maximum Ratings.

Table 1. Power-On Summary for OMAP-L13x Processors

Order	Supply Name	Nomainal Voltage (V)	Max. Current (mA) OMAP-L132	Max. Current (mA) OMAP-L137	Max. Current (mA) OMAP-L138
1	RTC_CVDD[1]	1.2	0.5	0.1	1
2a	CVDD[1,3]	1.2	500	600	600
2b	RVDD[1,2], PLLx_VDDA, USB_CVDD, SATA_VDD	1.2	70	60	200
3	DVDD18, DDR_DVDD18, USBx_VDDA18, SATA_VDDR, DVDD3318_x[4]	1.8	189	50	230
4	USBx_VDDA33, DVDD3318_x[4], DVDD[5]	3.3	93	115	114

1. RTC_CVDD, CVDD, RVDD are 1.3V for L137 456MHz version.
2. RVDD is 1.3V for L138 456 MHz version.
3. CVDD can be 1.0-1.3V nominal for L138 and 1.0-1.2V nominal for L132.
4. DVDD3318_x is a dual-voltage supply; it can operate at either 1.8V or 3.3V (L132 and L138 only).
5. DVDD is for L137, which can only operate at 3.3V.

2.2 Power-Off Sequence

There is no required voltage ramp-down rate for any of the supplies. However, the supplies operated at 3.3V (DVDD3318_x) must never exceed the static 1.8V supplies by more than 2 volts. If RTC_VDD is to be unpowered, it should take place after CVDD has been unpowered.

3 Schematic

The TPS650061 and the discrete sequencing circuit are shown in Figure 1. The output voltages have been configured using the external feedback resistors so that VDCDC, VLDO1, and VLDO2 are 1.2V, 3.3V, and 1.8V respectively. Additional bypass/decoupling capacitors not shown on the schematic *will be required* at the processor.

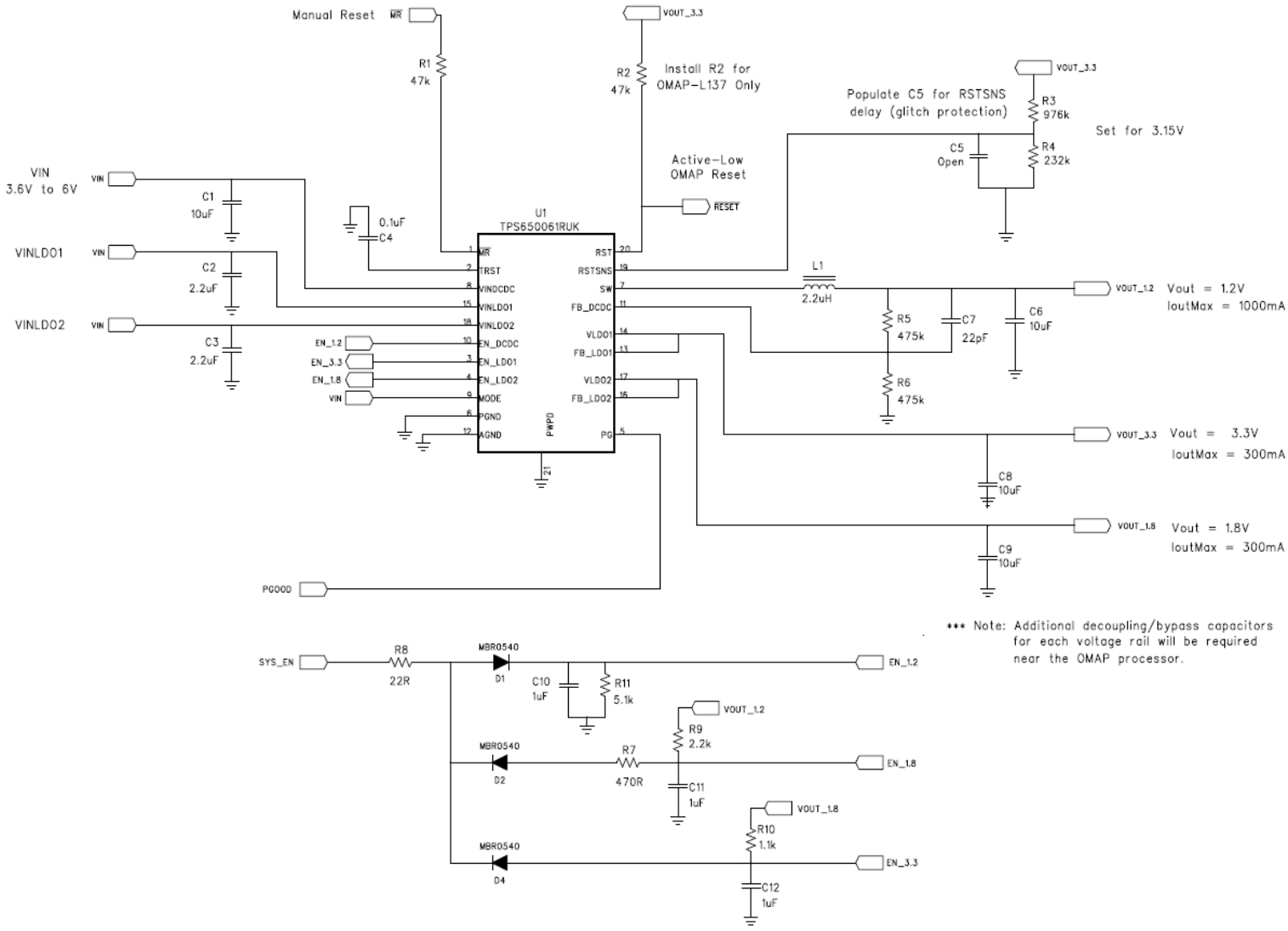

Figure 1: TPS650061 Schematic with Discrete Sequencing Components

4 Waveforms

The waveforms below show typical operation of the sequencing circuit during power-on and power-off cycles:

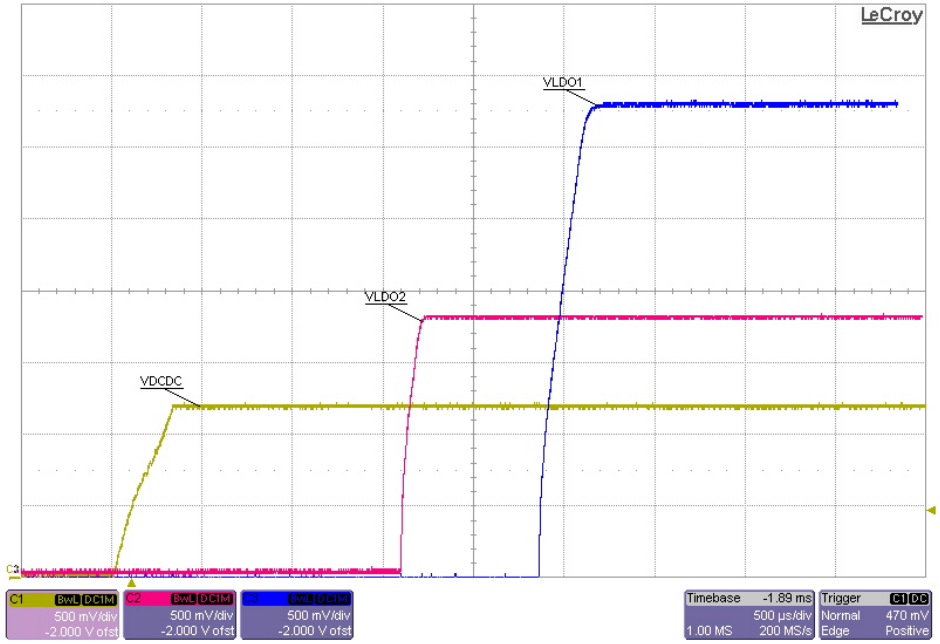

Figure 2: Power-On Sequence, 500 us/div

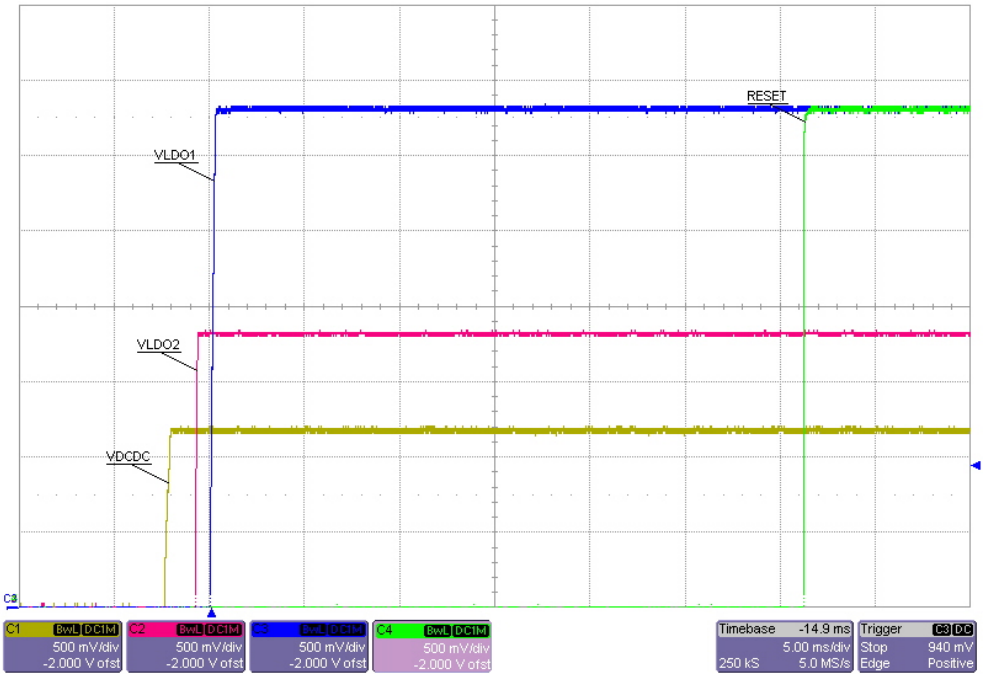

Figure 3: Power-On Sequence, 5 ms/div

For the turn-on sequence shown in Figure 2, note that the 1.2V rail (VDCDC) rises first, followed by the 1.8V (VLDO2) and 3.3V (VLDO1) rails. The same turn-on sequence is shown in Figure 3 on a larger timescale to show the /RST pin going high. The /RST pin goes high after a delay time once the 3.3V rail rises above 3.15V, as detected by the RSTSNS pin. The delay time of the /RST pin is controlled by an external capacitor on the TPS650061 TRST pin. Note that the 3.3V rail is always less than 2V above the 1.8V rail, satisfying the voltage margin requirements.

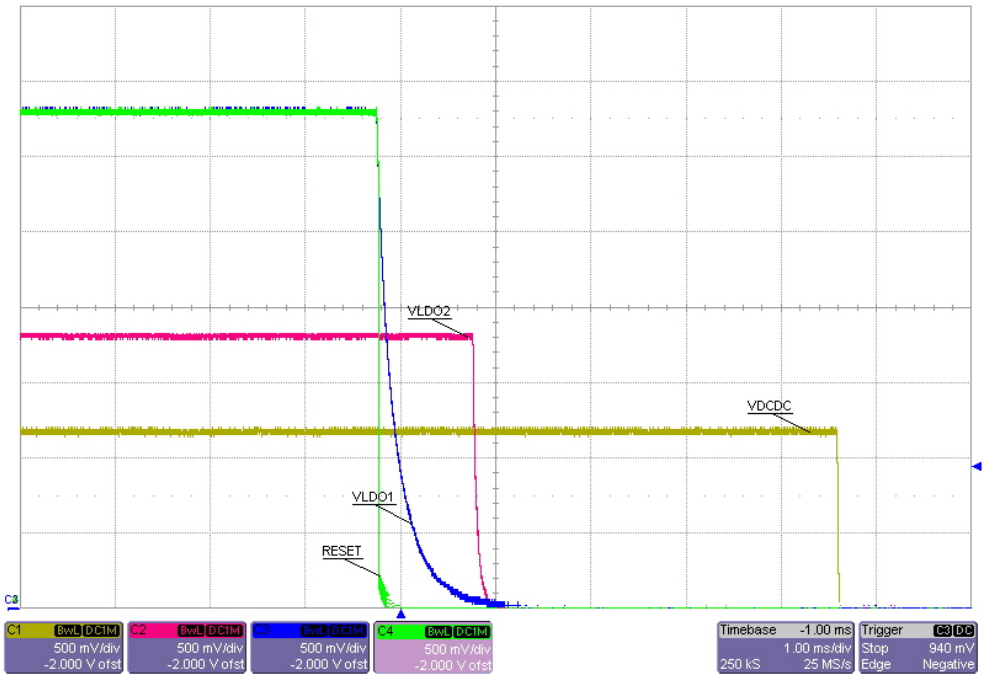

Figure 4: Power-Off Sequence, 1 ms/div

For the turn-off sequence shown in Figure 4, the 3.3V rail (VLDO1) goes low first, followed by the 1.8V (VLDO2) and 1.2V (VDCDC) rails. The /RST pin goes low when the 3.3V rail drops below 3.15V, as detected by the RSTSNS pin. Note that the 3.3V rail is always less than 2V above the 1.8V rail, satisfying the voltage margin requirements.

The circuit in Figure 1 was implemented on a TPS650061 Evaluation Module (TPS650061EVM-584) with the sequencing circuitry soldered to a small prototyping PCB. The waveforms above were taken at Vin = 4.2V with resistive loads at the full load conditions that are expected for the OMAP-L13x devices:

Table 2. Test Waveform Load Specifications

Supply Name	Voltage (V)	Current (mA)
VDCDC	1.2	850
VLDO2	1.8	250
VLDO1	3.3	120

5 Theory of Operation

This sequencing configuration uses a RC circuit on each of the TPS650061 Enable pins to ensure that the voltage rails turn on and off at different times. The values of the resistors and capacitors in the RC circuits determine the length of time between each successive voltage rail turn-on/off. The processor is turned on or off by bringing the System Enable (SYS_EN) node on the sequencing circuit high or low, respectively.

5.1 Startup

When SYS_EN is brought high, the 1.2V Enable (EN_1.2) will quickly go high and the 1.2V Output (VOUT_1.2) will turn on. Because of the orientation of diodes D2 and D4, EN_1.8 and EN_3.3 remain low at this time. As VOUT_1.2 rises, it charges the capacitor C11 through resistor R9. When the voltage at the EN_1.8 node exceeds the EN_1.8 threshold voltage, VOUT_1.8 will turn on. A similar process occurs to turn on VOUT_3.3.

Once VOUT_3.3 reaches the threshold of the RSTSNS pin, the Reset pin (/RST) will go high to enable the OMAP processor. The threshold is set at 3.15V for the schematic shown in Figure 1; it can be changed by adjusting the values of resistors R3 and R4. There is a delay between the triggering of the RSTSNS pin and the /RST pin going high. This delay time can be adjusted by changing the capacitor value on the TRST pin of the TPS650061 per the equation in the TPS650061 datasheet (SLVS810B).

5.2 Shutdown

Once the TPS650061 has been turned on, SYS_EN must be pulled to ground for power-down to occur. The outputs of the regulator will keep the Enable pins in a high state unless a path to ground through SYS_EN is provided.

When SYS_EN is pulled to ground, the capacitor on EN_3.3 will discharge quickly since there is a low-resistance path to ground. The voltage on EN_3.3 will drop, and VOUT_3.3 will turn off. Once VOUT_3.3 drops below 3.15V, the /RST pin will be pulled low to disable the processor.

The capacitor on the EN_1.8 node will begin to discharge at the same time as EN_3.3, but at a slower rate due to the resistor R7 in the capacitor's discharge path. This delays the turn-off of VOUT_1.8. The capacitor on the EN_1.2 node is discharged by the parallel resistor R11 since the polarity of the diode D1 will not allow a path to ground.

5.3 Supply Voltage Supervisor

The output of the Supply Voltage Supervisor (SVS), the /RST pin, connects to the active-low RESET pin of the OMAP-L13x processor. When the SVS is triggered, the /RST pin goes low, putting the processor into reset mode. The SVS can be triggered by the voltage on the RSTSNS analog comparator pin or by a forced reset on the /MR (Manual Reset) pin.

The sequencing circuit in this report takes advantage of the RSTSNS analog comparator to release the processor reset only when the VOUT_3.3 rail has reached approximately 3.15V, and to assert the processor reset when the VOUT_3.3 rail drops below 3.15V. The user can also use an external switch, transistor, or microcontroller to toggle the /MR pin and trigger a processor reset as needed.

6 Design Considerations

Although the discrete sequencing circuit is simple, care must be taken to ensure the circuit will operate in a specific application.

6.1 Enable Pin Thresholds

A voltage divider is formed at the EN_1.8 node due to R9 and R7; when SYS_EN is low, the voltage at the EN_1.8 node should be less than the threshold for the EN_1.8 pin (0.4V max). If R7 and R9 prevent the voltage from dropping low enough, VOUT_1.8 will not turn off. The value for R7 should be large enough to delay the EN_1.8 turn-off, but small enough for turn-off to occur.

6.2 Inrush Current

Inrush current in excess of 1A can occur on SYS_EN when it is pulled high due the low-impedance path to the capacitor on the EN_1.2 node. Use a small-value resistor in series with SYS_EN to limit the inrush current (R8 is 22 ohms in the schematic). Using too high a resistor value will influence the EN_1.8 voltage divider ratio since R7 will be connected to ground in series with R8 (see Section 6.1). If controlling SYS_EN with a microcontroller or other logic device, be sure that any inrush current does not exceed the maximum ratings of that device.

6.3 Diode Selection

Due to their low forward voltage drop (0.15-0.45V) and fast switching speed, Schottky diodes are recommended in the sequencing circuit. Schottky diodes also have a shorter reverse recovery time compared to other types of diodes, minimizing reverse current overshoot when changing from the forward conducting to the reverse blocking state.

6.4 Load Turn-Off Time

A factor that may affect the turn-off time is the capacitance and load resistance on the TPS650061 outputs. Since the DC/DC switching converter and the LDOs in the TPS650061 will look “open” to the output when disabled, the output voltage decay will be depend partly on the capacitance and load resistance on the output. Design the output capacitance to meet the ripple requirements of the processor and adjust the sequencing circuit component values if necessary to ensure proper sequence timing.

6.5 Output Capacitors

The OMAP-L13x processors will require several local bypass/decoupling capacitors in addition to the bulk output capacitors shown in Figure 1. The values of these capacitors will depend on the ripple tolerance of the voltage rails and the activity (load) of the processor and I/O peripherals. Ripple tolerance specifications can be found in the Recommended Operating Conditions table in the processor datasheet. Design the output capacitance to meet the ripple requirements of the processor and adjust the sequencing circuit component values if necessary to ensure proper sequence timing.

6.6 Power Good

The Power Good (PG) pin on the TPS650061 is an open-drain output that indicates the condition of the enabled step down converter and LDOs. The PG pin is pulled low only if all three outputs are regulating correctly. In the event one of the TPS650061 outputs fails because of a short or other means, the PG pin will change to a High-Z state. This can provide an additional level of protection to the system; an external transistor or microprocessor can be used to monitor the state of PG and disable SYS_EN to avoid possible damage to the processor.

6.7 RESET Pull-up Resistors

The active-low RESET pin on the OMAP-L13x processors should be pulled high during normal operation to prevent undesired processor resets. An external pull-up resistor to VOUT_3.3 is required on the RESET line for the OMAP-L137. The L132 and L138 have internal pull-up resistors on the RESET pin that connects to the DVDD3318_B supply.

7 References

1. TPS650061*, 2.25 MHz Step-Down Converter* Datasheet (SLVS810B).
2. *Using the TPS650061EVM 2.25 MHz Step-Down Converter with Dual LDO* (SLVU354).
3. OMAP-L132 C6-Integra™ DSP+ARM® Processor Datasheet (SPRS762).
4. *OMAP-L137 Low-Power Applications Processor* Datasheet (SPRS563E).
5. *OMAP-L138 C6-Integra™ DSP+ARM® Processor* Datasheet (SPRS586D).

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8 Bill of Materials

Below is the Bill of Materials for the circuit shown in Figure 1. Note that the RefDes numbers do not correspond to those on the TPS650061 Evaluation Board (TPS650061EVM-584).

Table 3: Bill of Materials

RefDes	Value	Description	Size	Part Number	Mfr	Qty
C1, C6, C8, C9	10uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	muRata	4
C2, C3	2.2uF	Capacitor, Ceramic, 16V, X5R, 10%	0603	GRM188R61C225KE15D	muRata	2
C4	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0805	GRM21BR71H104KA01L	muRata	1
C5	0.1uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std	0
C7	22pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std	1
C10, C11, C12	1uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	Std	Std	3
D1, D2, D3	MBR0540	Diode, Schottky, 0.5A, 40V	SOD-123	MBR0540	Fairchild	3
L1	2.2uH	Inductor, SMT, 2.0A, 110mΩ	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft	1
R1, R2	47kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std	2
R3	976kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std	1
R4	232kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std	1
R5, R6	475kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std	2
R7	470Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std	1
R8	22Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std	1
R9	2.2kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std	1
R10	1.1kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std	1
R11	5.1kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std	1
U1	TPS650061	IC, 2.25 MHz Step-Down Converter with Dual LDOs and SVS	QFN	TPS650061RUK	TI	1

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