

Powering the TMS320C6742, TMS320C6746, and TMS320C6748 With the TPS650061

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Battery Power applications

ABSTRACT

This document details the design considerations of a power solution for the TMS320C742, TMS320C6746, and TMS320C6748 (TMS320C6742/C6746/C6748) low-power application processor with a TPS650061, three-rail power management unit (PMU) or power management integrated circuit (PMIC).

Portable application solution size demands a high level of integration and the TMS320C6742/C6746/C6748 requires at least three different voltage rails with specific sequencing and reset requirements. The TPS650061 is a highly integrated power solution that can provide the 1.2-V, 1.8-V and 3.3-V rails and RESET signal required by the TMS320C6742/C6746/C6748. The TPS650061 has a single step-down converter, two low dropout regulators, and a voltage supervisor.

Included in this document is a power solution for the TMS320C6742/C6746/C6748. Power requirements, illustrated schematic, operation waveforms, performance data, and bill of materials are provided.

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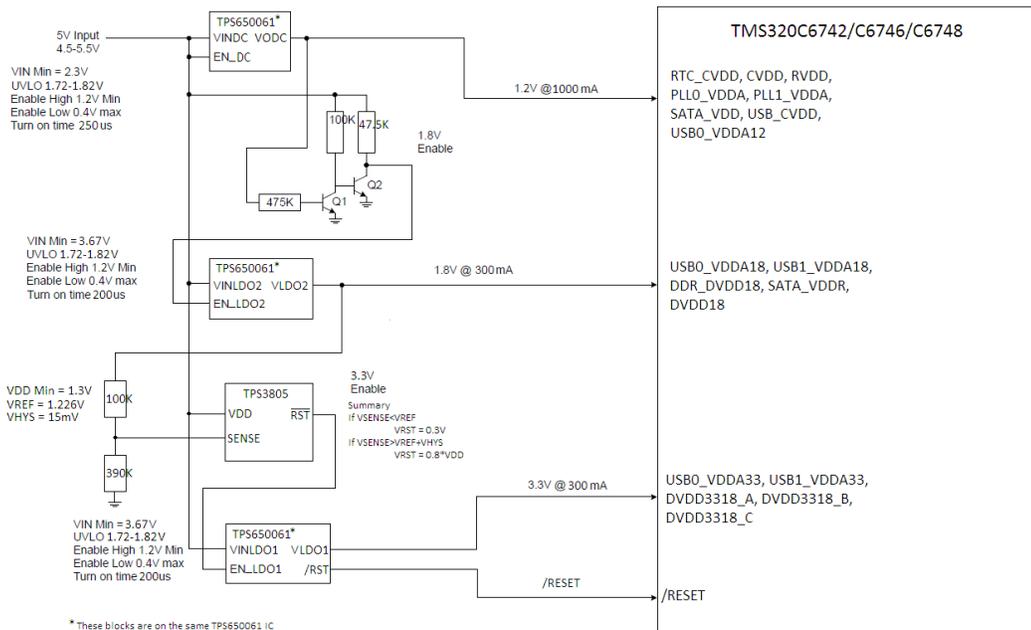


Figure 1. TPS3805, TPS650061, and TMS320C6742/C6746/C6748 Block Diagram

1 Power Requirements

The TMS320C6742/C6746/C6748 power requirements are listed in [Table 1](#).

Table 1. TMS320C6742/C6746/C6748 Power Requirements

Rail Name	Voltage (V)	I _{max} (mA)	Tolerance
RTC_CVDD	1.2	1	-25%, +10%
CVDD	1.2	375	-9.75%, +10%
RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	-5%, +10%
USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%
USB0_VDDA33, USB1_VDDA33	3.3	24	±5%
DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8/3.3	50/90	±5%

The TPS650061 meets these power requirements with its single step-down converter, two low dropout regulators and voltage supervisor.

1.1 Power-On Sequence

To meet the TMS320C6742/C6746/C6748 power-on requirements, the 1.2-V rail must power on first, then the 1.8-V rail, and lastly the 3.3-V rail. After all three rails are up, the RESET may be released. To ensure this power-up sequence, the 1.2-V enable is connected to VIN and the output is connected to EN_LDO2 through two transistors. The output of LDO2, VLDO2, is connected to the sense input of an SVS that has its RESET output connected to EN_LDO1. To ensure that the TPS650061 asserts its reset until all three supplies are up, RST is pulled up to VLDO2, MR is pulled up to VODC, and RSTSNS is connected to VLDO1 with a resistor divider. The proper connections for this power-on sequencing are shown in [Figure 2](#).

When selecting components for the circuit, consider the following:

- The resistor divider on RSTSNS is such that if VLDO1 goes below 3.3 V – 5% (3.125 V), reset becomes active (opens).
 - Because \overline{RST} is pulled up to VLDO2 and \overline{MR} is pulled up to VODC, it only goes high if VODC, VLDO1, and VLDO2 are all present.
- The RSTSNS pin can be connected to an external RC network to set the deglitch timing for triggering a reset when the RSTSNS pullup voltage falls below the set threshold.

Per the excerpt from the TMS320C6742/C6746/C6748 data sheet, the device must be powered on in the following order:

1. RTC (RTC_CVDD) can be powered from an external device (such as a battery) prior to all other supplies being applied or powered up at the same time as CVDD. If the RTC is not used, connect RTC_CVD to CVDD. RTC_CVDD must not be left unpowered while CVDD is powered.
2. Core logic supplies:
 - (a) CVDD core logic supply
 - (b) Other 1.2-V logic supplies (RVDD, PLL0_VDDA, PLL1_VDDA, USB_CVDD). If voltage scaling is not used on the device, groups 2a) and 2b) can be controlled from the same power supply and powered up together.
3. Use all 1.8-V I/O supplies (DVDD18, DDR_DVDD18, USB0_VDDA18) and any of the LVCMOS IO supply groups at 1.8 V nominal (DVDD3318_A, DVDDA3318_B, or DVDD3318_C).
4. All analog 3.3-V PHY supplies (USB0_VDDA33; this is not required if USB0 is not used) and any of the LVCMOS I/O supply groups used at 3.3 V nominal (DVDDA3318_A, DVDDA3318_B, or DVDDA3318_C).

No specific voltage ramp rate is required for any of the supplies as long as the LVCMOS supplies operated at 3.3 V (DVDDA3318_A, DVDDA3318_B, or DVDDA3318_C) never exceed STATIC 1.8-V supplies by more than 2 V. \overline{RESET} must be maintained active until all power supplies have reached their nominal values.

The TMS320C6742 Silicon Errata mentions that the DVDD18 voltage rail can pull up to 2.7 V when using dual-voltage I/Os at 3.3 V. To address this potential issue, a work-around (1a) from the errata is implemented. This work-around asserts that maintaining sufficient bulk capacitance on the DVDD18 supply ensures that it is not pulled up to 2.7 V. The capacitor value selected was calculated using the equation $I = C \times (dV/dt)$, where dV/dt is the ramp rate of the DVDD3318_x supply (around 280 μ s) and I is the maximum leakage current into the DVDD18 supply (140 mA). The calculation gives a capacitance value of 11.88 μ F, so the nearest valued available capacitor (22 μ F) was chosen and connected to the 1.8-V output rail.

1.2 Power-Off Sequence

For the TMS320C6742/C6746/C6748, the power supplies can be powered off in any order as long as the LVCMOS supplies operated at 3.3 V (DVDDA3318_A, DVDDA3318_B, or DVDDA3318_C) never exceed STATIC 1.8-V supplies by more than 2 V. No specific voltage ramp down rate is required for any of the supplies (except as required to meet the aforementioned voltage condition).

To meet the power-off requirement, this design uses the TPS3805 voltage supervisor and a resistor divider to detect the voltage of the 1.8-V rail. The TPS3805 has a threshold voltage of 1.226 V; therefore, using a resistor divider of $R1 = 100 \text{ k}\Omega$ and $R2 = 390 \text{ k}\Omega$ results in a trip voltage of 1.54 V. This setup ensures that the 3.3-V rail never exceeds the 1.8-V rail by more than 2 V. Note that if the LVCMOS IO supply groups are used at 1.8 V instead of 3.3 V, the TPS3805 is not needed.

2 Schematic

Figure 2 presents the schematic of the power solution for the TMS320C6742/C6746/C6748.

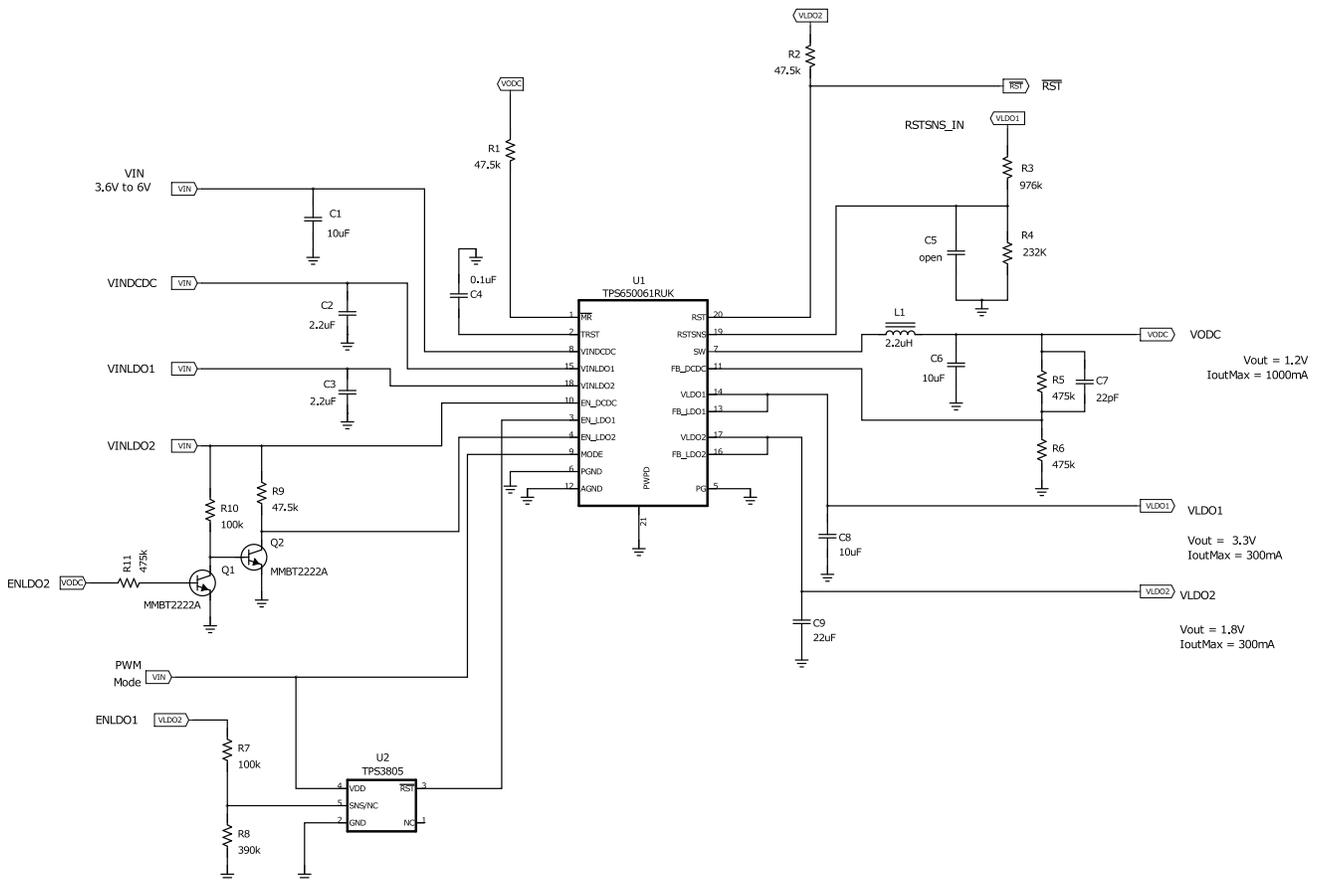


Figure 2. TPS650061 Schematic Diagram

3 Waveforms

The following waveforms demonstrate the start-up sequence and the reset of the TPS650061 as required by the TMS320C6742/C6746/C6748.

Figure 3 shows the TPS650061 power-on sequence of 1.2 V, then 1.8 V, and 3.3 V. Figure 4 shows the reset pin, \overline{RST} , being released after the voltage on RSTSNS rises above the threshold and after the reset recovery time, t_{RST} , is exceeded. Figure 5 shows the power-down sequence where the 3.3-V rail never exceeds the 1.8-V rail by more than 2 V.

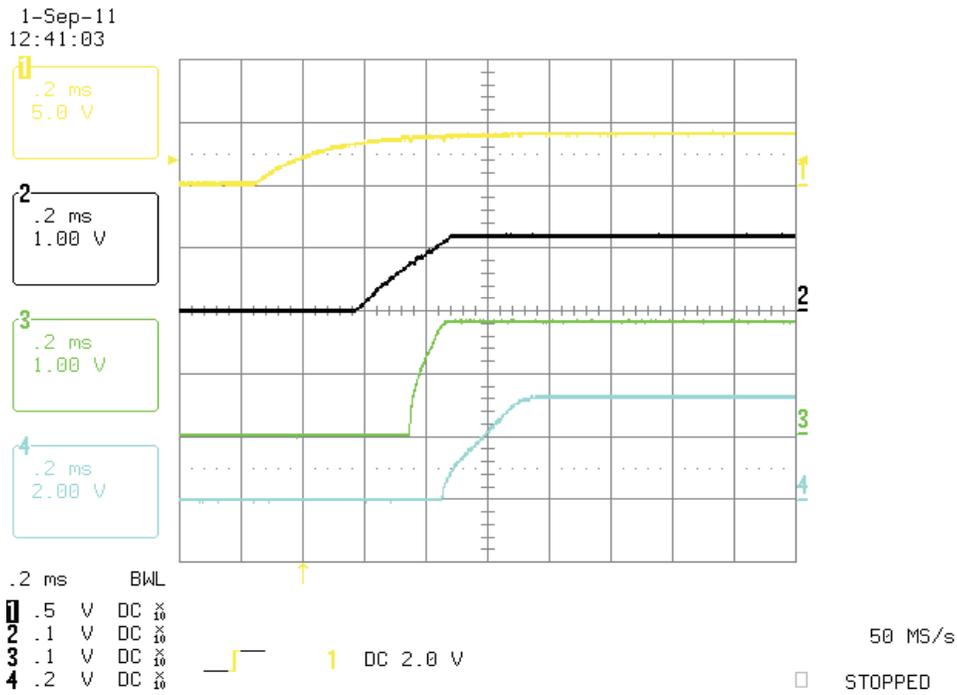


Figure 3. TPS650061 Power-On Ch1-Vin, Ch2-VODC, Ch3-VLDO2, Ch4-VLDO1

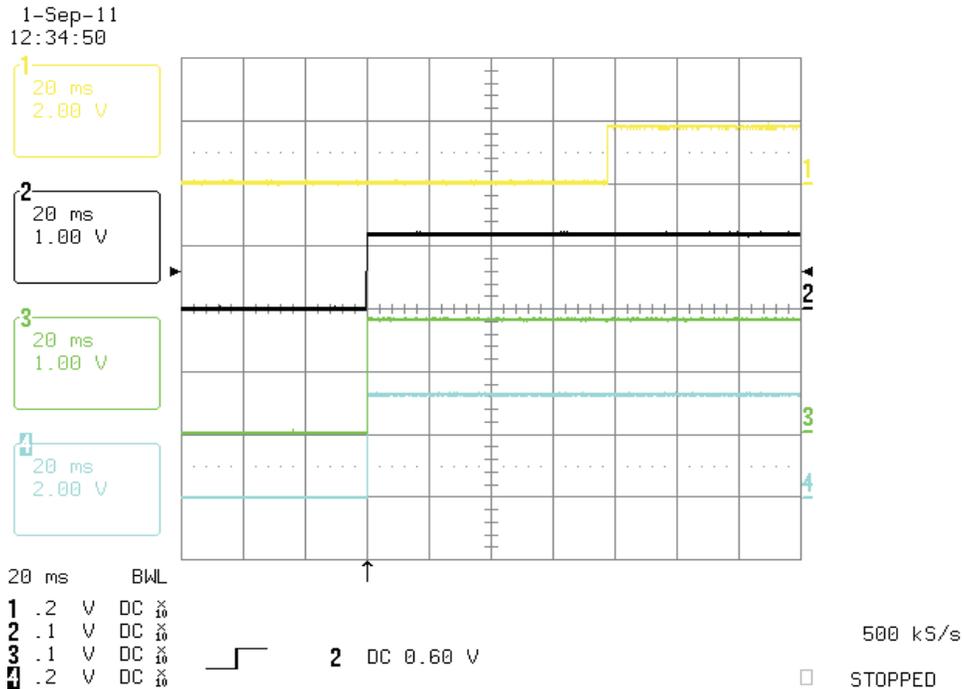


Figure 4. TPS650061 Power-On and $\overline{\text{RESET}}$ Ch1- $\overline{\text{RST}}$, Ch2-VODC, Ch3-VLDO2, Ch4-VLDO1

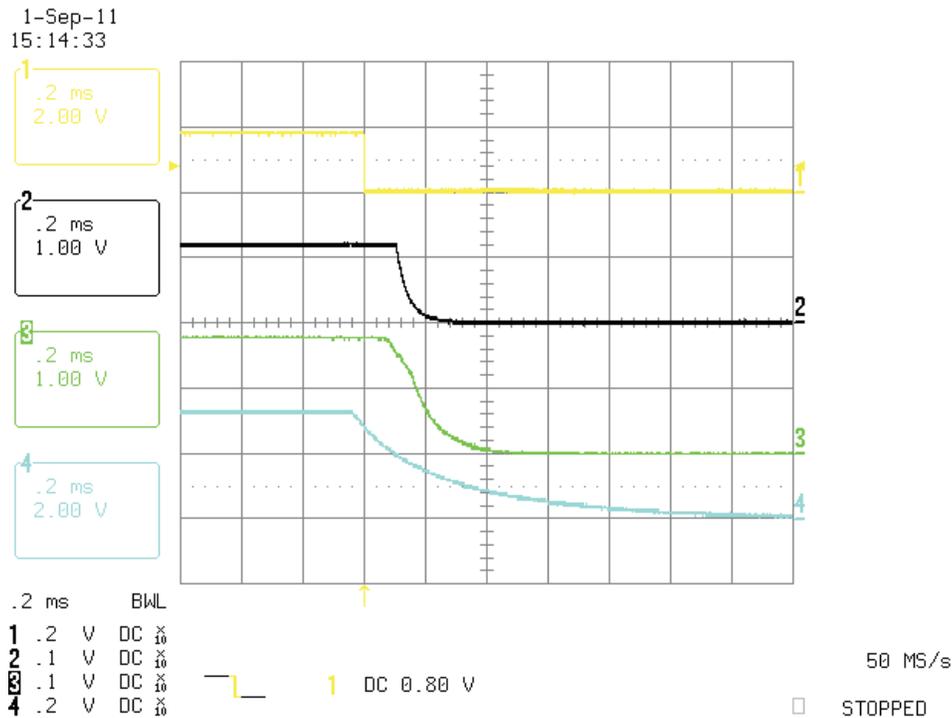


Figure 5. TPS650061 Power-Off Ch1–RST, Ch2–VODC, Ch3–VLDO2, Ch4–VLDO1

4 Bill of Materials

The bill of materials is displayed in [Table 2](#).

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
3	C1, C6, C8	10 μ F	Capacitor, Ceramic, 10 V, X5R, 10%	0805	Std	Std
1	C9	22 μ F	Capacitor, Ceramic, 10 V, X5R, 10%	0805	Std	Std
2	C2, C3	2.2 μ F	Capacitor, Ceramic, 10 V, X5R, 10%	0603	Std	Std
2	C4, C5	0.1 μ F	Capacitor, Ceramic, 16 V, X7R, 10%	0603	Std	Std
1	C7	22 pF	Capacitor, Ceramic, 50 V, COG, 5%	0603	Std	Std
1	L1	2.2 μ F	Inductor, SMT, 2.0 A, 110 m Ω	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft
3	R1, R2, R9	47.5 k Ω	Resistor, Chip, 1.16 W, 1%	0603	Std	Std
4	R3, R5 R6, R11	475 k Ω	Resistor, Chip, 1.16 W, 1%	0603	Std	Std
2	R7, R10	100 k Ω	Resistor, Chip, 1.16 W, 1%	0603	Std	Std
1	R4	255 k Ω	Resistor, Chip, 1.16 W, 1%	0603	Std	Std
1	R8	390 k Ω	Resistor, Chip, 1.16 W, 1%	0603	Std	Std
1	U1	TPS650061RUK	IC, 2.25 MHz Step Down Converter with Dual LDOs and SVS	QFN	TPS650061RUK	TI
1	U2	TPS3805	IC, Voltage Detector	SOP-5 (DCK)	TPS3805	TI
2	Q1, Q2	MMBT2222A	Transistor, NPN, High-Performance, 500 mA	SOT-23	MMBT2222A	Fairchild

5 Conclusion

The TPS650061 provides a low-cost, comprehensive power solution for the TMS320C6742/C6746/C6748. A 1.2-V rail (capable of supplying 1 A) is powered on followed by a 1.8-V rail (300 mA), and then a 3.3-V rail (300 mA); once all three supplies have reached minimum regulation, $\overline{\text{RESET}}$ goes high (i.e., rises to its pullup voltage). This meets the power requirements of the TMS320C6742/C6746/C6748.

6 References

1. *TPS650061, 2.25 MHz Step Down Converter with Dual LDOs and SVS* data sheet ([SLVS810](#))
2. *TMS320C6742, TMS320C6742 Fixed/Floating-Point DSP* data sheet ([SPRS587](#))
3. *TMS320C6746, TMS320C6746 Fixed/Floating-Point DSP* data sheet ([SPRS591](#))
4. *TMS320C6748, Fixed/Floating-Point DSP* data sheet ([SPRS590](#))
5. *Powering OMAP-L132/L138, C6742/4/6, and AM18x with TPS65070* application report ([SLVA371](#))
6. DM355 Reference Design ([SLVR331](#))
7. *TMS320C6742 Fixed/Floating-Point DSP Silicon Revisions 2.1, 2.0, 1.1 and 1.0 Silicon Errata* ([SPRZ305](#))

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