Application Report
SLVA449–December 2010

Protection for EOS for IEEE1394 Lines With TPD4S1394

Vinod Mukundagiri, Sagir Hasnain *High Volume Linear*

ABSTRACT

The IEEE 1394 interface is a serial bus interface standard for high-speed communications and isochronous real-time data transfer. It is frequently used by personal computers, as well as in digital audio, digital video, automotive, and aeronautics applications. All 1394 PHY devices are susceptible to electrical overstress damage when exposed to a combination of high-voltage cable power and a faulty cable or connector system that allows data (TPx) and cable power (Vp) connections to engage before the cable ground (Vg) connection. This set of circumstances is known as a "Late-Vg" event. Though there are many ways to take precautions against this event, a robust solution is to disconnect the power to the cable when late-Vg occurs.

The information in this application report is intended to help customer/system designers understand how to design a late-Vg protection circuit in their systems using the TPD4S1394.

Contents

List of Figures

1 Introduction

The IEEE 1394A-2000 specification calls for 1394 cable power (Vp) to range from 8 VDC up to 30VDC with a maximum current of 1.5 A. Legacy IEEE 1394-1995 systems can support cable power of 8 VDC up to 40 VDC, also with a maximum current of 1.5A. A typical 1394 PHY device has an absolute maximum input voltage rating of –0.5 VDC to VDD + 0.5 VDC, where the maximum value of VDD is 4.0 VDC. There is an obvious potential for catastrophic damage to a 1394 PHY device if the voltage levels of Vp (~30V) are presented on the differential pair signals of the 1394 PHY device.

If the Vp connection and any of the data (TPx) connections of two 1394 nodes are engaged before the Vg connection, high voltage can appear on the TPx signals in what is known as a *late-Vg* event. The IEEE 1394-1995 specification requires that the Vg and the Vp pins of the connector receptacle are approximately 15% longer to help ensure that these connections are "first make, last break", but this can be compromised if a cable is inserted at an extreme angle. Also, if the Vg connection is not well connected due to distressed cables or connectors, there is also a potential for a late-Vg event.

2 System Information

In a typical application, we see that the 1394 port is powered from an external port power supply which can range from 24V to 40V. As describe above, an occurrence of late-Vg event can cause catastrophic damage at such levels.

In cable powered systems, we see that the damage caused by a late-Vg event is due to cable power that is seeking a return path, thus systems that rely heavily on 1394 cable power are more likely to see late-Vg damage. The IEEE 1394A-2000 specification limits Vp supported on the 1394 bus to 30VDC. Typical PC applications source 10 VDC–12 VDC on Vp driven by the PCI bus. Damage to 1394 PHY devices due to a late-Vg event occurs most often on systems with Vp greater than 15VDC. Using older or worn out cables can also cause the late-Vg event to trigger by not allowing the Vg pin to make good contact. The 6-pin connectors are more susceptible to a late-Vg failure than the 9-pin ones.

Since the 1394 ports are externally exposed, it is important to have IEC level ESD protection on the Tp pins. For transmitting the high data rates of IEEE 1394, Tp pin capacitance must be kept low to meet the specification requirement. It is important to ensure that the IEC protection devices do not add too much additional capacitance and harm the data transmission eye-diagram requirement.

One approach to late-Vg protection is to use the breakdown of the ESD diodes to clamp the voltage to the PHY such that the majority of the late-Vg current flows through the ESD diodes thereby protecting the I394 port/controller. In this case the ESD diodes only act as a bypass path and hence don't completely solve the problem as late-Vg is not an ESD event. There is still a risk present that the ESD clamping voltage presented to the PHY during a late-Vg event may harm the reliability of the device and damage it permanently.

3 Device Architecture

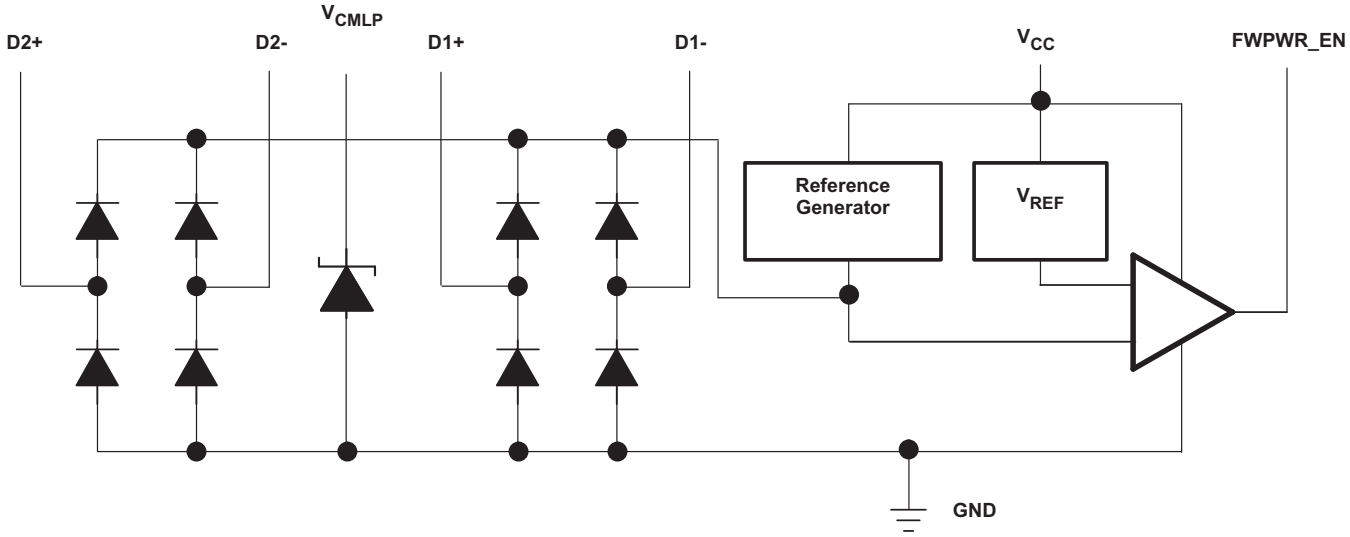

Figure 1. Block Diagram of TPD4S1394

Shown in Figure 1 is an internal block diagram of the TPD4S1394. It is comprised of 4 TVS type ESD clamp circuits, reference generators and a comparator. The ESD clamp circuits of the TPDS1394 are capable of providing IEC61000-4-2 (Level 4) system level ESD protection at the TP lines of the 1394 interface. In addition, these pins are rated at ±15kV HBM.

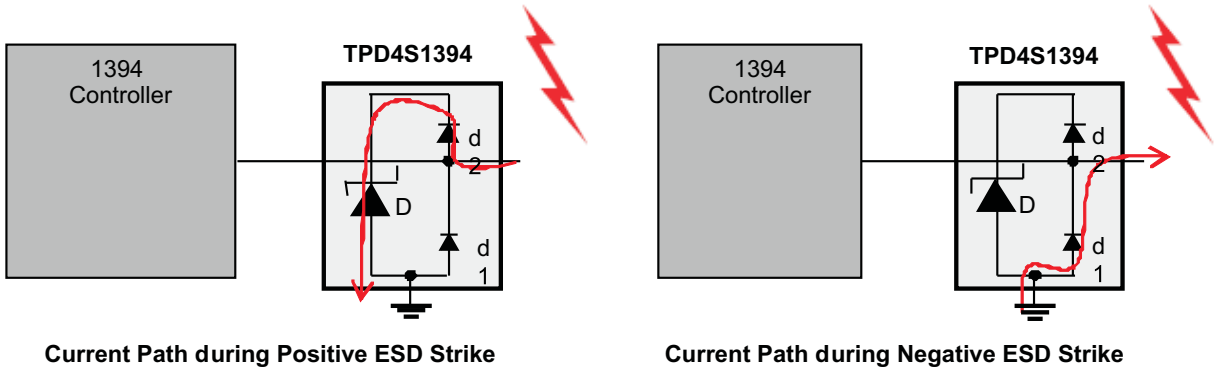

Figure 2. Current Path for IEC ESD Stress (Only One ESD Clamp Circuit is Shown)

The internal comparator with hysteresis is present to detect if an occurrence of late-Vg has taken place. Two internal references are used to determine if the Tp lines remain within acceptable voltage levels under normal mode of operation. The built in ESD protection devices work with the internal analog circuits to make sure that even under the event of an IEC or late-Vg, the internal circuits are protected and switch back to normal operation after the event has disappeared. The VOH level for FWPWR_EN output is ≥0.7Vcc at 10mA and the VOL level is ≤0.3Vcc at 10mA. The high level of the FWPWR_EN is referenced to the Vcc supply of the chip.

Referring to Figure 2, the TPD4S1394 employs a three diode configuration to implement the system level ESD solution at the 1394 TPx data lines. The central diode, D, is much larger in size and associates with higher capacitance to GND. The d1 and d2 diodes are much smaller in size and work to hide the larger capacitance of the central diode D. Since the TPx data lines are connected to d1, d2 diodes, the data lines are exposed to lower capacitance (1.5pF IO to GND) of the d1, d2 diodes only. During positive ESD strike, the central diode D breaks down and offers current path through d1 and D to GND and keeps the signal line from going too far above the supply rail. During negative ESD strike, the diode d2 conducts and keeps the signal line from going too far below ground. These diodes and their metal system are large enough to handle the high currents and protect the system from IEC 61000-4-2 ESD event.

4 Application Design

In order to design the TPD4S1394 into a system, it is important to understand the power source from the external source/power port. Shown in Figure 5 is a simple example of how the TPD4S1394 can be used in an application to protect the IEEE1394 controller. If a DC/DC converter or a load switch is used, there must be an enable pin to that device. This pin can either be an active high or active low shutdown. The TPD4S1394 provides an active high shutdown signal (FWPWR_EN) on the occurrence of a late-Vg event. The voltage level of this signal is equal to the controller supply or device supply of the TPD4S1394. The $\mathbf{V_{CLMP}}$ pin is a **No Connect** pin and is only useful for debug purposes to measure the internal reference voltage. This pin must be left open (not connected to any power supply or signal) under normal operating conditions. During the system design phase, this pin can be used for debugging by forcing an external voltage to it in order to trigger the comparator and get the FWPWR_EN signal to go high.

In a normal mode of operation as shown in Figure 3, an internal reference generator is connected to the V_{CLMP} pin and another reference voltage, both of these is fed to an internal comparator. By default, the output of the comparator to the FWPWR_EN pin is high. When a late-Vg event occurs, the Tp lines start rising due to the power port supply being active. During the event, the data lines rise high enough that the **internal ESD clamp** is triggered, holding the lines at the breakdown voltage for the clamp.

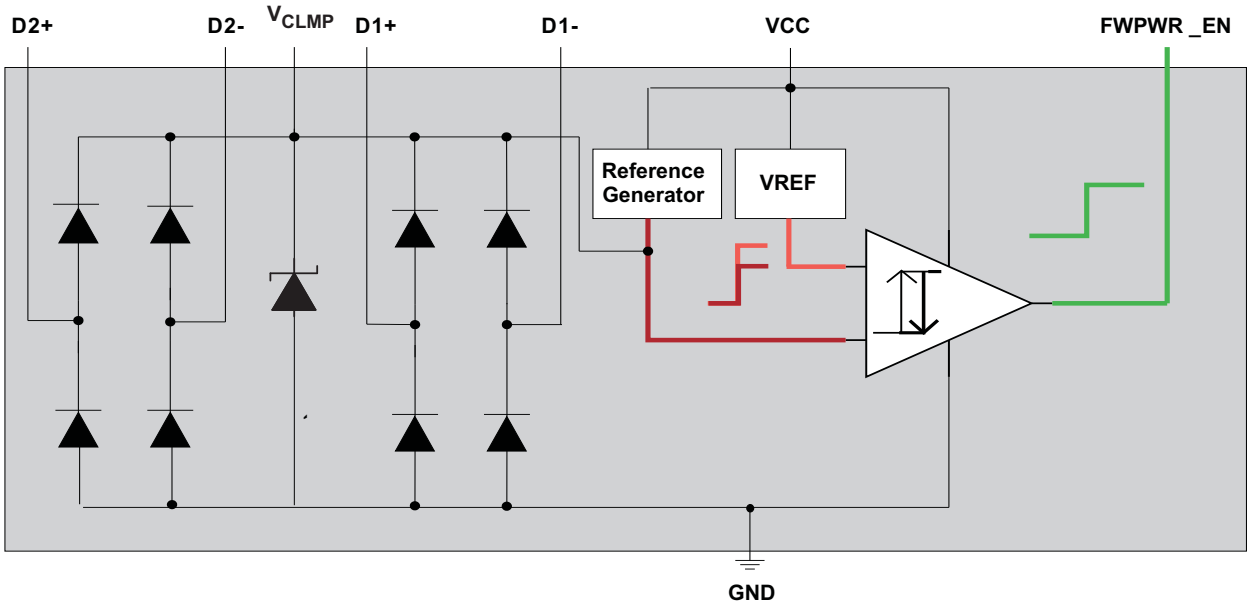

Figure 3. Output of FWPWR_EN High Under Normal Operation

During this time, the internal comparator will trip as soon as the VCLAMP level crosses the comparator threshold. This will in turn cause FWPWR_EN to immediately go low as shown in Figure 4. The comparator has an internal hysteresis to prevent noise from causing a false event. When proper connection has been established, the voltage on the Tp lines starts to return to their normal levels. When VCLAMP returns below the comparator threshold, there is an internal timer which prevents the FWPWR_EN from going high immediately. The purpose of this timer is to ensure that the Tp voltage has gone down to sufficient levels for safe operation. Once the timer times out, then the FWPWR_EN output goes to logic high.

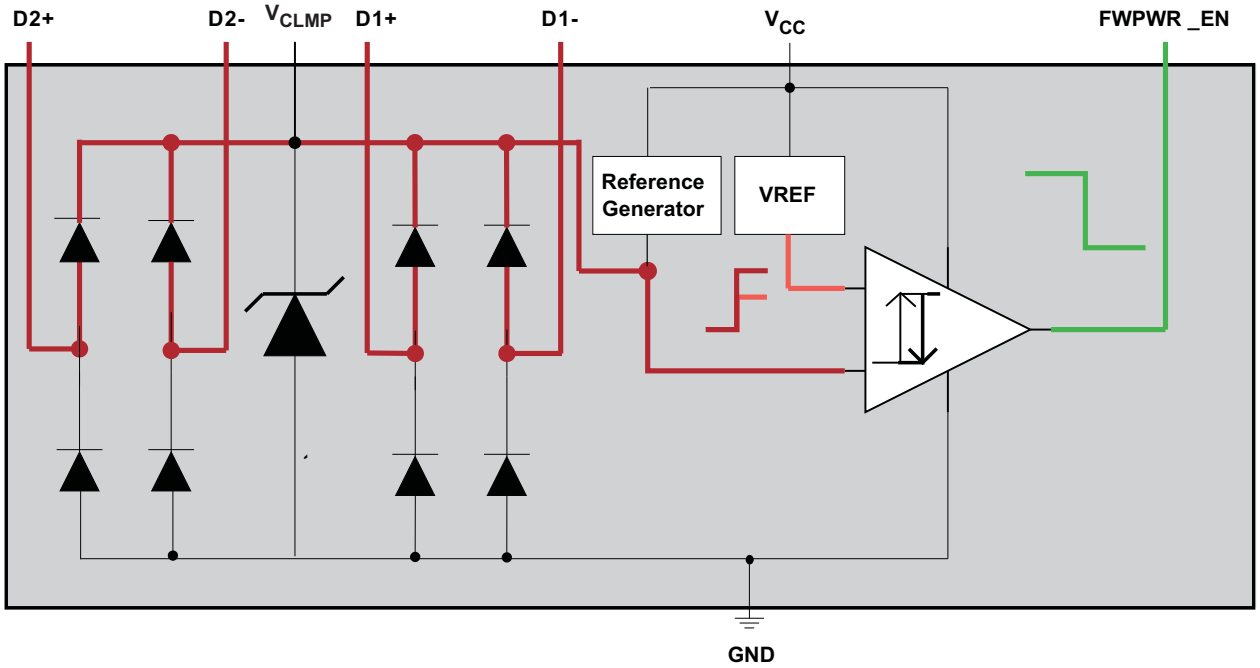

Figure 4. Output of FWPWR_EN High Under Late-Vg Event

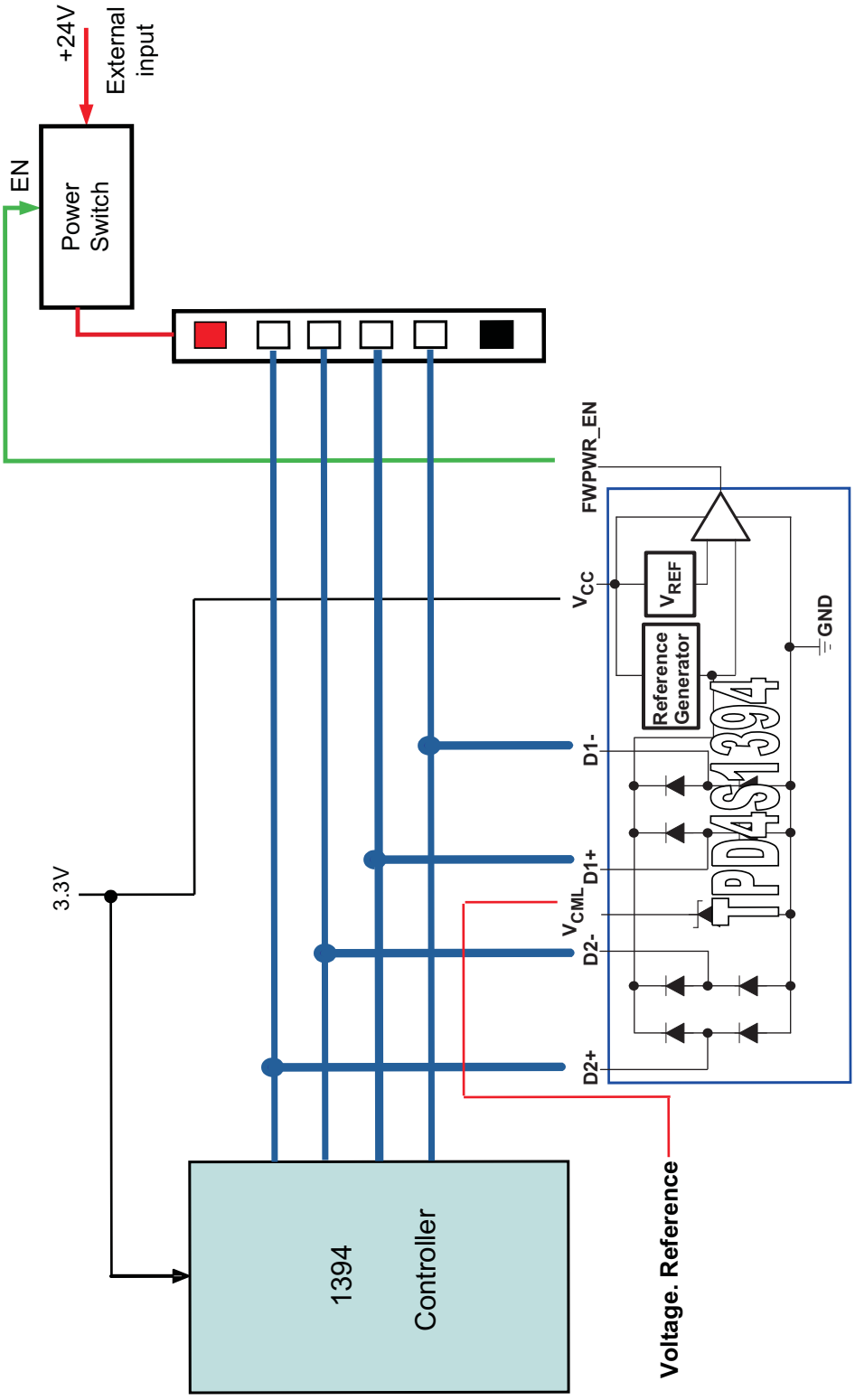

Figure 5. Application Diagram of TPD4S1394 with the 1394 Port Adapter

5 PCB Layout Consideration

It is important to have a good routing of the traces on the PCB to minimize capacitance for the Tp lines. The IEEE 1394 interface is not extremely high speed, but it is still beneficial to keep the above in consideration. Figure 6 shows the suggested PCB layout routing of the TPD4S1394 with respect to the connector and controller.

The data lines are connected in a way that there is no break of connectivity in the lines. The FWPWR_EN signal is a digital output and therefore there should be no issue of routing it under the layer to the system power switch control. The Vclmp pin is a NO Connect (only used as a test point/input) and hence its position is not critical. A 0.1µF decoupling capacitor is required to be connected on Vcc.

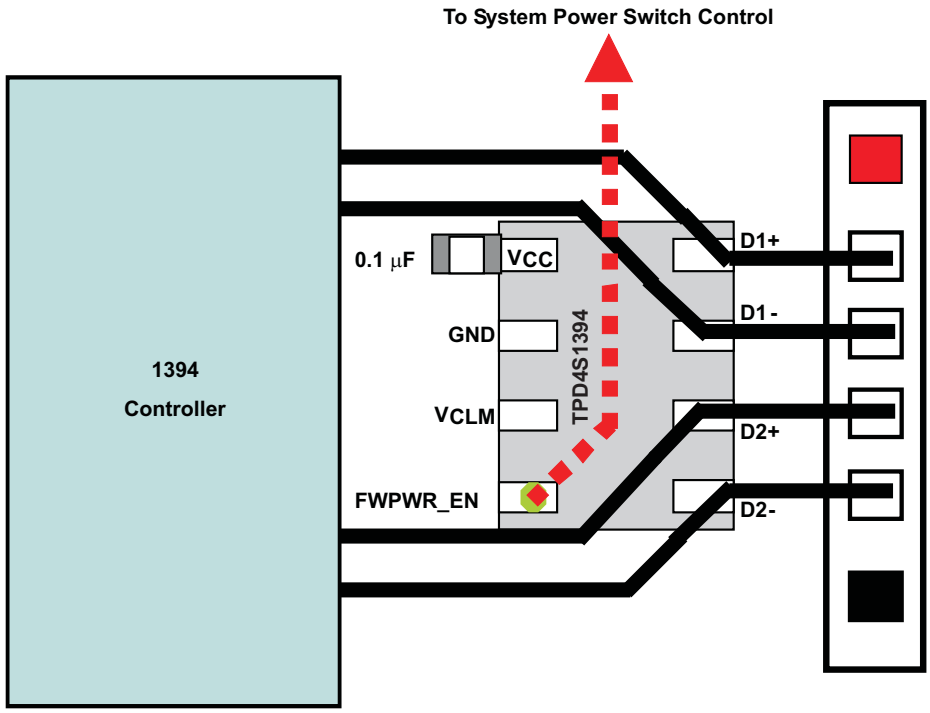

Figure 6. PCB Board Layout with TPD4S1394

6 Conclusion

The TPD4S1394 provides a robust solution to the EOS or late 'Vg' type event with the IEEE1394 lines. Though other means may be used to help guard against late-Vg (adding shielding, replacing older cables, or adding external components), the TPD4S1394 provides a simple and effective solution by turning off the switch which provides the path for the current to the Tp lines. With this solution, there is no chance of the Tp lines ever reaching such catastrophic voltage levels.

The TPD4S1394 also provides integrated ESD protection with a clamping voltage much lower than the absolute max for the protected device. This adds another level of protection if the response time of the switch is a little long. The above device can be used to protect IEEE1394 ports in laptops and desktops and other applications with IEEE1394 devices.

Visit www.ti.com for data sheets for all TPD type protection devices of Texas Instruments. For more info about late-Vg event and causes, refer to Application Note (SLEA072A).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265