Measuring the Thermal Performance of theTPS54620

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1 Abstract

The thermal management of printed-circuit boards is complex, but must be well understood to achieve optimum performance and reliability. SWIFT™ dc/dc converters in the 14-pin QFN package rely on an exposed lead frame die pad on the bottom of the package to provide an extremely low thermal resistance from junction to case. The junction to ambient thermal impedance, $R_{\theta JA}$ (formerly $\theta_{J\text{-}A}$), is greatly dependent on the printed circuit board design, orientation, and airflow; so, it is difficult to estimate the actual junction temperature of the converter IC without detailed computer simulation of the circuit board and its operating environment. A technique is demonstrated to measure actual junction temperatures of a device in a user's application circuit using the body diode of the PWRGD open drain output transistor. Using this information it is possible to accurately predict the junction to ambient thermal impedance of a given circuit.

2 Introduction

The 14-pin QFN package is used for the TPS54620 dc/dc converters. This device offer an output current of 6 A. As the power FETs are integrated into the device, the power dissipation can be high at output currents approaching the maximum of 6 A. Thermal management becomes an important factor in determining the performance and reliability of the design. The QFN package used by the TPS54620 is manufactured with the lead frame exposed on the under side of the package. This provides an extremely low thermal resistance between the integrated circuit die and the package. By soldering this exposed thermal pad on the device directly to the PCB, the heat generated can be drawn away from the device. Thermal vias located under the device can be used to channel the heat directly to internal ground planes or other heat sinking structures built into the PCB. Because the thermal impedance from the junction to the exposed thermal pad is very low, the junction to ambient thermal resistance is mainly dependent on the printed circuit board design. It is difficult to model the thermal performance of the printed circuit board without specific modeling software. It is possible, however, to estimate the junction temperature of the device from the voltage across the body diode of the PWRGD open drain output transistor when the transistor is biased with a fixed current .

3 Test Setup

The TPS54620EVM-374 circuit is used for this application report. The schematic diagram is shown inFigure 1.

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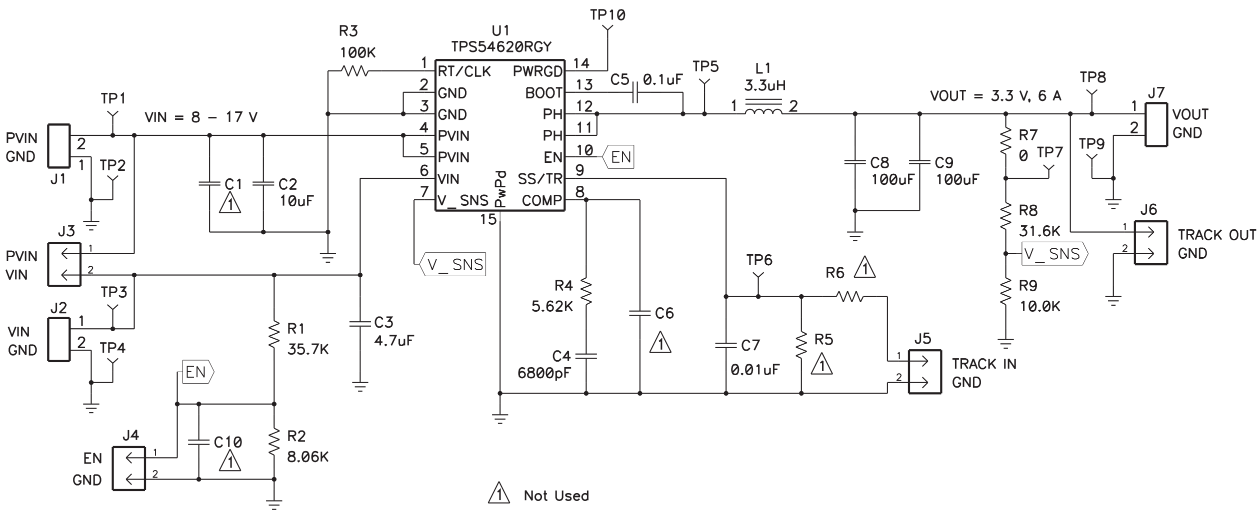

Figure 1. Electrical Schematic

To accurately measure the junction temperature of the device, it is possible to monitor the forward voltage drop of the internal drain-to-source body diode of the PWRGD open-drain FET. The diode is forward biased with a constant 300 μA current. This 300 μA bias current can be supplied by a current source or a voltage supply connected in series with a 10-kΩ resistor as shown in Figure 2 .

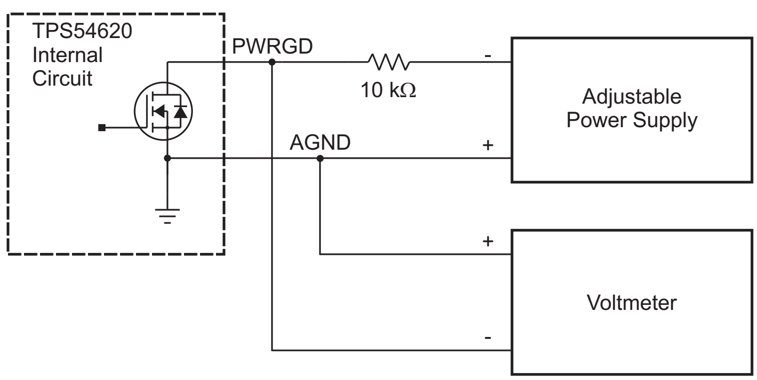

Figure 2. Test Setup

4 Body Diode Characterization

The first step in obtaining thermal data is to determine the diode forward voltage versus junction temperature characteristics. With no power applied to the VIN input PCB, measure the diode voltage at various ambient temperatures as shown in Table 1 .

Table 1. Diode Voltage vs Temperature

T_J-C°	Measured Diode Voltage-V
25	0.4609
50	0.4438
75	0.4265
100	0.4076
125	0.3863
150	0.3591

Plotting the data shows the linear relationship of the diode voltage to the junction temperature. A trend line can be used to easily determine the equation to express this relationship as shown in Figure 3 .

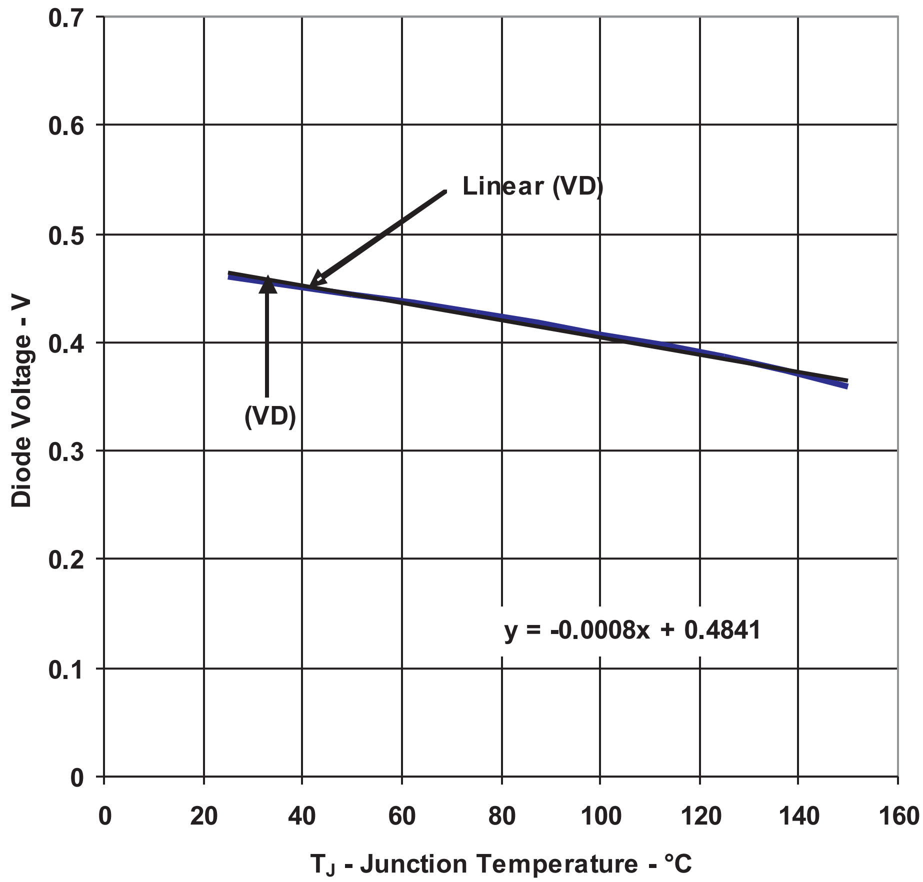

Figure 3. Diode Voltage vs Junction Temperature

The junction temperature as a function of diode voltage equation can easily be derived by rearranging terms in the trend line equation:

$$T_J = \frac{V_D - 0.4841}{0.0008} \tag{1}$$

5 Test Results

Now that the junction temperature to diode voltage characteristics are known, the thermal performance data can be taken and the junction to ambient thermal resistance can be calculated. At a known ambient temperature such as room ambient, it is necessary to calculate the device power dissipation and measure the diode voltage over the range of output currents. The test board was set up with 12-V input and 3.3-V output. Power dissipation was determined by measuring the input voltage, input current, output voltage and output current. Because the high- and low-side FETs are integrated into the devices, the only other significant power loss is the series resistance of the inductor. The device power dissipation is then given by:

$$P_{DISS} = (V_{IN} \times I_{IN}) - (V_{OUT} \times I_{OUT}) - (I^2_{OUT} \times R_{INDUCTOR}) \tag{2}$$

It is important to understand that these test PCBs contain only the power conversion circuitry. All load power is dissipated external to the PCB and does not contribute to the thermal measurements presented here.

Figure 4 shows the device power dissipation as a function of output current. For a given output current, the power dissipation is primarily due to the RDSon of the internal FET. For the TPS54620, the FET high-side on-resistance is nominally 26mΩ and the low-side is 19 mΩ.

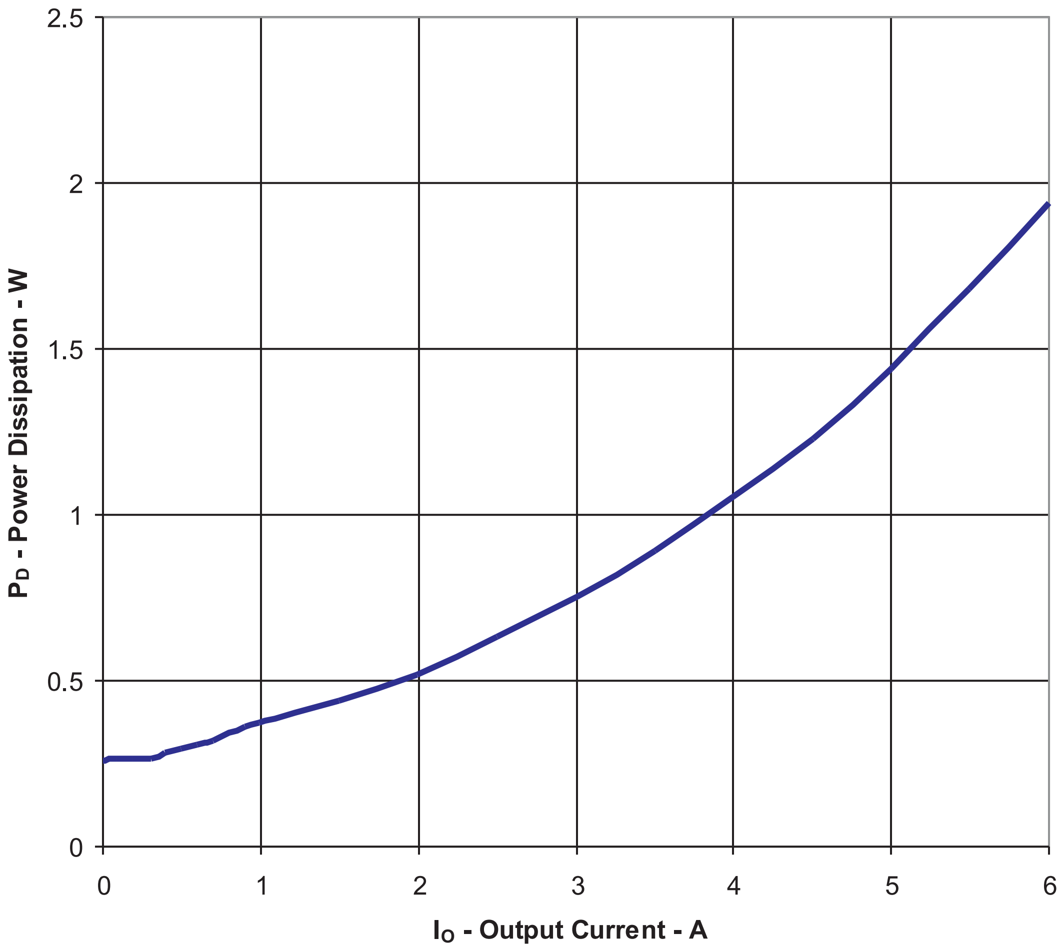

Figure 4. Device Power Dissipation vs Output Current

Figure 5 shows the junction temperature as a function of output current.

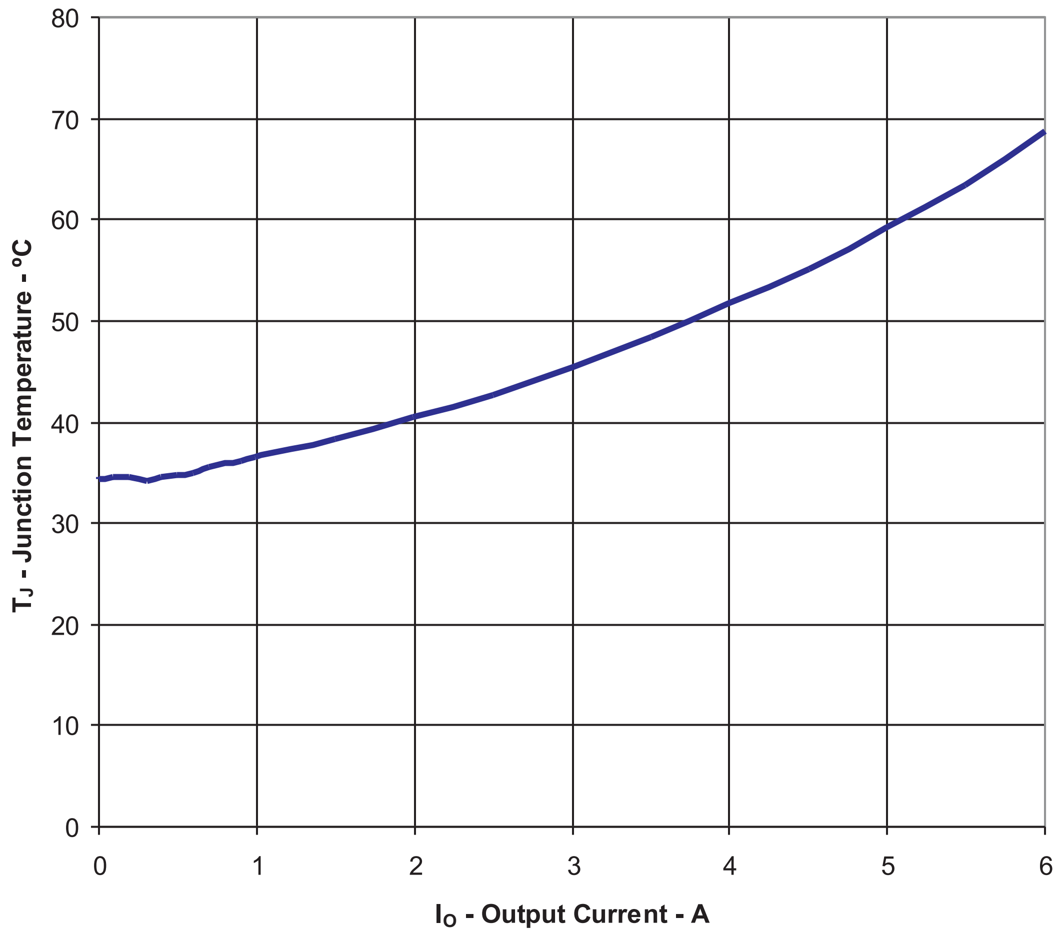

Figure 5. Device Junction Temperature vs Output Current

With the power dissipation and the junction temperature of the devices known, the thermal resistance $R_{\theta JA}$, can be determined. This parameter has the units of ºC/W; so, the device temperature rise is plotted vs power dissipation. This curve is shown in Figure 6.

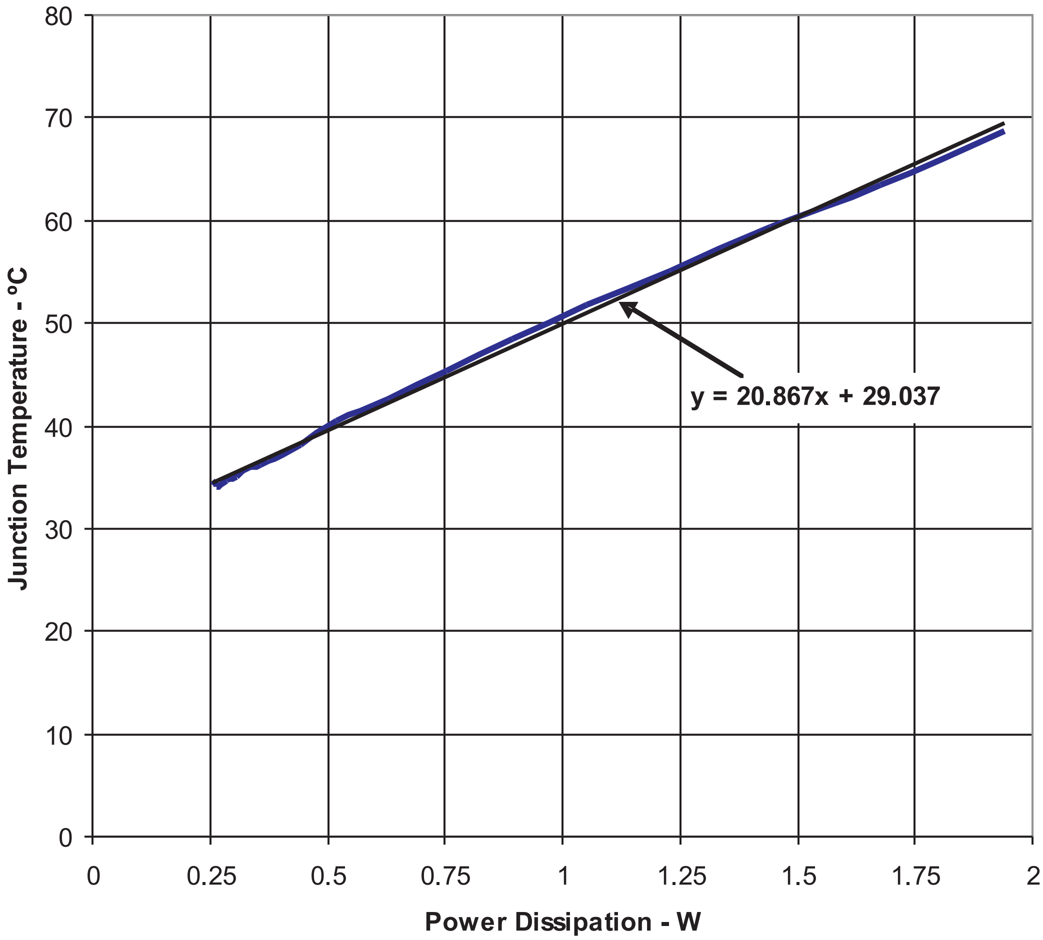

Figure 6. Junction Temperature Rise vs Device Power Dissipation

The junction temperature rise vs power dissipation curve is close to linear. The slope of this line, given by the coefficient of 20.867 in Figure 6, is the thermal resistance from junction to ambient.

6 Conclusion

For designs using the TPS54620 SWIFT device in the 14-pin QFN package, the thermal performance almost completely depends on the PCB design and layout. For optimal performance, always use the recommended footprint as provided in the device data sheets. Make sure that the device thermal pad is soldered to the exposed copper area under the device. Increasing the amount of copper area used for heat sinking and providing for airflow can improve the thermal performance, especially in high-current applications. It is important to understand that the test results presented in this application report are only valid for the PCB configurations described herein. Results in other application circuits will vary. In typical applications, the SWIFT dc/dc converter will likely be used as point of load power supply; the power dissipated at the load will contribute significantly to thermal performance as the heat dissipated by the load may be many times that dissipated in the SWIFT dc/dc converter. Using the technique described in this application report allows users to easily determine the thermal performance of their designs.

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