Application Report
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Designing a Split-Rail SEPIC With the TPS61175

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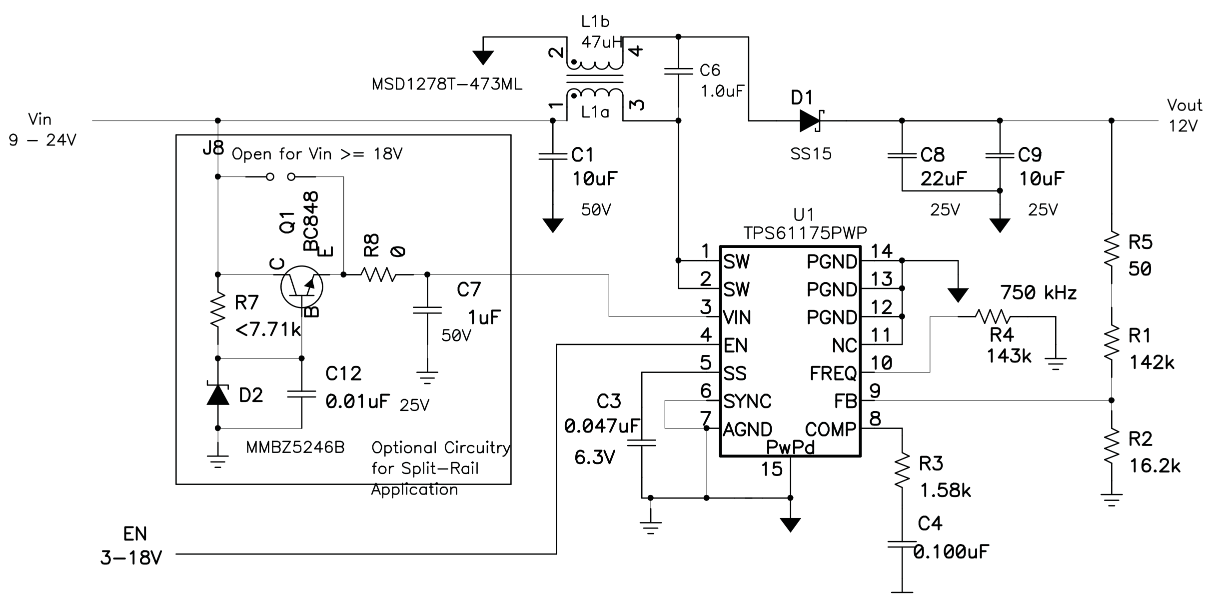
PMP-DC Low-Power DC/DC Converters

ABSTRACT

Often a regulated DC output voltage is needed between the minimum and maximum input voltages of a DC/DC converter, but neither a buck or boost converter in standard configurations is sufficient. However, a boost converter integrated circuit (IC) can be configured to drive a single-ended, primary inductor converter (SEPIC) power stage and provide an output voltage that is between the input voltage extremes. In addition, the user may want to extend the maximum input voltage range of the converter to limits beyond the absolute maximum of the IC.

1 Power Stage Design

The following design example can help a user design a 12-V power supply from a 9-V to 24-V input power source using the TPS61175 boost converter IC in the SEPIC configuration with split-rail capability. In order to simplify this report, only the SEPIC and discrete linear regulator design equations with minimal explanatory text are included. For more information on the SEPIC topology and its design equations, see application reports SLYT309 and SLVA337. More information is available on extending the input voltage range of a converter in application report SLVA338. shows the power supply circuit.



NOTE: This schematic excludes the reference designators of open component on the PR894E-1 PCB.

Figure 1. 12-V Power Supply From 9-V to 24-V Input Power Source

Table 1 gives the performance specifications for the reference design.

Table 1. Performance Specifications for the Reference Design

Parameter	Conditions	Min	Nom	Mac	Unit
Input and Ambient Characteristics					
V_{IN}		9	15	24	V

Table 1. Performance Specifications for the Reference Design (continued)

Parameter		Conditions	Min	Nom	Mac	Unit
f_S				750		MHz
T_A					55	°C
Output Characteristics						
V_{OUT}	Output voltage		11.5	12	12.5	V
	Load regulation	V_{IN} = 9 V, 10 mA < I_O < 800 mA			1%	DV_O/I_O
V_{RIPPLE}	Output voltage ripple	I_O = 800 mA			50	MVP
I_O	Output current		1		750	mA
η	Efficiency			90%		
Transient Response						
I_{TRAN}	Load step			325		mA
DV_{TRAN}	V_O undershoot			350		mV

Table 2 summarizes the design considerations for the passive components.

Table 2. Design Equations for Passive Components

SLYT309 Equation (Eq) Number	Design Equation and Computation	Selection
Eq 1	$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D}$ $D_{max} = \frac{12 + 0.5}{9 + 12 + 0.5} = 0.58$ $D_{min} = \frac{12 + 0.5}{24 + 12 + 0.5} = 0.34$	
Eq 2 with η_{EST}	$I_{IN(DC),MAX} = \frac{I_{OUT,MAX}}{\eta_{EST}} \times \frac{V_{OUT} + V_D}{V_{IN,MIN}} = \frac{0.75}{0.9} \times \frac{12 + 0.5}{9} = 1.16\ A$	MSD1278T-473ML, 47µH, I_{SAT}=1.45A, DCR=0.180 Ω
[(1)]Eq 3 where K_{IND}=0.2	$\Delta I_L = K_{IND} \times I_{IN(DC)MAX} = 0.20 \times 1.16A = 0.23\ A$	
Eq 4	$L_{1a} = L_{1b} \geq \frac{1}{2} \times \frac{V_{IN(MIN)} \times D_{(MAX)}}{\Delta I_{L(24V_{IN})} \times f_S} = \frac{1}{2} \times \frac{9 \times 0.58}{0.23 \times 750\ kHz} = 15.1\ \mu H$	
Eq. 5	$I_{L1a(PEAK)} = \frac{I_{IN(DC),MAX}}{\eta} \times \left(1 + \frac{K_{IND}}{2}\right) = \frac{1.16}{0.9} \times \left(1 + \frac{20\%}{2}\right) = 1.42\ A$	
Eq. 7	$C_{OUT} \geq \frac{I_{OUT} \times D_{(MAX)}}{\Delta V_{RPL} \times f_S} = \frac{0.75 \times 0.581}{50\ mVpp \times 750\ kHz} = 11.62\ \mu F$	C8=22 µF || C9=10µF, 25-V ceramic capacitors
NA	$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} = \geq \frac{0.250\ A}{2\pi \times 3\ kHz \times 0.5V} = 27\ \mu F$	
$DV_{Cp\text{-}PKPK}$ < 5%×Vo	$V_{Cp(MAX)} = V_{IN} + \frac{1}{2} \times \Delta V_{Cp\text{-}PKPK} = 24\ V + \frac{1}{2} \times 0.05 \times 12\ V = 24.3\ V$	
Eq 11	$C_P \geq \frac{I_{OUT} \times D_{(MAX)}}{\Delta V_{Cp\text{-}PKPK} \times f_S} \geq \frac{0.75A \times 0.581}{0.6V \times 750\ kHz} = 0.97\ \mu F$	C6 = 1 µF, 50V

(1) This customer application needed low current ripple and EMI, so a 47-µH inductor was selected.

Because ceramic capacitors with very low ESR and therefore very high RMS current ratings were used, the capacitor ripple current calculations were excluded in the preceding equations. In addition, the additional output voltage ripple caused by the capacitor's ESR was ignored. These calculations must be included if higher ESR capacitors are used.

Table 3 summarizes the design considerations for the active components.

Table 3. Design Equations for Active Components

SLYT309 Equation (Eq) Number	Design Equation and Computation	Selection
Figure 3	$V_{Q1(max)} = V_{IN(max)} + V_{OUT} = 24\text{ V} + 12\text{ V} = 36\text{V}$	U1 = TPS61175 with 38 V, 3-A peak FET and P_D = 0.9 W at T_A = 85°C
Eq 12	$I_{Q1(PEAK)} = I_{IN(DC),MAX} + I_{OUT,MAX} + \Delta I_L = 1.16\text{ A} + 0.75\text{ A} + 0.23\text{ A} = 2.14\text{ A}$	
Eq 14	$I_{Q1(RMS)} = \frac{I_{IN(DC),MAX}}{\sqrt{D_{max}}} = \frac{1.16}{\sqrt{0.58}} = 1.5\text{ A}$	
Eq 13	$P_{D\_Q1} = I^2_{Q1(RMS)} \times r_{DS(on)} \times D_{max} + I_{Q1(PEAK)} \times (V_{IN,MIN} + V_{OUT} + V_D) \times \frac{t_{Rise} + t_{Fall}}{2} \times f_{SW} = 1.5^2 \times 0.13 \times 0.581 + 2.14\text{ A} \times (9 + 12 + 0.5) \times \frac{10\text{ ns} + 10\text{ ns}}{2} \times 750\text{ kHz} = 0.52\text{ W}$	
NA	$V_{R(DIODE)} = V_{IN(max)} + V_{OUT} = 24\text{ V} + 12\text{ V} = 36\text{ V}$	D2 = B150B-13, 50 V, 1 A
NA	$P_{D(DIODE)} = I_{OUT(MAX)} \times V_D = 0.75\text{ A} \times 0.5\text{ V} = 375\text{ mW}$	

If using a converter with integrated FET like TPS61175, use this equation to quickly estimate I_{OUTmax}.

$$I_{OUT(MAX)} = \frac{I_{LIM}}{\left(\frac{V_{OUT} + V_D}{V_{IN(MIN)}}\right) \times \left(\frac{1 + K_{IND}}{\eta_{EST}}\right) + 1} = \frac{3A}{\left(\frac{12 + 0.5}{9}\right) \times \left(\frac{1 + 20\%}{0.9}\right) + 1} = 1.05\text{ A} \quad (1)$$

Table 4. Discrete Linear Regulator Passive Components

SLVA338 Equation (Eq) Number	Design Equation and Computation	Selection
Eq 4	$V_{Zmax} < V_{ICmax} = 18\text{V and } V_{Zmin} > V_{INmin} + V_{BEmax} = 2.9\text{ V} + 0.7\text{ V}$	D2 = MMBZ5246B, 16 V, 225 mW
Eq 5 using Q1=BC848 with h_{FEmin} = 200	$R_{1D} < \frac{V_{PWRmax} - V_{Zmax}}{I_Z + \frac{I_{Qmax}}{h_{FE}}} = \frac{24\text{ V} - 0.9 \times 18\text{ V}}{1\text{ mA} + \frac{2.3\text{ mA}}{200}} = 7.71\text{ k}\Omega$	R7 = 7.68 kΩ

Table 5 explains how the remaining components were chosen.

Table 5. Additional Components

Component	Rationale
C1 = 10 µF	$C_{IN(MIN)}$ per TPS61175 data sheet (SLVS892)
C3 = 0.047 µF	$C_{SS(MIN)}$ per TPS61175 data sheet (SLVS892)
R1 = 143 kΩ and R2 = 16.2 kΩ	Equation 7 per TPS61175 data sheet (SLVS892)
R4 = 143 kΩ for f_S = 750 kHz	Figure 13 of TPS61175 data sheet (SLVS892)
Q1 = BC848 30-V	Low-cost NPN transistor per (SLVA338)
C7 = 1.0 µF, 25 V	Minimum recommended input capacitor for split rail operation per (SLVA338)
C12 = 0.1 µF, 25 V	Minimum recommended base capacitor per (SLVA338)

2 Compensating the Control Loop (R3 and C4)

Figure 2 shows the measured results from the power stage transfer function's gain and phase at full load for $V_{IN(MIN)}$, in red and royal blue, and $V_{IN(MAX)}$, maroon and dark blue, respectively.

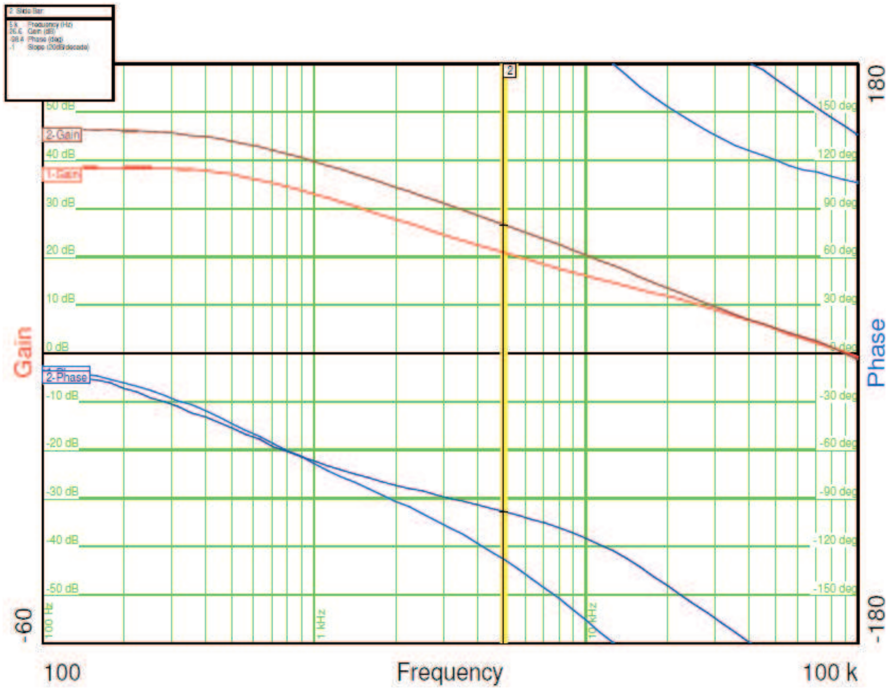


Figure 2. Measured Power Stage Gain and Phase with R3 = 1 kΩ and C4 = 1 µF

The lowest frequency right-hand plane zero (RHPZ) occurs at $V_{IN(MIN)}$ and is calculated in Equation 2.

$$f_{RHPZ} = \frac{1}{2\pi \times \frac{L_{1a}}{R_{OUT}} \times \left(\frac{D}{1\text{-}D}\right)^2} = \frac{1}{2\pi \times \frac{47\ \mu H}{16\ \Omega} \times \left(\frac{0.581}{1 - 0.581}\right)^2} = 28.2\ kHz \tag{2}$$

The bandwidth typically is set to $f_{BW} = f_{RHPZ}/10$; however, in this case, the RHPZ is fairly low, so f_{BW} is chosen to be 5 kHz. Therefore, the compensation gain, K_{COMP}, and power stage gain at the 5-kHz crossover frequency must be 0 dB, or $K_{COMP}(f_{BW}) + 20\log(G_{PW}(f_{BW})) = 0$ dB, so $K_{COMP}(f_{BW}) = -20\log(G_{PW}(f_{BW}))$ = -23 dB as illustrated by the yellow line in Figure 2. Using Type II compensation and finding G_{EAmax} = 440 µmho in the data sheet, Equation 3 computes the value of R3 to give $K_{COMP}(f_{BW}) = -23$ dB, rounded up to the closest standard value.

$$R3 \cong \frac{10^{\frac{K_{COMP}(f_{BW})}{20\ dB}}}{G_{EA(MAX)} \times \frac{R2}{R2 \times R1}} = \frac{10^{\frac{-23\ dB}{20\ dB}}}{440\ \mu mho \times \frac{16.2\ k\Omega}{16.2\ k\Omega + 143\ k\Omega}} = 1.58\ k\Omega \tag{3}$$

With $f_Z \approx f_{BW}/5$ = 1 kHz, C4 is solved for in Equation 4.

$$C4 \cong \frac{1}{2\pi \times R3 \times f_Z} = \frac{1}{2\pi \times 1.58\ k\Omega \times 1\ kHz} = 100\ nF \tag{4}$$

Figure 3 shows the measured loop gain and phase. The measured f_{BW} is centered around 5 kHz for both $V_{IN(MIN)}$, in red and royal blue, and $V_{IN(MAX)}$, in maroon and dark blue, and the phase margin is near 60° for both cases.

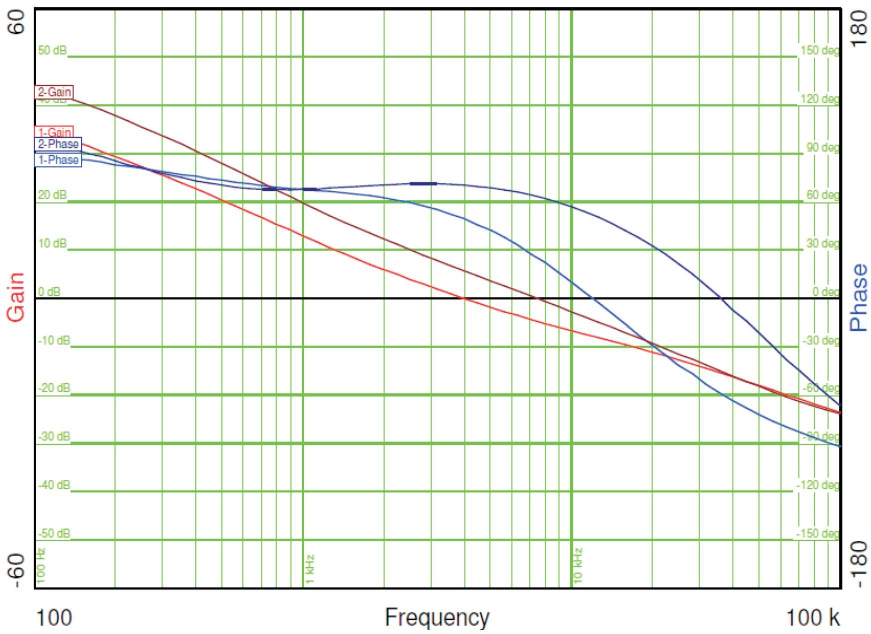


Figure 3. Measured Total Loop Gain and Phase With R3 = 1.58 kΩ and C4 = 0.100 µF

Figure 4 shows the transient response for a 325-mA load step. The DV_{TRAN} droop of 350-mV is below the 400-mV design specification.

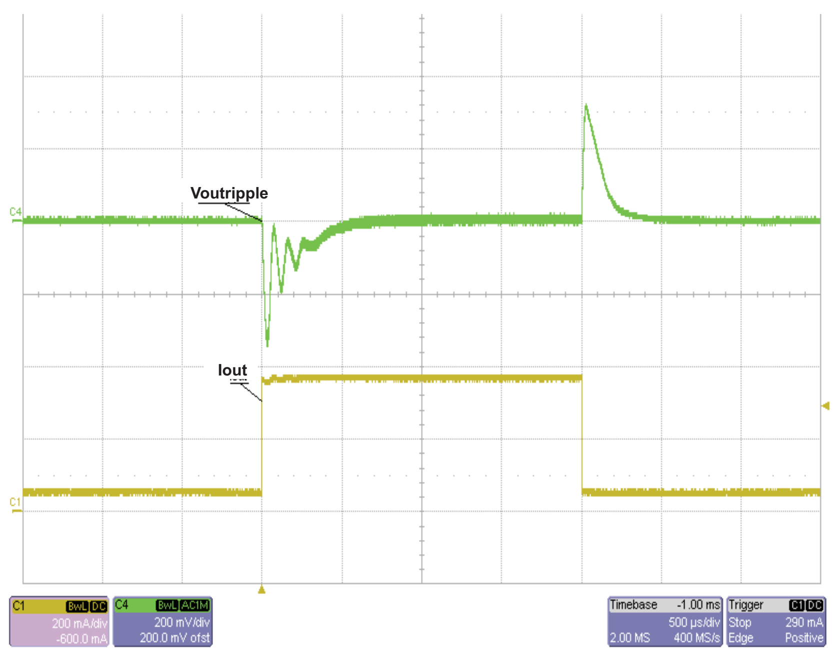


Figure 4. Load Transient Response With V_{IN} = 9 V and I_{OUT} = 50 mA to 375 mA

Figure 5 shows the efficiency.

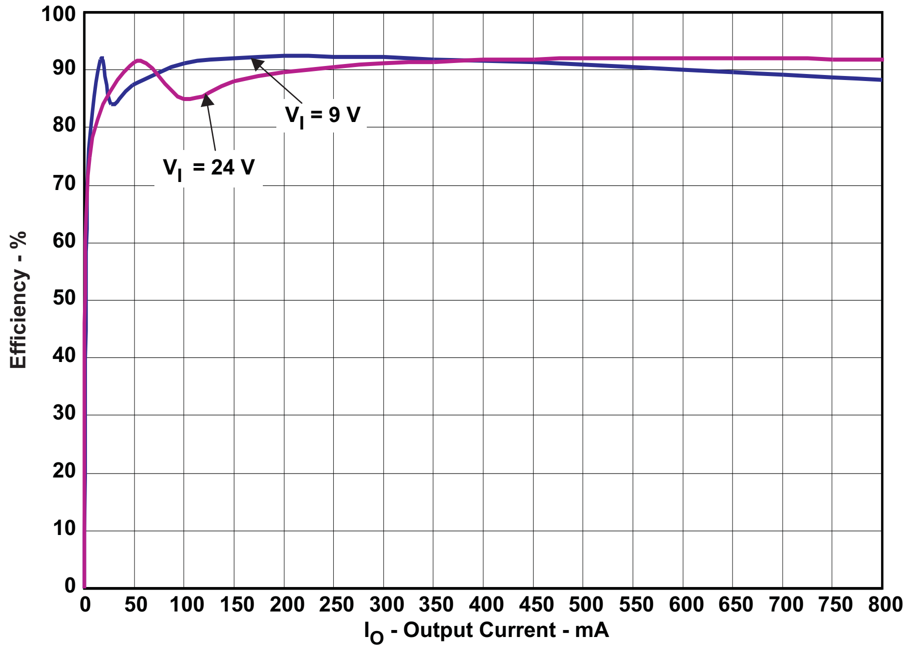


Figure 5. Efficiency

Figure 6 shows the load regulation, well within the 1% specification.

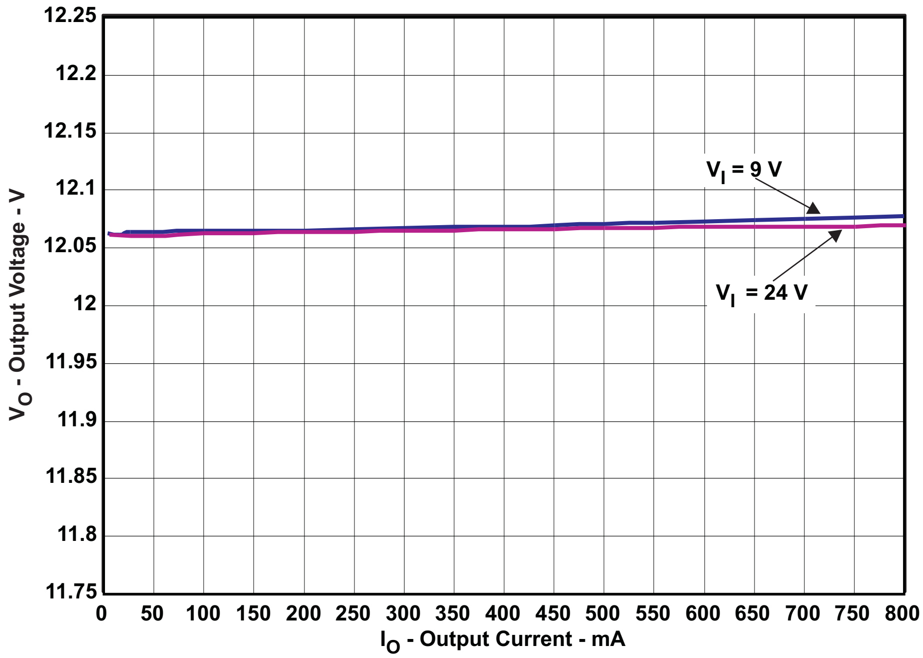


Figure 6. Load Regulation

Figure 7 and Figure 8 show the typical operating waveforms.

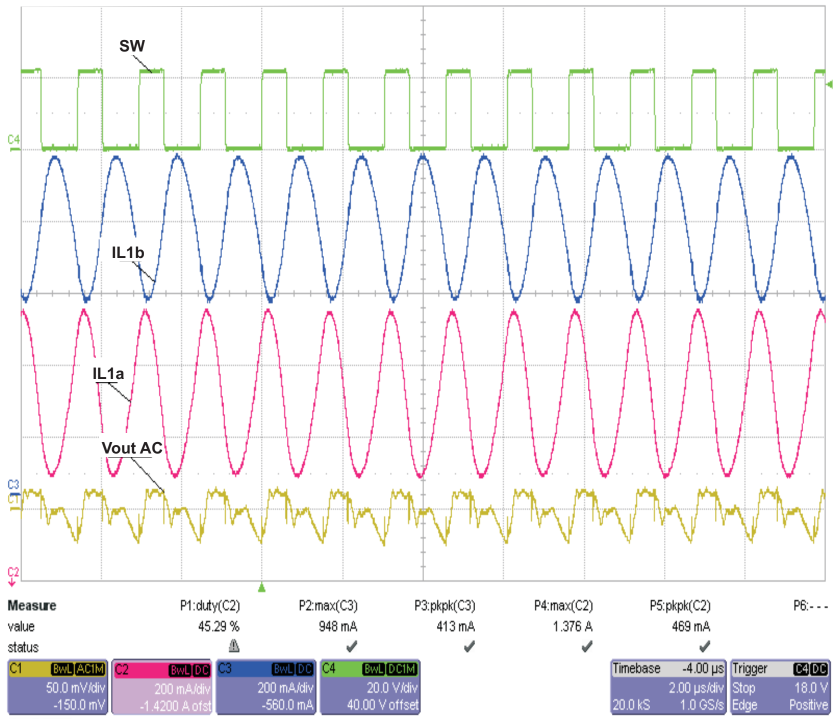


Figure 7. Operation Including V_{RIPPLE} at V_{IN} = 9 V and I_{OUT} = 750 mA

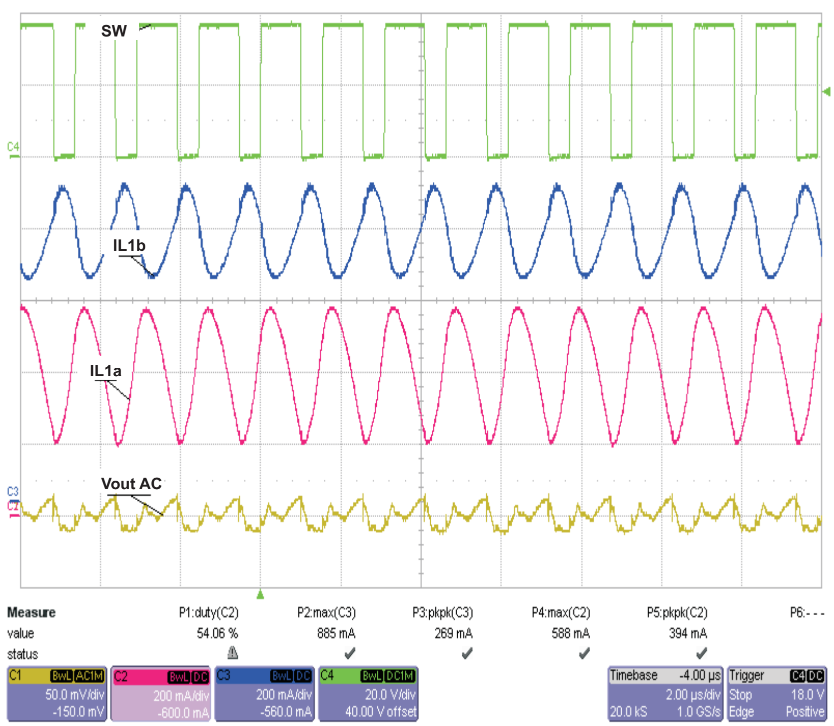


Figure 8. Operation Including V_{RIPPLE} at V_{IN} = 24 V and I_{OUT} = 750 mA

Figure 9 shows the start-up waveform.

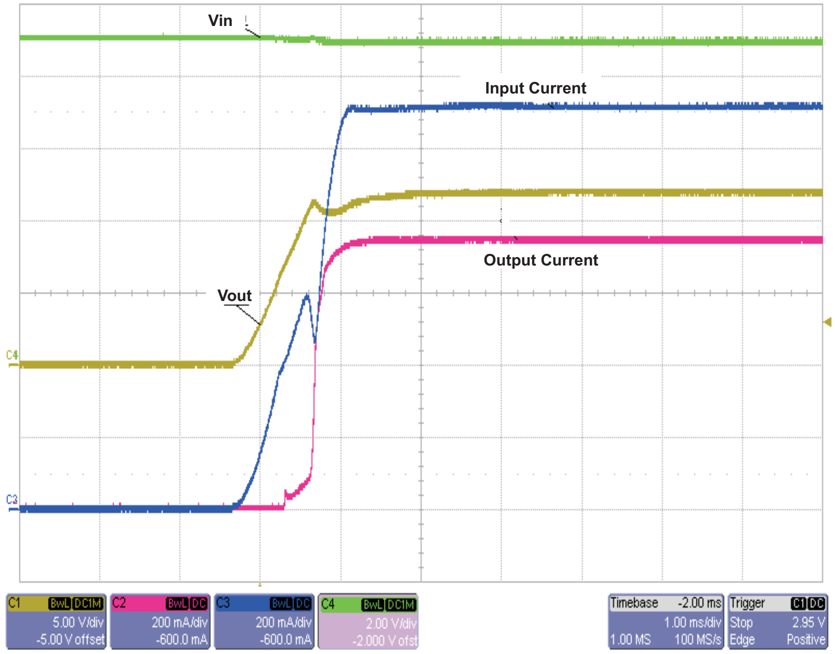


Figure 9. Start-up at V_{IN} = 9 V and I_{OUT} = 750 mA

In a SEPIC configuration, if the input voltage to the IC and V_{ENABLE} is separated from the power stage, careful attention must be paid to the order in which power is applied. If V_{IN} and V_{ENABLE} are applied to the IC, but no power is flowing to the power stage, the device drives to maximum duty cycle. Once power is supplied to the circuit, switching does not occur and the input current is unregulated. This can lead to device damage if the supply current is not limited.