Application Report
SLVA376–DECEMBER 2009

Powering OMAP™35x With TPS65073: Design-In Guide

PMP - Catalog Power Mgmt Units

ABSTRACT

This document details the design considerations of a power management unit solution for the OMAP™35x processor using the TPS65073 device.

Contents

List of Figures

List of Tables

1 Introduction

The OMAP35x Applications Processors have a diverse set of power management features which potentially enable lower cost power solutions based on the application. This design-in guide describes a power solution based on the TPS65073 (or TPS650731) device. This guide can be used to evaluate this solution, or help make decisions when designing an application using this solution. Note that throughout this document, the term TPS65073 is used to describe the functionality in both the TPS65073 and TPS650731. When the functionality differs between the two, the text mentions each device separately.

2 Power Requirements and Features of OMAP35x

A TPS65073-based power solution can power any device in the OMAP35x family (OMAP3503, OMAP3515, OMAP3525, and OMAP3530). The following section describes the specifications and power management features of these devices.

2.1 Power Specifications

The following tables detail the power requirements for each OMAP35x device that is supported by a TPS65073-based power solution. Note that the only difference in power lies in the amount of current required by the VDD_CORE and VDD_MPU_IVA voltage rails. Otherwise, the specifications are identical.

Table 1. OMAP3503 Power Specifications

	POWER RAIL	VOLTAGE	TOLERANCE	I_{MAX} (mA)	SEQUENCING ORDER
Core	VDD_MPU	0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)	±5%	680	4
Core	VDD_CORE	0.95 V, 1 V, 1.15 V (1)	±5%	320	3
I/O	VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM	1.8 V	±5%	147	1
I/O	VDDS_DPLL_PER, VDDS_DPLL_DLL	1.8 V	±5%	40	2
I/O	VDDA_DAC	1.8 V	±5%	65	After reset
I/O	VDDS_MMC1, VDDS_MMC1A	1.8 V	±5%	22	After reset (see MMC Boot section for more information)
		3 V	±10%		
The preceding power numbers assume that SmartReflex™ AVS is implemented.					

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values

Table 2. OMAP3515 Power Specifications

	POWER RAIL	VOLTAGE	TOLERANCE	I_{MAX} (mA)	SEQUENCING ORDER
Core	VDD_MPU	0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)	±5%	680	4
Core	VDD_CORE	0.95 V, 1 V, 1.15 V (1)	±5%	433	3
I/O	VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM	1.8 V	±5%	147	1
I/O	VDDS_DPLL_PER, VDDS_DPLL_DLL	1.8 V	±5%	40	2
I/O	VDDA_DAC	1.8 V	±5%	65	After reset
I/O	VDDS_MMC1, VDDS_MMC1A	1.8 V	±5%	22	After reset (see MMC Boot section for more information)
		3 V	±10%		
The preceding power numbers assume that SmartReflex™ AVS is implemented.					

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

Table 3. OMAP3525 Power Specifications

	POWER RAIL	VOLTAGE	TOLERANCE	I_{MAX} (mA)	SEQUENCING ORDER
Core	VDD_MPU_IVA	0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)	±5%	1140	4
Core	VDD_CORE	0.95 V, 1 V, 1.15 V (1)	±5%	330	3
I/O	VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM	1.8 V	±5%	147	1
I/O	VDDS_DPLL_PER, VDDS_DPLL_DLL	1.8 V	±5%	40	2
I/O	VDDA_DAC	1.8 V	±5%	65	After reset
I/O	VDDS_MMC1, VDDS_MMC1A	1.8 V	±5%	22	After reset (see MMC Boot section for more information)
		3 V	±10%		
The preceding power numbers assume that SmartReflex™ AVS is implemented.					

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

Table 4. OMAP3530 Power Specifications

	POWER RAIL	VOLTAGE	TOLERANCE	I_{MAX} (mA)	SEQUENCING ORDER
Core	VDD_MPU_IVA	0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)	±5%	1140	4
Core	VDD_CORE	0.95 V, 1 V, 1.15 V (1)	±5%	433	3
I/O	VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM	1.8 V	±5%	147	1
I/O	VDDS_DPLL_PER, VDDS_DPLL_DLL	1.8 V	±5%	40	2
I/O	VDDA_DAC	1.8 V	±5%	65	After reset
I/O	VDDS_MMC1, VDDS_MMC1A	1.8 V	±5%	22	After reset (see MMC Boot section for more information)
		3 V	±10%		
The preceding power numbers assume that SmartReflex™ AVS is implemented.					

(1) See the latest OMAP35x Operating Condition Addendum for the most current voltage values.

2.2 Power-Up Sequencing

Figure 1 shows the power-up sequencing requirements of OMAP35x. The description of the power-up sequence follows.

1. VDDS_WKUP_BG, VDDS_MEM, VDDS, and VDDS_SRAM are all 1.8-V rails and are tied to the same power supply. These are ramped first, ensuring a valid level on the I/O domain.
2. During the entire power-up sequence, the power-on-reset signal SYS_NRESPWRON must be held low until all rails and clocks are stable.
3. Both the 32-kHz and the high-frequency clock need to start oscillating and be stable.
4. After 1.8 V is stabilized, VDD_CORE can start ramping.
5. After VDD_CORE is stabilized, VDD_MPU_IVA can start ramping.
6. After 1.8 V is stabilized, VDDS_DPLL_DLL and VDDS_DPLL_PER (rails are tied to the same power supply) can ramp during or after VDD_CORE and VDD_MPU_IVA ramp.
7. After all of the preceding power rails have stabilized, and 32-kHz and the high-frequency clock have stabilized, then SYS_NRESPWRON can be released.
8. Other power supplies, such as VDDS_MMC1, VDDS_MMC1A, VDDS_DAC, etc., can be turned on or off depending on the application.

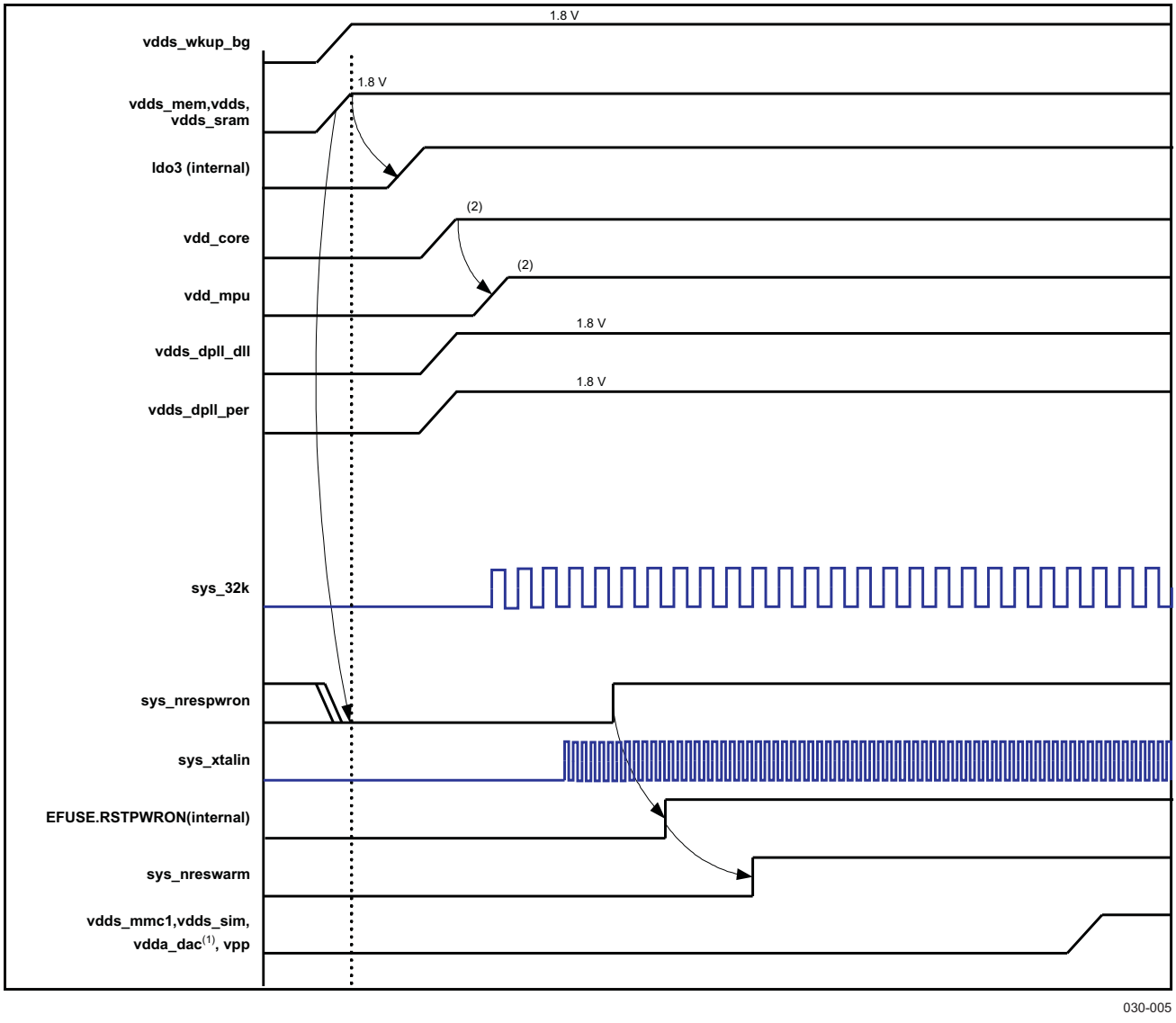

Figure 1. OMAP35x Power-Up Sequencing Requirements

2.3 Power-Down Sequencing

When using the TPS65073 power solution, power down is achieved by setting POWER_ON input to 0. When this occurs, all voltages ramp down at the same time, and the ramp rate of each voltage is generally determined by the load on that voltage.

During power down, all signals driving OMAP35x should have a voltage level equal or less than the I/O voltage of OMAP35x to avoid driving pins that are unpowered.For example, the schematic example of Figure 2 shows the 32-kHz clock gated by a 1.8-V Power Good signal. This ensures that this clock circuit does not drive the OMAP35x input clock pins when the 1.8 V is removed from OMAP35x.

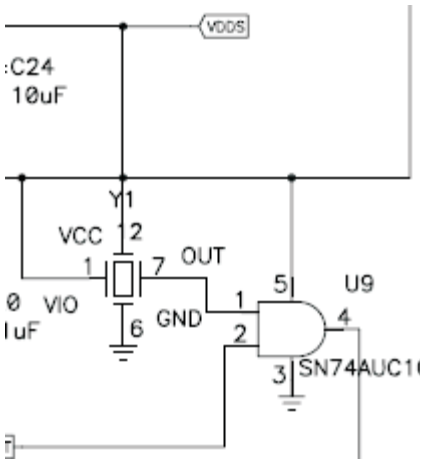

Figure 2. 32-kHz Clock Circuitry

2.4 OMAP35x Power Management Features

The OMAP35x Application Processors have a rich set of features that make aggressive power optimizations feasible in a user application. These features include DVFS (dynamic voltage frequency scaling) and SmartReflex™ AVS (adaptive voltage scaling). Both of these features allow for the lowest power operation depending on the OMAP35x processing requirements. In short, DVFS allows the user to change between the OMAP35x's operating points (voltages) depending on the device's operating frequency. Depending on the application, it may be necessary to move among these voltage levels during operation to reduce power consumption. SmartReflex™ AVS optimizes each of these operating points based on wafer process differences, temperature, and silicon degradation.

2.4.1 Dynamic Voltage and Frequency Scaling (DVFS)

DVFS is a power management technique used while active processing is going on in the system-on-chip (SoC). This technique matches the operating frequency of the hardware to the performance requirement of the active application scenario. Whenever clock frequencies are lowered, operating voltages can be lowered as well to achieve power savings. OMAP35x supports this technique on VDD_MPU_IVA and VDD_CORE power rails by defining discrete voltage values for these power rails and the accompanying maximum clock frequencies allowed for the modules supplied by those power rails. Each operating voltage and accompanying maximum clock frequency specification is called an operating performance point (OPP). The following tables show the OPP definitions for VDD_MPU_IVA and VDD_CORE.

Table 5. VDD_MPU_IVA Operating Performance Points

PROCESSOR OPP	VDD_MPU_IVA	ARM Maximum MHz
5	1.35	600
4	1.27	550
3	1.20	500
2	1.00	250
1	0.95	125

Table 6. VDD_CORE Operating Performance Points[(1)]

INTERCONNECT/ PERIPHERALS OPP	VDD_CORE	L3 Maximum MHz
3	1.15	166
2	1.00	100
1	0.95	41.5

(1) Refer to the latest OMAP35x Operating Condition Addendum for the most current voltage and frequency values

A TPS65073 power solution supports DVFS for OMAP35x by meeting the requirements shown in Table 7.

Table 7. TPS65073 Power Solution Support for DVFS

Power IC Requirement for DVFS	Does TPS65073 based power solution implement the requirement?	Does TPS650731 based power solution implement the requirement?
Support all five DVFS voltage values (0.95 V, 1 V, 1.2 V, 1.27 V and 1.35 V) defined for VDD_MPU_IVA	**Yes**. TPS65073 DC/DC3 supports full voltage range and can adjust in 25-mV increments	**Yes.** TPS650731 DCDC3 supports full voltage range and can adjust in 25mV increments
Support all three DVFS voltage values (0.95 V, 1 V, and 1.15 V) defined for VDD_CORE	**Yes.** Yes. TPS65073 DC/DC2 supports full voltage range and can adjust in 25-mV increments.	**Yes.** TPS650731 DCDC2 supports full voltage range and can adjust in 25mV increments.
I2C™ interface for setting output voltage to any of the values defined for DVFS	**Yes.** TPS65073 supports full speed I2C bus available for controlling voltage output for all DC/DCs and LDOs.	**Yes.** TPS650731 supports full speed I2C bus available for controlling voltage output for all DC/DCs and LDOs.

2.4.2 SmartReflex™ Adaptive Voltage Scaling (AVS)

AVS is a power management technique that can be used to refine system power consumption at a given OPP. The DVFS technique defines safe voltages for the OPPs so that all manufactured devices can meet the maximum frequency specifications for the OPPs. However, the silicon manufacturing process yields a distribution of devices, some (called strong or hot devices) of which can meet the frequency specifications at lower operating voltages than the conservative values defined by DVFS. SmartReflex™ AVS has been implemented by Texas Instruments to continuously adapt the operating voltage to the process properties of individual devices in order to maximize power savings for active scenarios. The OMAP35x integrates specialized hardware to enable SmartReflex™ AVS on VDD_MPU_IVA and VDD_CORE. This special hardware can be used to implement Class-3 or Class-2 SmartReflex™.

- **Class-2 SmartReflex™:** The special hardware monitors real-time performance; small software loop runs on ARM processor to change voltage whenever necessary.
- **Class-3 SmartReflex ™**: The special hardware has a dedicated hardware loop to dynamically monitor performance and adjust voltage without ARM processor intervention.

Equivalent power savings can be achieved with either implementation.

A TPS65073 power solution supports SmartReflex™ for OMAP35x by meeting the requirements shown in Table 8. See the Enabling Class 2 SmartReflex section for more implementation details.

Table 8. TPS65073 Power Solution for SmartReflex™ Implementation

Power IC Requirement for SmartReflex™ Implementation	Does TPS65073- or TPS650731-based power solution implement the requirement?	Does TPS650731-based power solution implement the requirement?
High-speed (or full-speed) I2C bus for setting output voltage	**Yes.** FS I2C bus available.	**Yes.** FS I2C bus available.
Voltage programmability in steps over the range 0.8 V to 1.35 V.	**Yes.** Can scale the output voltage between 0.725 V to 1.6 V with voltage steps down to 2 5mV.	**Yes.** Can scale the output voltage between 0.725 V to 1.6 V with voltage steps down to 25 mV.
(For Class-3 SmartReflex™) Ability to effect voltage change with a single I2C register write	**Yes.** TPS65073 can change voltage with one I2C write. However, this precludes the use of other functions (battery charger, touchscreen) on the TPS65073	**Yes.** TPS650731 can change voltage with one I2C write. However, this precludes the use of other functions (battery charger, touchscreen) on the TPS650731
(For Class-2 SmartReflex™) Ability to effect voltage change with a sequence of one or more I2C register writes	**Yes.** TPS65073 can change any DCDC or LDO with a single I2C write.	**Yes.** TPS650731 can change any DCDC or LDO with a single I2C write.
Slew rate between 4 mV/µs and 16 mV/µs	**Yes.** TPS65073 supports multiple slew rates, including 7.2 mV/µs and 0.45 mV/µs selectable in DEFSLEW register.	**Yes.** TPS650731 supports multiple slew rates, including 7.2 mV/us or 0.45 mV/us using the DEFSLEW register.

2.4.3 Static/Standby Leakage Management (SLM)

Static/standby leakage management (SLM) is the combination of techniques used to achieve the lowest power consumption during system idle time, when a system-on-chip (SoC) performs no useful processing. The OMAP35x supports various options for low-power standby states that trade-off level of power savings with speed of wakeup latency. The level of power savings during standby is determined by whether internal memories and logic are retained or powered down, whether clocks are on or off, and whether external voltage regulators maintain an on or off state.

Several SLM features are built into the OMAP35x architecture to enable low-power standby modes. In addition, OMAP35x supports features for achieving further standby power savings by putting system components external to the OMAP™ SoC into lower power states. Notable among these are control signals for gating external clock and power sources.

- SYS_CLKREQ is a signal used to gate the high-frequency clock when it is not needed. The OMAP35x can be set up to automatically deassert the sys_clkreq in full-chip retention and/or off modes.
- SYS_OFF_MODE is a signal used to indicate to external voltage regulators when they can be shut down.

OMAP35x supports a standby mode called off-mode, which is the lowest power state from which the device can wake up autonomously. In OMAP35x off-mode, system state is saved in external memory that can be put into self-refresh mode, most of the SoC is off, but a small wakeup domain stays powered on and operational at 32 kHz to monitor for wakeup events. The sys_clkreq is used to sequence an external clock source, while the sys_off_mode signal is used to sequence power during transitions into and out of the off-mode. The ability to shut off most of the external voltage supplies in this off-mode saves additional power dissipation in the voltage regulators. Alternatively to using the sys_off_mode pin, OMAP35x supports I2C commands for VDD_MPU_IVA and VDD_CORE sequencing during off-mode transitions.

A TPS65073 power solution supports OMAP35x SLM by meeting the requirements shown in Table 9.

Table 9. TPS65073 Power Solution Support for SLM

Power IC Requirement for SLM	Does TPS65073-based power solution implement the requirement?	Does TPS650731 based power solution implement the requirement?
Ability to gate high-frequency clock source with IO signal for standby power savings	**Yes.** Can be facilitated in hardware with SYS_CLKREQ. See High Frequency Clock Circuit.	**Yes.** Can be facilitated in hardware with SYS_CLKREQ. See High Frequency Clock Circuit.
(For SLEEP mode) Ability to lower voltage on VDD_MPU_IVA power source to lowest OPP via I2C	**Yes.** Supports I2C register write to to lower voltage to OPP1.	**Yes.** Supports I2C register write to to lower voltage to OPP1.
(For SLEEP mode) Ability to lower voltage on VDD_CORE power source to lowest OPP via I2C	**Yes.** Supports I2C register write to lower voltage to OPP1.	**Yes.** Supports I2C register write to lower voltage to OPP1.
(For OFF mode) Ability to turn off/on VDD_MPU_IVA power source with SYS_OFF_MODE signal or a single register write to the power IC over I2C	**Yes.** Supports SYS_OFF_MODE signal to turn on/off VDD_MPU_IVA and VDD_CORE power.	**No.** TPS650731 does not support use of SYS_OFF_MODE to individually enable/disable of VDD_MPU_IVA.
(For OFF mode) Ability to turn off/on VDD_CORE power source with SYS_OFF_MODE signal or a single register write to the power IC over I2C	**Yes.** Supports SYS_OFF_MODE signal to turn on/off VDD_MPU_IVA and VDD_CORE power.	**No.** TPS650731 does not support use of SYS_OFF_MODE to individually enable/disable of VDD_CORE power

3 TPS65073 Design-In Considerations

Figure 3 is a block diagram of a complete power solution example using the TPS65073 or TPS650731 device to power OMAP™35x. The remainder of the section details a more specific power solution.

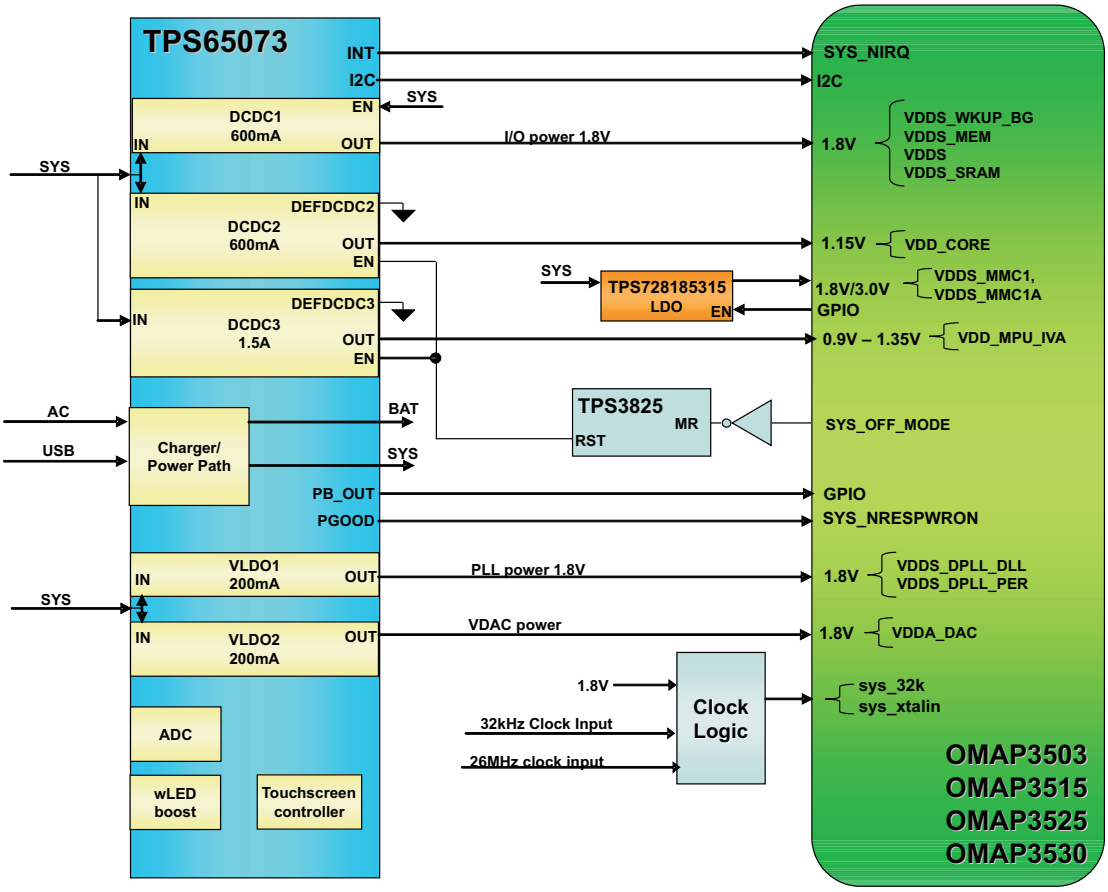

Figure 3. TPS65073 Power Solution Block Diagram

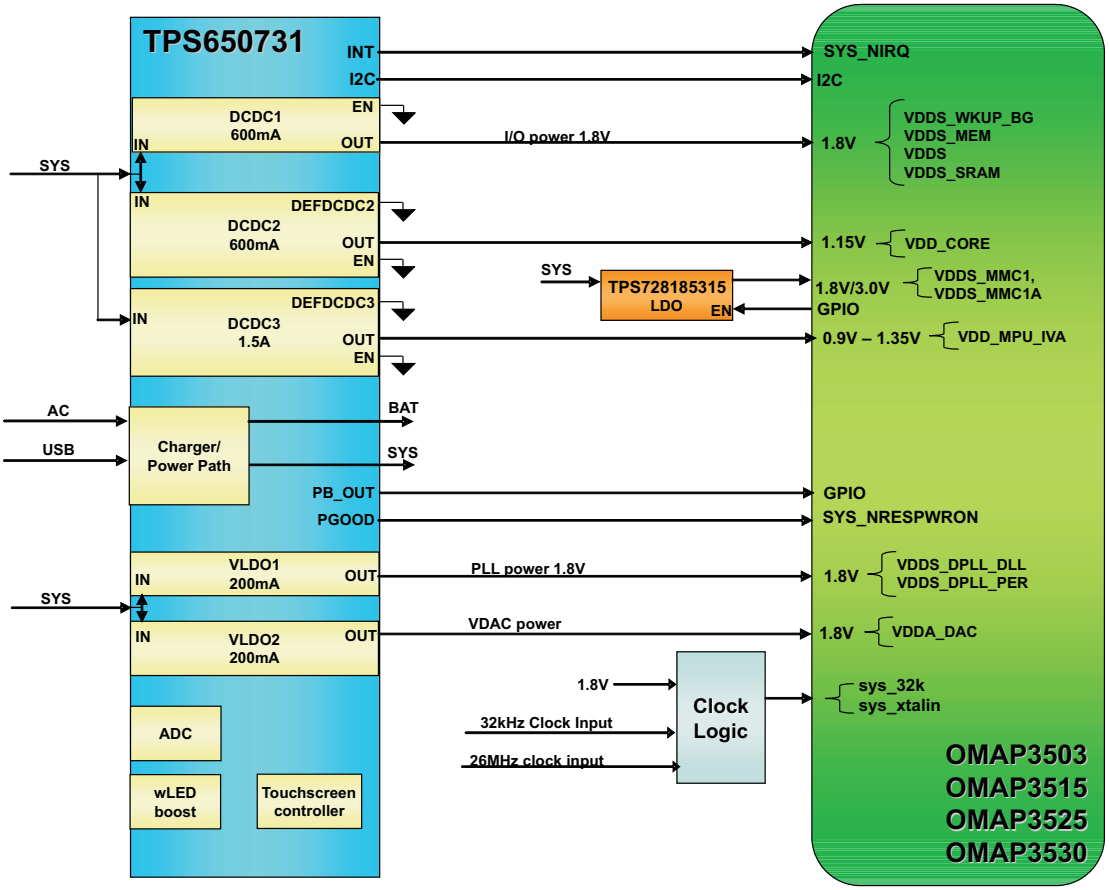

Figure 4. TPS650731 Power Solution Block Diagram

3.1 Reset

3.1.1 SYS_nRESPWRON Rise Time

The OMAP35x data sheet states that the maximum rise/fall time for SYS_nRESPWRON is 10 ns (see the following highlighted sections extracted from data sheet tables).

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AH25	NA	sys_nrespwron0	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS

.

In order to meet this requirement, a push-pull output buffer is required, with rise/fall time of <10 ns.

The TPS65073 PGOOD output is open drain and requires a buffer or gate with a fast rise time to meet the OMAP™35x requirement. If multiple reset sources are needed, use an AND gate as shown in Figure 5 to provide fast rise time for all reset sources.

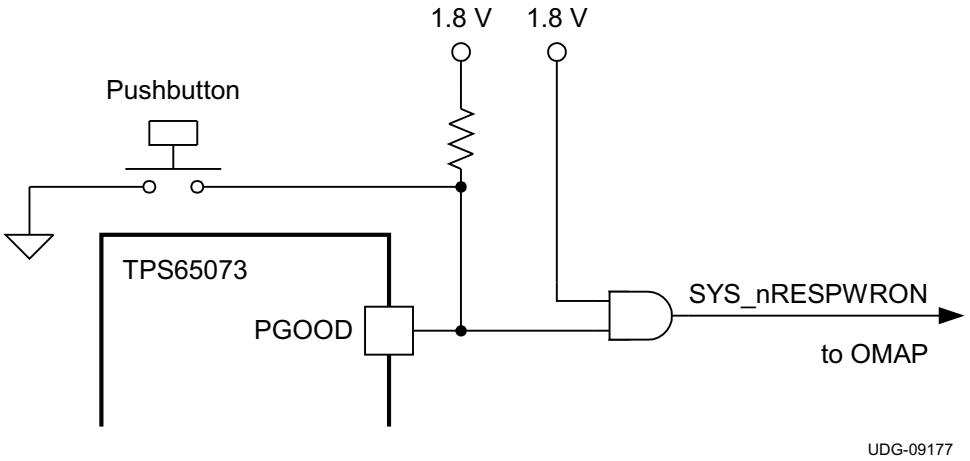

Figure 5. Circuitry to Combine Multiple Reset Sources

3.1.2 SYS_nRESPWRON Timing

Typical 32-kHz oscillators on the market may require up to a 1 second maximum time to stabilize. This poses a challenge in the power up sequencing in that the reset signal must be maintained low throughout this stabilization time in order to properly reset OMAP35x. The TPS65073 PGOOD output includes a 400-ms delay from the time the voltage sources are stable until the PGOOD signal transitions high. The PGOOD signal depends on the sources defined PGOODMASK in TPS65073 (the default sources are DCDC1, DCDC2 and DCDC3).

If a further delay is required for the reset signal, there are two options:

- Use the THRESHOLD and RESET signals of the TPS65073 to double the delay time of the reset to OMAP35x. The THRESHOLD input is compared to a 1-V reference. Once this threshold is met, the RESET output transitions high after a 400-ms delay. Thus, with the delay of 400 ms for the PGOOD output, total delay of 800 ms in SYS_nRESPWRON can be created to further extend the time needed to stabilize (see Figure 6).

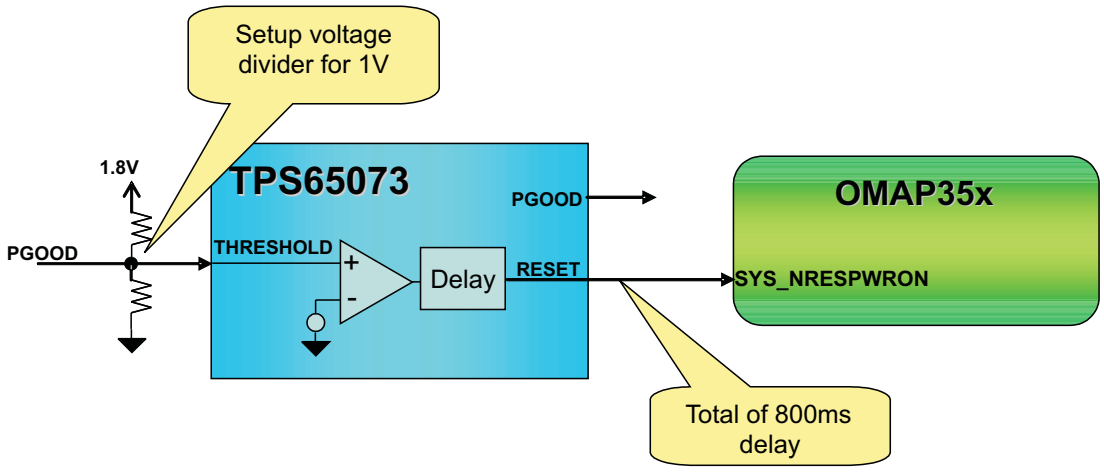

Figure 6. Using THRESHOLD to Further Extend RESET Signal to OMAP35x

- Add an external reset supervisor to further extend the length of the RESPWRON signal into OMAP35x. An example block diagram is shown in Figure 7.

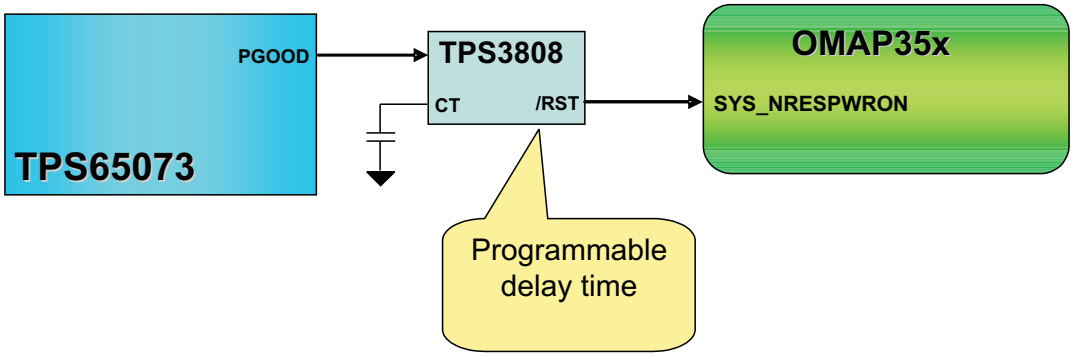

Figure 7. Using Reset Supervisor to Further Extend RESET Signal to OMAP35x

3.2 Clocks

3.2.1 Clock Rise/Fall Time

OMAP™35 clocks (both 32-kHz and high-frequency clocks) also have strict rise/fall requirements. Note the excerpts from the data manual in Table 10.

Table 10. Data Manual Excerpts

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_32k	32.768 kHz		±200 ppm	—	—	<20 ns
sys_xtalout sys_xtalin	12, 13, 16.8 or 19.2 MHz	Crystal	±25 ppm	NA	NA	NA
	12, 13, 16.8, 19.2, 26 or 38.4 MHz	Square	±50 ppm	45% to 55%	<1%	<2.5 ns
sys_altclk	48, 54, or up to 59 MHz		±50 ppm	40% to 60%	<1%	<10 ns

In order to meet these rise/fall times, a push-pull buffer is required to provide a faster edge on both clocks. See the diagrams in sections 32 kHz Clock Circuit and High Frequency Clock Circuit sections.

3.2.2 Clock Gating

When using an external oscillator for the high-frequency clock, OMAP35x SYS_CLKREQ signal is used to request the high-frequency clock. This signal can be used to gate the clock during the power up sequence while OMAP35x is going through its power up sequence.

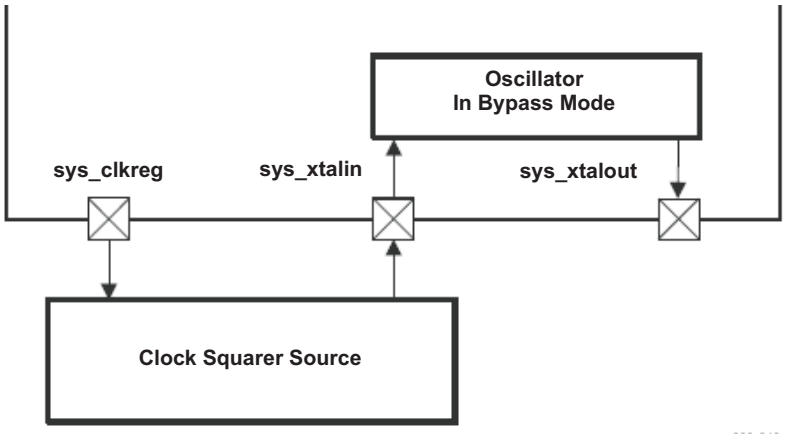

Figure 8. Clock Squarer Source Connection

Generally, the 32-kHz oscillator is powered by the 1.8-V supply. This should be used as a condition before applying the 32 kHz to the I/Os of OMAP35x.

3.2.3 32-kHz Clock Circuit

If the chosen 32-kHz oscillator exceeds the rise/fall time limit, a push-pull output buffer should be used to create a faster edge. Generally, the 32-kHz oscillator is powered by the 1.8-V supply. This should be used as a gating condition before applying the 32-kHz to the I/Os of OMAP35x. Alternatively, the RESET output of the TPS65073 can be used to provide a proper gating signal for this clock.

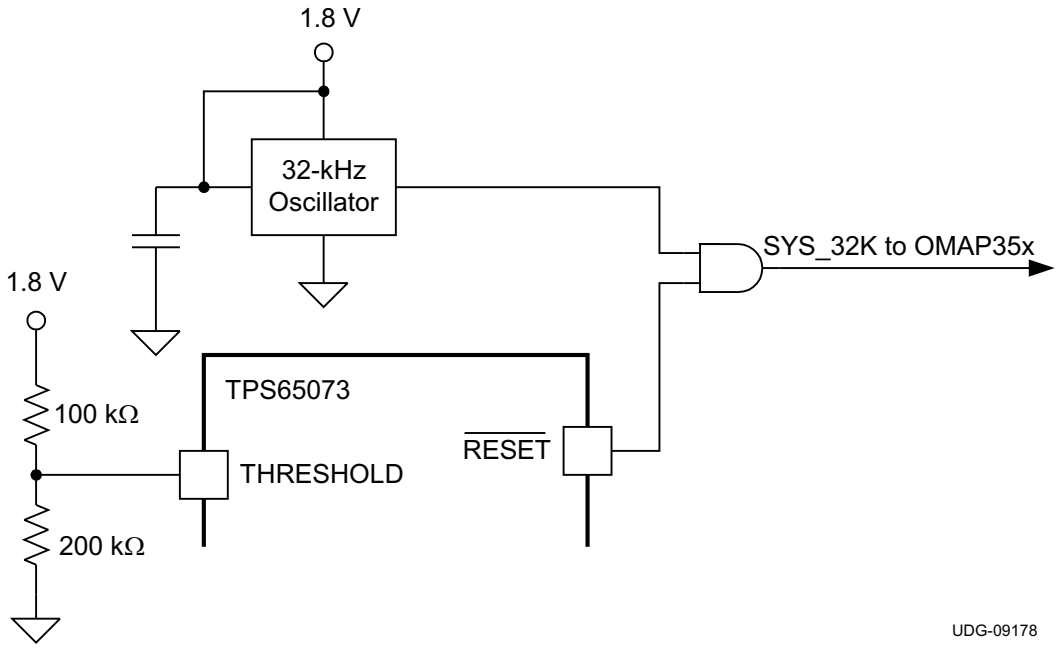

Figure 9. Push-Pull Buffer Circuitry on 32-kHz Clock

3.2.4 High-Frequency Clock Circuit

OMAP35x requires a high-frequency clock for normal operation. OMAP35x accepts two different types of input clock sources:

- a crystal can be used in combination with the internal OMAP35x oscillator for frequencies 12, 13, 16.8, or 19.2 MHz.
- a square oscillator can be used with the OMAP35x oscillator in bypass mode for frequencies 12, 13, 16.8, 19.2, 26, or 38.4 MHz

When an external oscillator is used, it has strict rise/fall time restrictions of less than 2.5 ns.

Table 11. Clock Source Requirements With External Oscillator

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_32k	32.768 kHz		±200 ppm	—	—	<20 ns
sys_xtalout sys_xtalin	12, 13, 16.8 or 19.2 MHz	Crystal	±25 ppm	NA	NA	NA
	12, 13, 16.8, 19.2, 26 or 38.4 MHz	Square	±50 ppm	45% to 55%	<1%	<2.5 ns
sys_altclk	48, 54, or up to 59 MHz		±50 ppm	40% to 60%	<1%	<10 ns

In order to meet these requirements, a push-pull buffer is required before the clock input of OMAP™3.

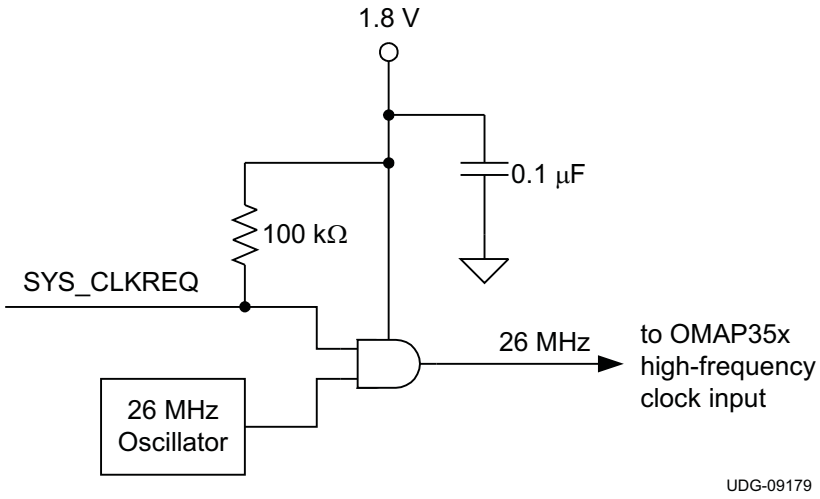

Figure 10. Push-Pull Buffer Circuitry on 26-MHz Clock

3.3 Power Devices

TPS65073- and TPS650731-based power solutions integrate many different power sources required to power up OMAP35x devices.

The TPS65073 features the following benefits to make it an ideal PMIC for OMAP35x:

- Contains three DC-DC converters and two LDOs with enough supply current for all OMAP35x family devices
- Each DC-DC converter and the LDOs can be sequenced using external sense signals and enables.
- The second LDO inside the TPS650731 can be used to power the OMAP35x MMC or VDAC rail. For power-sensitive applications, it is recommended to power the MMC and VDAC rails from a separate LDO to allow the enable/disable of the voltage separate from the PLL.
- Provides adjustable reset circuitry to control reset timing
- Provides adequate default voltages on power up
- Provides I2C control of all power sources
- Provides voltage scaling and adequate voltage granularity to allow implementation of DVFS and SmartReflex™ AVS.

3.4 VDAC Voltage

For applications requiring VDAC voltage, a separate LDO (TPS72118) is used which provides the proper 1.8-V, 150-mA maximum current. By connecting an OMAP35x GPIO, this power source can be enabled or disabled as the application requires. An example schematic is shown in Figure 11. If the application does not use the video DAC on OMAP35x, there is no need to include this LDO in the design.

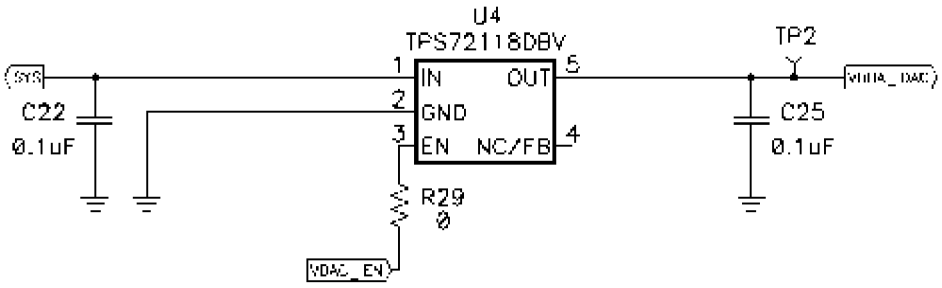

Figure 11. LDO Circuitry to Provide VDAC Voltage

Alternatively, one of the LDOs inside TPS65073 can be used to power the VDAC.

3.5 Sleep/Standby Modes

As described in Power Requirements and Features of OMAP35x section, the OMAP35x has many power management features that make it attractive in power-sensitive applications. One aspect of this is the sleep/standby modes of OMAP™35x, which allow the device to enter very low power states while maintaining certain levels of functionality. The OMAP35x also has the ability to go into a deep sleep mode and still recognize wakeup events when needed.

With a TPS65073 power solution, these sleep/standby modes can be implemented to take advantage of the power savings of an OMAP35x solution. Many different sleep/standby modes exist, depending on which portions of OMAP35x need to be active for the application. With the TPS65073 solution, there is individual control over each DCDC and LDO that powers the system. These can be enabled/disabled via I2C commands. Also, the TPS65073 can vary the voltage of VDD_MPU_IVA and VDD_CORE rail to enable low power operation. Furthermore, the TPS65073 can implement OFF mode using the SYS_OFF_MODE signal. This output of OMAP35x indicates when to turn on/off the VDD_MPU_IVA and VDD_CORE rails. When input into TPS65073, SYS_MODE_OFF can control these power rails to implement low power OFF mode conditions. OMAP35x can also detect wakeup signals, and subsequently enable the TPS65073 by transitioning SYS_OFF_MODE signal.

3.6 Enabling Class-2/3 SmartReflex™ Implementations

The TPS65073 power solution supports both Class 2 and Class 3 SmartReflex, however, using Class 3 limits the power features of the device. When implementing Class 3, the I2C communication is write only, so reading from the TPS65073 (necessary for touchscreen or battery charging, for example) is not possible. Class 2 SmartReflex does not have this limitation , and is fully supported along with the other features of the TPS65073.

Class-2 SmartReflex Implementation

With a Class-2 SmartReflex™ implementation, the ARM processor in OMAP3 controls all of the functions of the TPS devices. OMAP35x I2C1, I2C2 or I2C3 can each be used to connect to the I2C port of the TPS65073. If possible, use a dedicated I2C bus between OMAP35x and TPS65073. If ythe bus must be shared with other peripherals, group the TPS65073 devices with peripherals which require only infrequent I2C activity. This avoids long latencies during voltage changes. I2C communication allows full control over both SmartReflex voltage rails (VDD_MPU_IVA and VDD_CORE) to allow power optimization on the OMAP35x.

Class-3 SmartReflex Implementation

With a Class 3 SmartReflex implementation, the SmartReflex subchip inside OMAP35x handles most of the processing and communication with the power device, so that the burden of handling voltage variations is not on the ARM processor. In this scenario, connection from I2C4 to the TPS65073 is required, as this I2C port is used by the SmartReflex subchip to communicate with the TPS65073. OMAP35x can be configured with the I2C address of the TPS device, as well as the sub addresses of the appropriate registers to adjust VDD_MPU_IVA and VDD_CORE.

3.7 MMC/SD Boot

The OMAP35x processor has the ability to boot from many different sources. One possible boot configuration is to boot from MMC/SD. This configuration requires that the MMC/SD memory card is properly powered before ROM code executes (i.e., on power on reset).

If MMC/SD boot is a requirement, ensure that VDDS_MMC1 (and VDDS_MMC1A if using 8-bit MMC/SD data) is set for the proper voltage at power up. For MMC/SD cards, this is generally 3 V. If the MMC/SD boot source is a managed NAND device, for example, this may only require 1.8 V. In either case, ensure that the voltage source for this device is enabled on power up.

As shown in Figure 3, MMC voltage is connected to an external LDO. This voltage is enabled/disabled using an OMAP35x GPIO. In order to have this voltage enabled on power up, an OMAP35x GPIO which defaults to an output with the correct polarity is required. For example, in an excerpt from the OMAP35x data manual below, the columns labeled BALL RESET STATE and BALL RESET REL. STATE are important for this functionality. BALL RESET STATE is the state of the signal during reset (ie, during the power up sequencing). BALL RESET REL. STATE is the name of the signal after reset is released.

When using a low enabled signal, choose a signal with 0 or L in these two columns. When using a high enabled signal, choose a signal with 1 or H in these two columns. This allows the external power device to be properly enabled on power up so MMC/SD boot operates correctly. Ensure the chosen GPIO is not used by the ROM for booting from other sources. When using a GPIO-enabled power source the LDO can be selectively enabled/disabled to conserve power when not using MMC/SD.

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE(10) [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
		gpio_57	4	IO								
		safe_mode	7									
N8	NA	gpmc_ncs7	0	O	H	H	7	vdds_ mem	Yes	4(4)	PU/ PD	LVCMOS
		gpmc_io_dir	1	O								
		mcbsp4_fsx	2	IO								
		gpt8_pwm_ evt	3	IO								
		gpio_58	4	IO								
		safe_mode	7									
T4	W2	gpmc_clk	0	O	L	0	0	vdds_ mem	Yes	4(4)	PU/ PD	LVCMOS
		gpio_59	4	IO								
		safe_mode	7									
F3	W1	gpmc_nadv_ ale	0	O	0	0	0	vdds_ mem	No	4(4)	NA	LVCMOS
G2	V2	gpmc_noe	0	O	1	1	0	vdds_ mem	No	4(4)	NA	LVCMOS

Figure 12. Ball Characteristics

Alternatively, use one of the LDOs that is included in the TPS65073. These LDOs default to a 1.8-V input supply only, so if a higher voltage is needed on power up, choose an external LDO and use the method previously described.