Application Report

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High-Efficiency Power Solution Using DC/DC Converter With DVFS

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ABSTRACT

This reference design helps those desiring to design-in the TMS320C6742, TMS320C6746, TMS320C6748 and OMAP-L138. This design, employing sequenced power supplies, describes a system with an input voltage of 5 V, and uses a high-efficiency DC/DC Converters with integrated FETs and DVFS for a small, simple system.

Sequenced power supply architectures are becoming commonplace in high-performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have smaller geometry cells and require lower supply voltages than the system bus voltages. Power management in these systems requires special attention. This application note addresses these topics and suggests solutions for output voltage sequencing.

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1 Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter ICs.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up. Bus contention also may affect I/O reliability. Power supply designers must check the requirements regarding bus contention for individual devices.

The power-on sequencing for the OMAP-L138, TMS320C6742, TMS320C6746, and TMS320C6748 are shown in the Power Requirements table below. No specific voltage ramp rate is required for any of the supplies as long as the 3.3-V rail never exceeds the 1.8-V rail by more than 2 V.

In order to reduce the power consumption of the processor core, Dynamic Voltage and Frequency Scaling (DVFS) is used in the reference design. DVFS is a power management technique used while active processing is going on in the system-on-chip (SoC) which matches the operating frequency of the hardware to the performance requirement of the active application scenario. Whenever clock frequencies are lowered, operating voltages are also lowered to achieve power savings. In the reference design, TPS62353 is used which can scale its output voltage.

2 Power Requirements

The power requirements are as specify in the table.

	PIN NAME	VOLTAGE (1) (2) (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
I/O	RTC_CVDD	1.2	1	–25%, +10%	1(3)	
Core	CVDD(4)	1.0 / 1.1 / 1.2	600	–9.75%, +10%	2	
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	–5%, +10%	3	
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%	4	
I/O	USB0_VDDA33, USB1_VDDA33	3.3	24	±5%	5	
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 / 3.3	50 / 90(5)	±5%	4 / 5	

(1) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3 -V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1)

(2) There is no specific required voltage ramp rate for any of the supplies LVCMOS33 (USB0_VDDA33, USB1_VDDA33) never exceeds STATIC18 (USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18) by more than 2 volts.

(3) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

(4) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.

(5) If DVDD3318_A, B, and C are powered independently, maximum power for each rail is 1/3 the above maximum power.

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3 Features

The design uses the following high-efficiency DC/DC Converter with integrated FETs .

INPUT VOLTAGE	~5V
	HIGH EFFICIENCY AND INTEGRATION (w DVFS)
COMBINE RTC AND STATIC 1.2	
Core 1.2 V at 600 mA	TPS62353
Static 1.2 V + VRTC at 251 mA	TPS62232
Static 1.8 V at 230 mA	TPS62231
Static 3.3 V at 115 mA	TPS71733 (DRV)

Here VRTC is included in the STATIC12 (fixed 1.2 V) group.

TPS62353

- 88% Efficiency at 3-MHz Operation
- Output Peak Current up to 800 mA
- 3-MHz Fixed Frequency Operation
- *Best in Class* Load and Line Transient
- ±2% PWM DC Voltage Accuracy
- Efficiency Optimized Power-Save Mode
- Transient Optimized Power-Save Mode
- Fixed 1.2-V output eliminates need for external voltage-setting resistors
- Available in a 10-Pin QFN (3 × 3 mm) 12-Pin NanoFree™ (CSP) Packaging

TPS62231 and TPS62232

- 3 MHz switch frequency
- Up to 94% efficiency
- Output Peak Current up to 500mA
- Small External Output Filter Components (1 µH/ 4.7 µF)
- Small 1 × 1,5 × 0,6-mm 3 SON Package
- Fixed 1.8V and 1.2V output respectively eliminates need for external voltage-setting resistors

TPS71733

- 150-mA Low-Dropout Regulator with Enable
- Low Noise: 30 µV typical (100 Hz to 100 kHz)
- Excellent Load/Line Transient Response
- Small SC70-5, 2-mm × 2-mm SON-6, and 1,5-mm × 1,5-mm SON-6 Packages

More information on the devices can be found from the data sheets:

- TPS62353, http://focus.ti.com/lit/ds/symlink/tps62350.pdf
- TPS71733, http://focus.ti.com/lit/ds/symlink/tps71733.pdf
- TPS62231 and TPS62232, http://focus.ti.com/lit/ds/symlink/tps62230.pdf

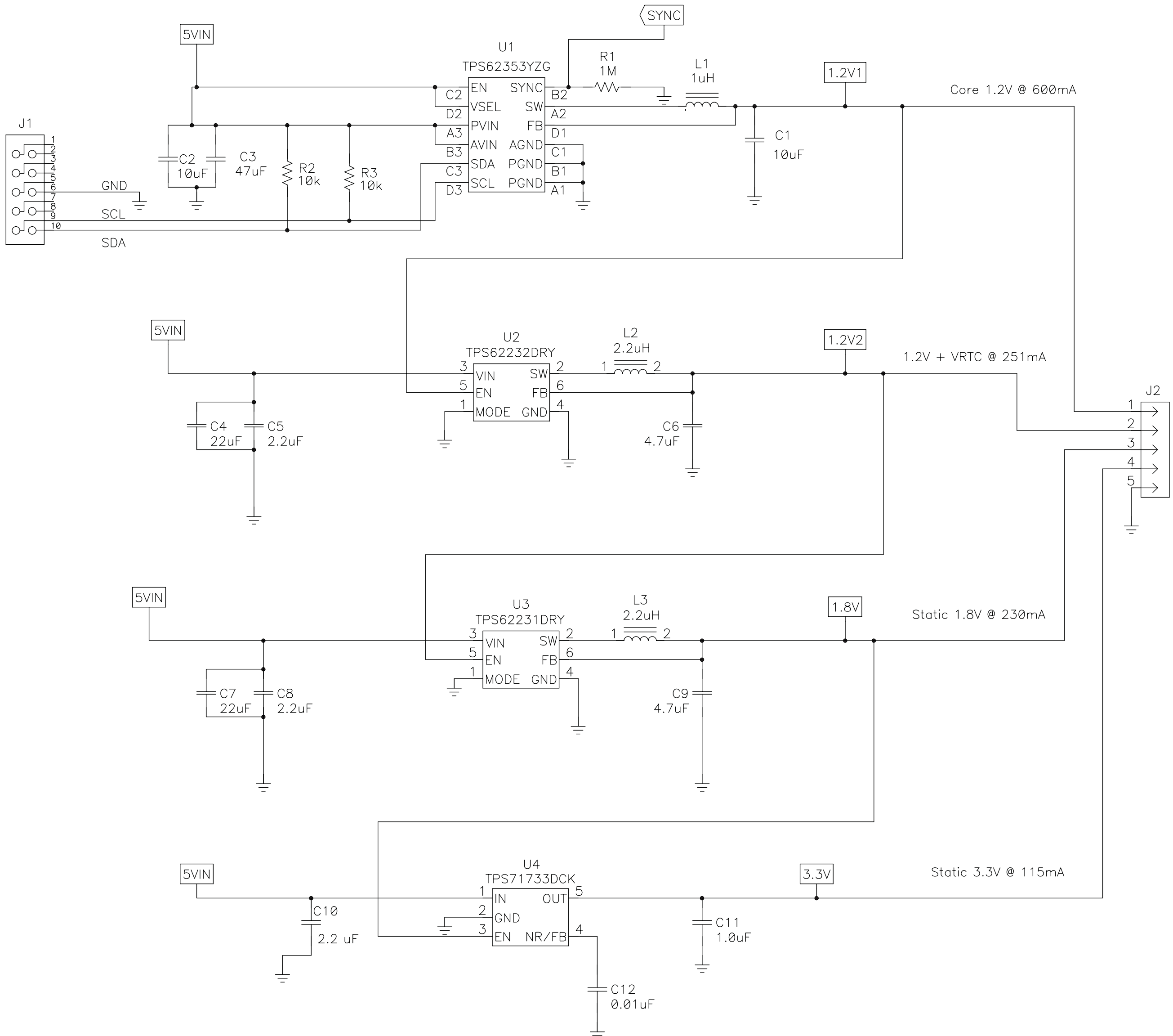
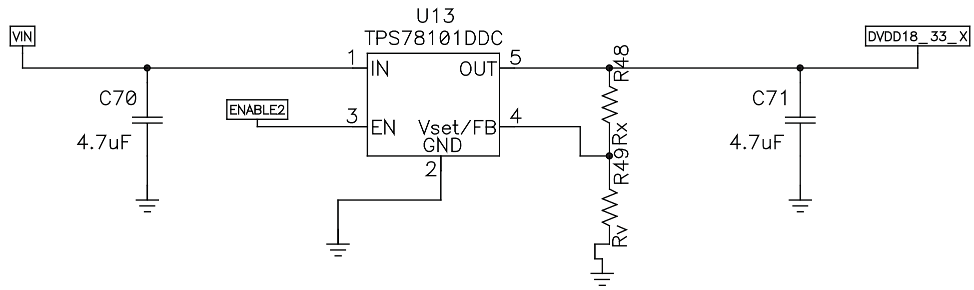


Figure 1. PMP4979 Reference Design Schematic

Proper sequencing is ensured in the design with the use of a enable pins. As required, Core 1.2 V at 600 mA comes first, followed by Static 1.2 V + VRTC at 251 mA, Static 1.8 V at 230 mA which in turn enable the LDO and hence at last Static 3.3 V at 115 mA comes up.



(1) Use three such LDOs to power up DVDDA, DVDDB, DVDDC (It can either be 1.8 V or 3.3 V)

(2) Rx = 0.499 MΩ, Ry = 1 MΩ for Vout = 1.8 V

(3) Rx = 1.8 MΩ, Ry = 1 MΩ for Vout = 3.3 V

(4) For proper sequencing of output, enable of the LDOs are fed either from 1.2-V output from 1.2-V output from TPS62232 if DVDDX is 1.8 V or from 1.8-V output from TPS62231 if DVDDX is 3.3 V.

Figure 2. Optional Circuit for DVDD_A, DVDD_B, and DVDD_C

4 List of Material

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
2	C1	10 μF	Capacitor, Ceramic, 6.3V, X5R, 10%	603	C1608X5R0J106KT	TDK	5650
	C2	10 μF	Capacitor, Ceramic, 6.3V, X5R, 10%	603	C1608X5R0J106KT	TDK	5650
1	C3	47 μF	Capacitor, Ceramic, 10V, X5R, 20%	1812	C4532X5R1A476M	TDK	43,360
2	C4	22 μF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std	83,600
2	C5	2.2 μF	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ225MV	Taiyo Yuden	2800
2	C6	4.7 μF	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ475MV	Taiyo Yuden	2800
	C7	22 μF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std	83,600
	C8	2.2 F	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ225MV	Taiyo Yuden	2800
	C9	4.7 F	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ475MV	Taiyo Yuden	2800
1	C10	2.2 F	Capacitor, Ceramic, 16V, X5R, 10%	603	C1608X5R1C225K	TDK	5650
1	C11	1.0 F	Capacitor, Ceramic, 25V, X5R, 10%	603	C1608X5R1E105K	TDK	5650
1	C12	0.01 F	Capacitor, Ceramic, 50V, X7R, 10%	603	C1608X7R1H103K	TDK	5650
1	J1	2510-6002UB	Connector, Male Straight 2x10 pin, 100mil spacing, 4 Wall	0.338 × 0.788	2510-6002UB	3M	301.024
1	J2	PEC36SAAN	Header, Male 5-pin, 100mil spacing, (36-pin strip)	0.100 inch × 5	PEC36SAAN	Sullins	60000
1	L1	1 H	Inductor, SMT, 1.6A, ±30%	0.118 × 0.118	LPS3010-102NLC	Coilcraft	26,560
2	L2	2.2 H	Inductor, SMT, 0.7A, 230-mΩ	805	MIPSZ20120D2R2	FDK	10160
	L3	2.2 H	Inductor, SMT, 0.7A, 230-mΩ	805	MIPSZ20120D2R2	FDK	10160
1	R1	1M	Resistor, Chip, 1/16W, 1%	603	Std	Std	5650
2	R2	10k	Resistor, Chip, 1/16W, 1%	603	Std	Std	5650
	R3	10k	Resistor, Chip, 1/16W, 1%	603	Std	Std	5650
1	U1	TPS62353YZG	IC, 3MHz Synchronous Step Down Converter with I^2C, 800mA	CSP-12	TPS62353YZG	TI	12,000
1	U2	TPS62232DRY	IC, 3MHz Ultra Small Step Down Converter, x.x V	QFN	TPS62232DRY	TI	6020
1	U3	TPS62231DRY	IC, 3MHz Ultra Small Step Down Converter, x.x V	QFN	TPS62232DRY	TI	6020
1	U4	TPS71733DCK	IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators	SC70	TPS71728DCK	TI	18.6

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.1 Test Result

The start-up waveform is shown in Figure 3, which specifies the sequencing order that is required.

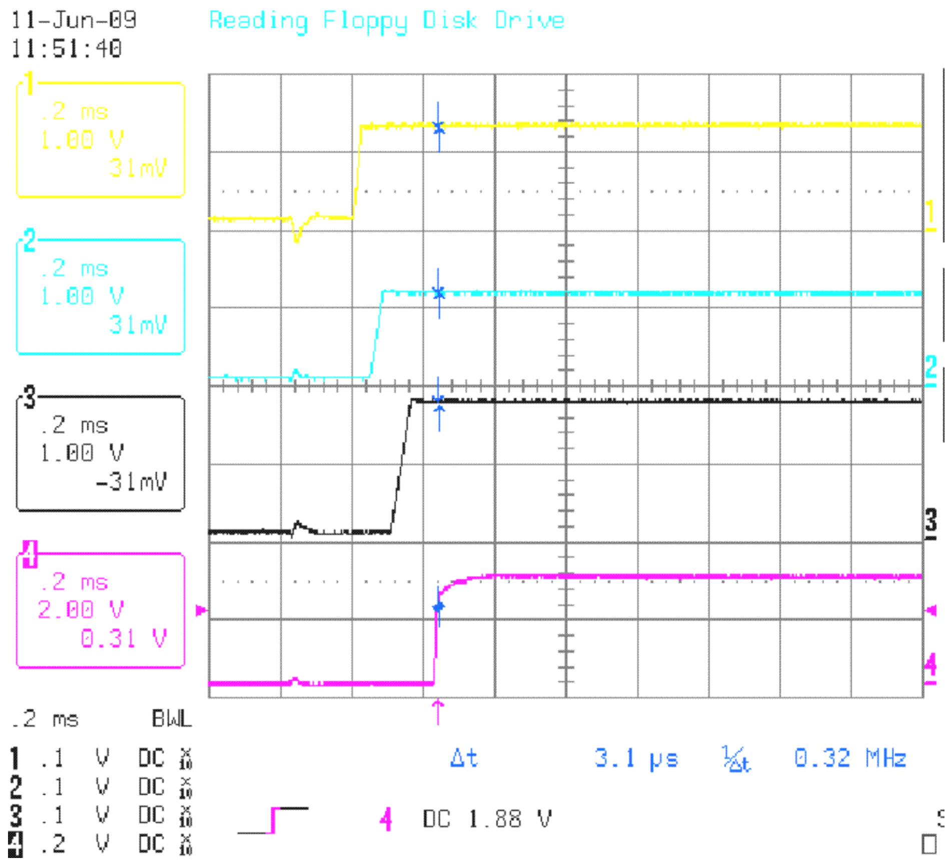


Figure 3. Sequencing in Start-Up Waveform

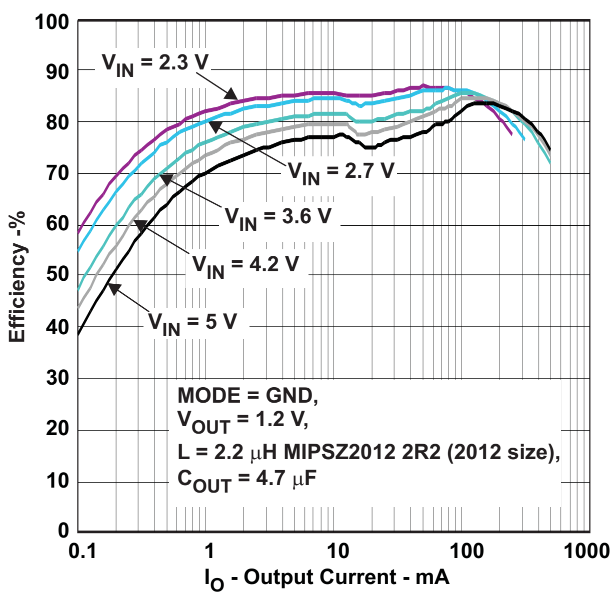


Figure 4. Efficiency vs Output Current

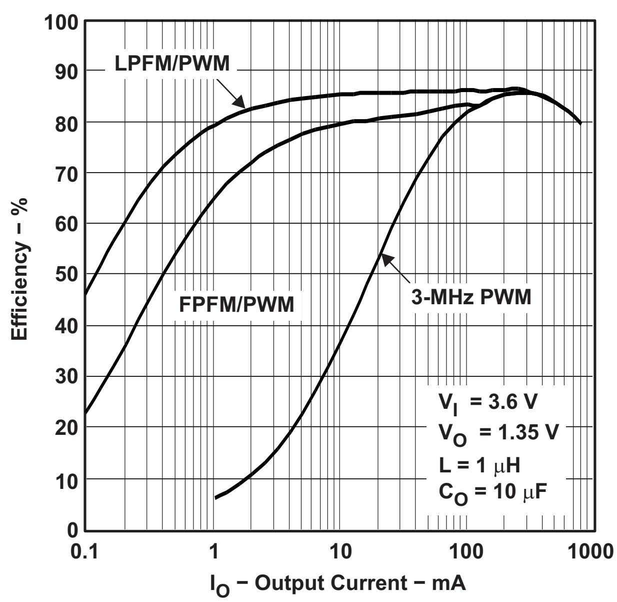


Figure 5. Efficiency vs Output Current

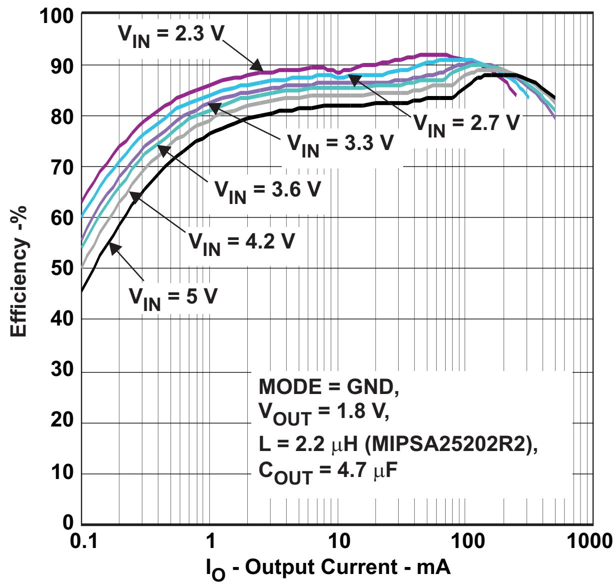


Figure 6. Efficiency vs Output Current

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