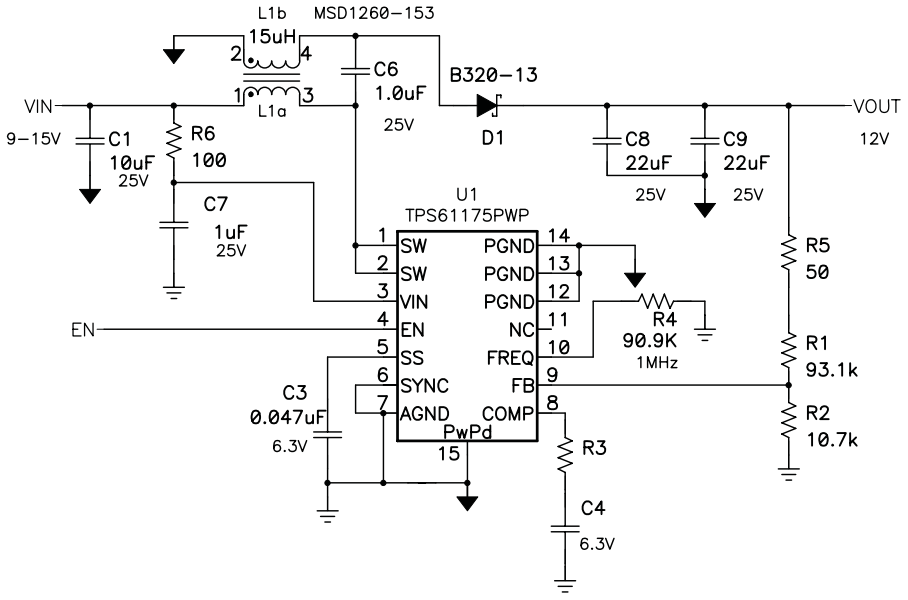
TPS61175 SEPIC Design

Jeff Falin
PMP - DC/DC Low-Power Converters

Design Example

When a dc/dc converter providing a regulated output voltage between the minimum and maximum input voltage is required, neither a single buck or a boost converter can provide the output voltage. However, a boost converter integrated circuit (IC) can be configured to drive a single-ended, primary-inductor converter (SEPIC) power stage and provide an output voltage that is between the input voltage extremes. The following design example helps a user design a 12-V power supply from a 9-V to 15-V input power source using the TPS61175 boost converter IC in the SEPIC configuration. The Texas Instruments application report SLYT309 gives detailed explanations of how the SEPIC converter operates and provides more information on the equations used in this document. Figure 1 shows the power supply circuit.



Note: This schematic excludes the reference designators of open components on the PR894E–1 PCB.

Figure 1. 12-V Power Supply From 9-V to 15-V Input Power Source

Table 1 gives the performance specifications for the reference design.

Table 1. Performance Specifications for the Reference Design

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT and AMBIENT CHARACTERISTICS						
V_{IN}	Input voltage		9	12	15	V
f_S	Switching frequency			1		MHz
T_A	Ambient temperature				55	°C
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		11.5	12	12.5	V
	Load regulation	V_{IN} = 9 V, 10 mA < I_O < 800 mA			1%	$\Delta V_O/\Delta I_O$
V_{RIPPLE}	Output voltage ripple	I_O = 800 mA			100	mVpp

Table 1. Performance Specifications for the Reference Design (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
I_O	Output current		1		800	mA
η	Efficiency	I_O = 800 mA		85%		
TRANSIENT RESPONSE						
ΔI_{TRAN}	Load step			400		mA
$\Delta I_{TRAN}/\Delta t$	Load slew rate		0.20			A/µs
ΔV_{TRAN}	V_O undershoot			400		mV

1. DUTY CYCLE: Use Equation 1 to estimate the duty cycle.

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D} \quad (1)$$

D_{MAX} = 0.58 occurs at $V_{IN(MIN)}$= 9 V and D_{MIN}=0.45 occurs at $V_{IN(MAX)}$=15V.

2. $I_{OUT(MAX)}$ and $I_{SW(DC)}$: Use Equation 2 to estimate the maximum average input current.

$$I_{IN(DC)} = \frac{I_{OUT}}{\eta_{EST}} \times \frac{V_{OUT} + V_D}{V_{IN}} \quad (2)$$

At $V_{IN(MIN)}$=9 V and η_{EST} = 0.85, $I_{IN(DC)}$ = 1.31 A while at $V_{IN(MAX)}$ = 15 V and η_{EST} = 0.90, $I_{IN(DC)}$ = 0.74 A. Note that in a SEPIC, the switch must handle the current from the input source as well as the output current. So, the maximum average switch current, ignoring inductor current ripple, is 1.31 A + 0.8 A = 2.11 A. Equation 2 ignores the inductor ripple current. But, for stable power supply operation and to minimize EMI, the inductor ripple current, ΔI_L must be no more than a fraction, K_{IND} = 20%-40% of the maximum input current. So, use Equation 3 to estimate the maximum output current for an IC with internal current limit, I_{LIM}, including the effects of ΔI_L . Assuming estimated efficiency η_{est} = 85% at $V_{IN(MIN)}$ = 9 V and K_{IND} = 0.2,

$$I_{OUT(MAX)} = \frac{I_{LIM}}{\left(\frac{V_{OUT} + V_D}{V_{IN(MIN)}}\right) \times \left(\frac{1 + K_{IND}}{\eta_{EST}}\right) + 1} = \frac{3A}{\left(\frac{12V + 0.5V}{9V}\right) \times \left(\frac{1 + 30\%}{0.85}\right) + 1} = 0.960A \quad (3)$$

Equation 3 assumes that both inductors, L_{1a} and L_{1b}, are coupled on the same core. Computing the switch power dissipation was omitted since we are using the IC well below its maximum current and voltage capabilities.

3. INPUT CAPACITANCE (C1): Use the data sheet's recommendation of 10 µF for the input capacitance. If nonceramic, higher ESR capacitors used, the designer must confirm that the capacitor's ripple current does not exceed that capacitor's ripple current rating as explained in SLYT309.

4. INDUCTANCE (L1a and L1b): From the previous computations where K_{IND}=0.2 and $I_{IN(DC)}$ = 1.31 A at $V_{IN(MIN)}$ = 9 V, $\Delta I_L = K_{IND}$ X $I_{IN(DC)}$=0.26 A. After substituting f_S = 1 MHz, $V_{IN(MAX)}$ = 9 V, use Equation 4 to get the minimum coupled inductance L_{1a}=L_{1b} required to keep the inductor ripple current less than 20% of the input current.

$$L_{1a} = L_{1b} \geq \frac{1}{2} \times \frac{V_{IN(max)} \times D_{(min)}}{\Delta I_{L(15V_{IN})} \times f_S} = \frac{1}{2} \times \frac{15V \times 0.45}{0.220A \times 1MHz} = 15.3\mu H \rightarrow 15\mu H \quad (4)$$

Note if L1a and L1b are closely coupled, the ripple current is divided between them and the required inductance is halved. In account for inductor tolerance, the designer selected the next closest standard value, which is 15 µH.

When selecting an inductor, the two additional specifications are its DC resistance (DCR) and its current rating, which is the lower of either its saturation current or its current for 40°C temperature rise. For the SEPIC converter with two inductors, choosing a coupled inductor with DCR less than 100 mΩ per winding minimizes these losses. The maximum inductor current per winding occurs at $V_{IN(MIN)}$ and is $I_{IN(DC)}$ + ΔI_L/2 = 1.31 A + 0.26/2 = 1.70 A for L_{1a} and I_{OUT} + ΔI_L= 0.8 A + 0.26 A/2 = 0.93 A for L_{1b}. Adding 20% for inductor current ripple spikes due to load transients, the designer selected MSD1260-153 from Coilcraft, capable of 2.06 A in each winding simultaneously, 2.92 A maximum in a single winding, and 85-mΩ DCR per winding.

5. OUTPUT CAPACITANCE (C8 and C9): Use Equation 5 and the transient specification to size the output capacitance.
   Assuming a ceramic output capacitor with negligible ESR and output ripple specification V_{RIPPLE} = 50 mVpp, Equation 5 recommends that the minimum output capacitance be
   $$C_{OUT} \geq \frac{I_{OUT} \times D_{(max)}}{\Delta V_{RPL} \times f_S} = \frac{0.8A \times 0.58}{50mV_{PP} \times 1MHz} = 9.3\mu F \quad (5)$$
   To meet the load transient specification and assuming a control loop bandwidth f_{BW} = 5 kHz, Equation 6 gives
   $$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} = \frac{0.4A}{2\pi \times 5KHz \times 400mV} = 32\mu F \quad (6)$$
   The loop bandwidth assumption of 5 kHz may have to be modified later. The designer selected C2 = 2 × 22 μF, 50-V output capacitors instead of one 47-μF capacitor because the resonance frequency of most 47-μF capacitors is above the 1-MHz switching frequency. If capacitors with higher ESRs than those of ceramic capacitors are used, the designer must include the effect of the ESR when sizing the output capacitor for the specified ripple but also confirm that the capacitor ripple current does not exceed that capacitor's ripple current rating as explained in SLYT309.
6. SERIES CAPACITOR (C6): Knowing that $I_{L1b} = I_{OUT}$ flows into C_P during the on time, it is recommended to choose C_P so that its ripple ΔV_{Cp} is no more than 5% of $V_{Cp(DC)} = V_{IN}$. The worst case occurs at $V_{IN(MAX)}$. Use Equation 7 to compute the minimum capacitor assuming ΔV_{Cp} = 5% x $V_{IN(MAX)}$ = 0.75 V.
   $$C_6 \geq \frac{I_{OUT} \times D_{(MAX)}}{\Delta V_{Cp-PKPK} \times f_S} = \frac{0.8A \times 0.45}{0.75V_{PKPK} \times 1MHz} = 0.48uF \quad (7)$$
7. SOFT START CAPACITOR (C3): Use the data sheet's recommendation of 0.047 μF for the soft start capacitor. Increasing this value slows down the output voltage's rise time and also minimizes in-rush current.
8. SCHOTTKY DIODE (D1): Even with an ideal printed-circuit board layout containing short traces to minimize stray inductance and capacitance, the switching node of the boost converter may exhibit ringing up to 30% higher than the output voltage. Therefore, the designer selected a 20-V-rated diode to accommodate such ringing. The designer also selected a diode with a thermal rating that is high enough to accommodate its power dissipation, which is approximately $P_{D(DIODE)} = I_{OUT} \times V_f$ = 800 mA × 0.5 V = 400 mW.
9. FEEDBACK RESISTORS (R1 and R2): The data sheet recommends 10 kΩ as an optimum value for R2. Larger or smaller values can be used at the risk of noise being injected into FB or higher current lost through the FB resistors, respectively. After first trying 10 kΩ, the designer selected R2 = 10.7 kΩ so that R1 computes closer to a standard resistor value per Equation 8:
   $$R1 = R2 \times \left(\frac{V_{OUT}}{1.229V} - 1 \right) = 10.7k\Omega \times \left(\frac{12V}{1.229V} - 1 \right) = 93.7k\Omega \rightarrow 93.1k\Omega \quad (8)$$
10. SWITCHING FREQUENCY RESISTOR (R4): Use data sheet Figure 13 to properly size the resistor for f_S = 1 MHz. Higher switching frequencies allow for lower valued, and therefore potentially smaller packaged, inductors at the expense of higher switching losses and lower efficiency.
11. COMPENSATING THE CONTROL LOOP (R3 and C4): As summarized in Dr. Ray Ridley's article[1], the mathematical model for the SEPIC converter is extremely complicated. Therefore, when using a current-mode controlled converter with a transconductance amplifier like the TPS61175, it is easier and faster to compensate the loop by inspection of the duty cycle to output (i.e., power stage or plant) transfer function. This transfer function can be obtained from either simulated data using a Spice model as explained in Dr. Ridley's article or measured data. To obtain the measured data, a Venable or equivalent gain/phase analyzer is necessary. After designing the converter using the previous steps, use a large compensation capacitor (e.g., C4 = 1 μF) and nominal compensation resistor (e.g., R3 = 1 kΩ) to roll off the control loop at a very low frequency and then measure the power stage transfer function. Figure 2 shows measured results from the power stage transfer function's gain and phase at full load for $V_{IN(MIN)}$, in red and royal blue, and $V_{IN(MAX)}$, in maroon and dark blue, respectively.

(1) Ray Ridley, Designer's Series, Part V: Current-Mode Control Modeling. *Switching Power Magazine* , 2006, [Online]. http://www.switchingpowermagazine.com/downloads/5%20Current%20Mode%20Control%20Modeling.pdf

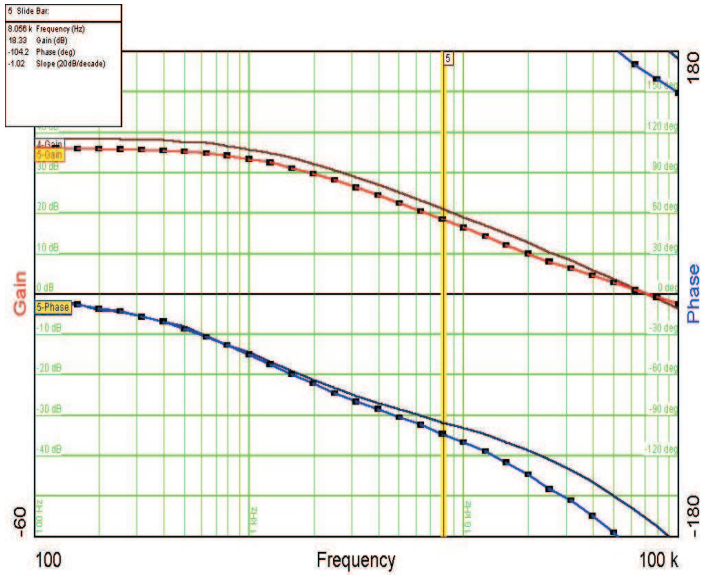


Figure 2. Measured Power Stage Gain and Phase With R3 = 1 kΩ and C4 = 1 μF

Dr. Ridley[1] writes that there are three RHP zeroes with two of those being complex. Equation 9 computes the lowest frequency RHP zero, which occurs at $V_{IN(MIN)}$.

$$f_{RHPZ} = \frac{1}{2\pi \times \frac{L_{1a}}{R_{OUT}} \times \left(\frac{D}{1-D}\right)^2} = \frac{1}{2\pi \times \frac{15\mu H}{15\Omega} \times \left(\frac{0.58}{1-0.58}\right)^2} = 83.5kHz \quad (9)$$

To prevent switching noise or gain fluctuations due to changes in nonmeasured parameters from causing small signal instability, conventional wisdom is for the crossover frequency, f_{BW}, to be kept below f_{RHPZ}/10 =X 8 kHz in order to avoid the effects of the RHPZ on the control loop. Therefore, the compensation gain, K_{COMP}, and power stage gain at the 8-kHz crossover frequency must be 0 dB, or $K_{COMP}(f_{BW})$ + 20log($G_{PW}(f_{BW})$) = 0 dB, so $K_{COMP}(f_{BW})$ = -20log($G_{PW}(f_{BW})$ = –18.33 dB as illustrated by the yellow line in Figure 2. Using Type II compensation and finding G_{EAmax}= 440 μmho in the data sheet, Equation 10 computes the value of R3 to give $K_{COMP}(f_{BW})$ = –-18.33 dB, rounded up to the closest standard value.

$$R3 \cong \frac{10^{\frac{K_{COMP}(f_C)}{20dB}}}{G_{EA(MAX)} \times \frac{R2}{R2+R1}} = \frac{10^{\frac{-18.33dB}{20dB}}}{440\mu mho \times \frac{10.7k\Omega}{93.1k\Omega + 10.7k\Omega}} = 2.69k\Omega \quad (10)$$

The compensation zero, f_Z, is typically set between 1/5 and 1/10 of f_{BW} in order to maximize its phase boost at the crossover frequency. The designer set the f_Z ~= f_{BW}/5 = 1.6 kHz and solved for C4. The answer was rounded down to the closest standard value.

$$C4 \cong \frac{1}{2\pi \times R3 \times f_Z} = \frac{1}{2\pi \times 2.67k\Omega \times 1600Hz} = 0.037\mu F \rightarrow 0.039\mu F \quad (11)$$

Figure 3 shows the measured loop gain and phase. As designed for $V_{IN(MIN)}$, the measured f_{BW} is slightly higher than 8 kHz and the phase margin is almost 60°.

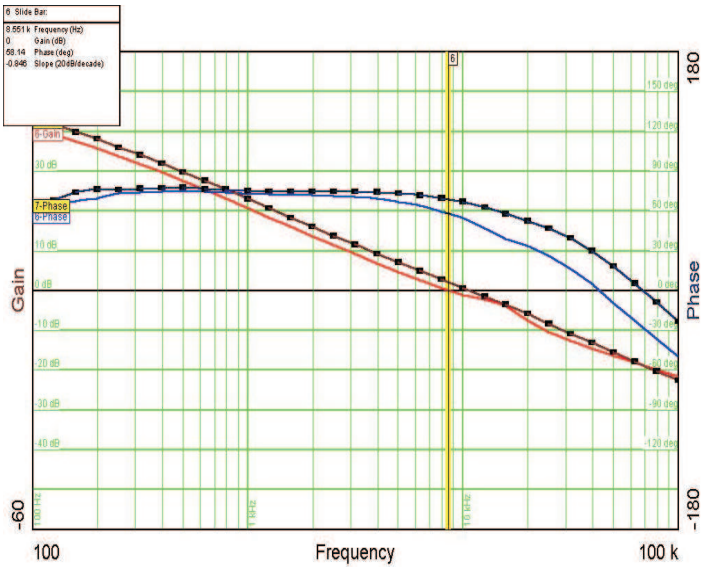


Figure 3. Measured Total Loop Gain and Phase With R3 = 2.67 kΩ and C4 = 0.039 μF

Figure 4 shows the transient response for a 400-mA load step. The ΔV_{TRAN} droop of 320 mV is below the 400-mV design specification.

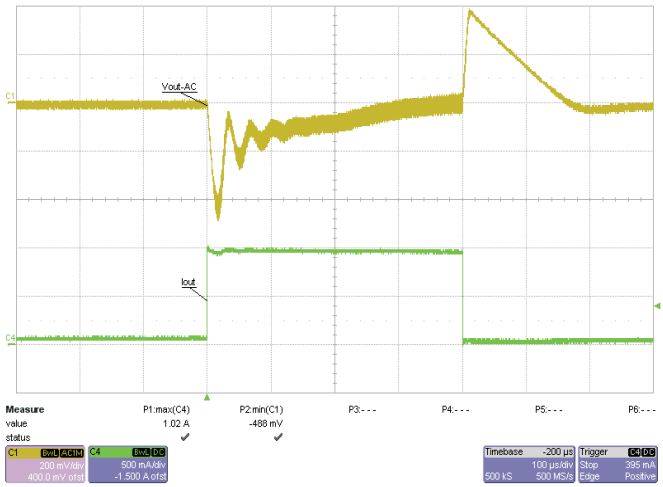


Figure 4. Load Transient Response With V_{IN} = 9 V and I_{OUT} = 20 mA to 400 mA

Figure 5 shows the efficiency.

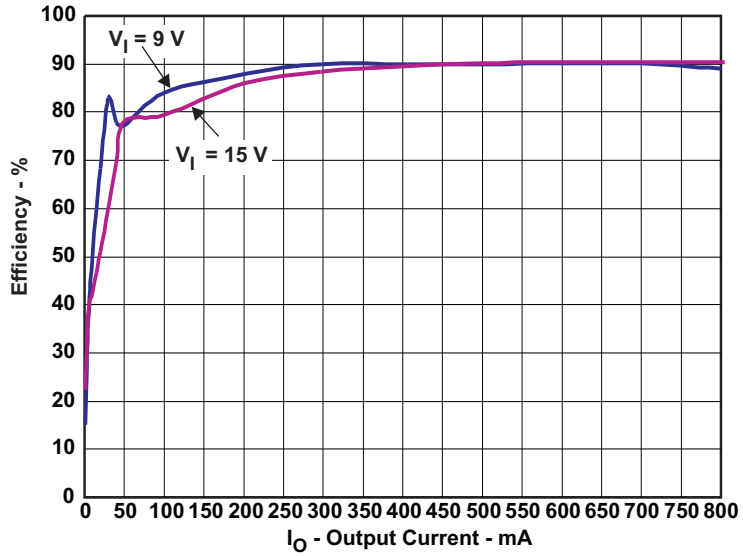


Figure 5. Efficiency

Figure 6 shows the load regulation, which is well within the 1% specification

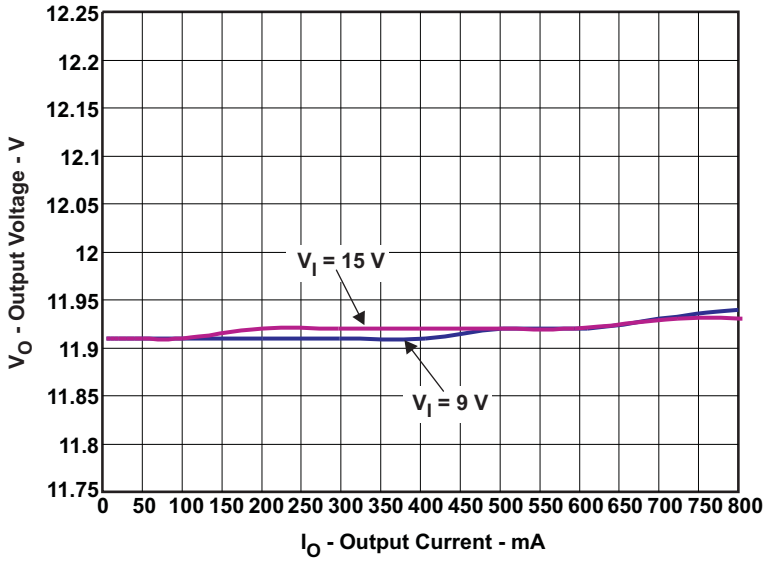


Figure 6. Load Regulation

Figure 7 and Figure 8 show typical operating waveforms.

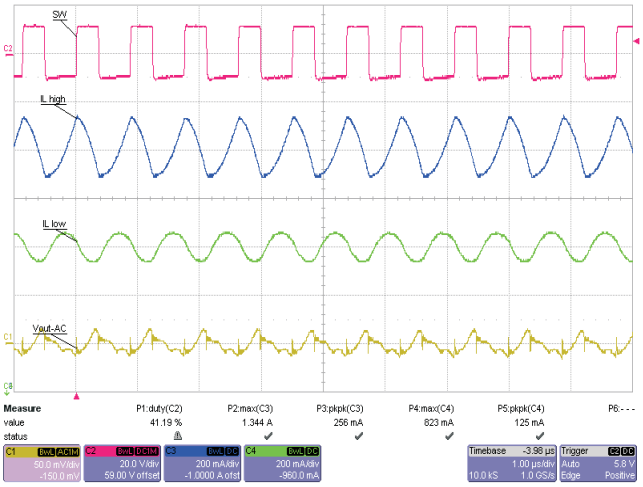


Figure 7. Operation Including V_{RIPPLE} at V_{IN} = 9 V and I_{OUT}=800 mA

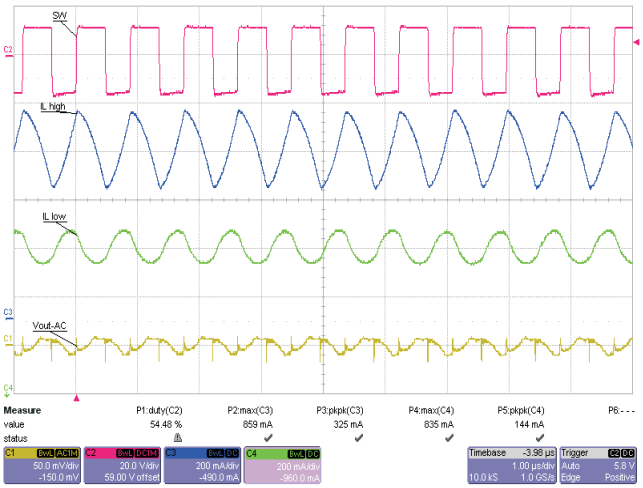


Figure 8. Operation Including V_{RIPPLE} at V_{IN} = 15 V and I_{OUT}=800 mA

Figure 9 shows the startup waveform.

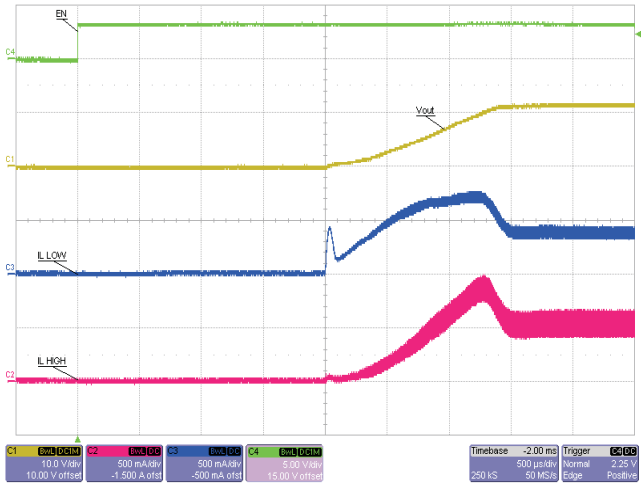


Figure 9. Startup at V_{IN} = 9 V and I_{OUT}=400 mA

The preceding design steps are applicable to any current-mode, control-based nonsynchronous boost converter used in a SEPIC configuration.

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