Application Report
SLVA332A–October 2009–Revised June 2010

# 3.6-V to 6-V Input, 3.3-V Output, Tiny, and High-Efficiency DC/DC Converter

*PMP - DC/DC Low-Power Converters*

## ABSTRACT

This reference design is presented to help application designers and others who are trying to use the MSP430 in a system with an input voltage in the range of 3.6 V to 6 V with the primary design objective to minimize solution size as well as to maintain high efficiency and long battery life.

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## 1 Features

- 3.6-V to 6-V input voltage range
- Capable of driving up to 500 mA (TPS62300)
- High efficiency (over 92%)
- 3-MHz operation allows for small passive components
- Low quiescent current (20 μA)
- Tiny 8-pin NanoStar™ (chip scale) and QFN-10 packages

## 2 Introduction

This reference design is for the MSP430 family of microcontroller devices and accounts for the voltage and current requirements as described herein. The MSP430 devices require only a single 3.3-V input; no sequencing is required. The operating input voltage for this reference design is between 3.6 V to 6 V. This design is optimized for a small solution size with a low component count and high efficiency.

For more information and other reference designs, please visit www.ti.com/processorpower.

## 3 Requirements

The power requirements for each MSP430 family are listed below. The power given is based on the amount of current the core consumes per megahertz (MHz). The *Analog* $I_{MAX}$ column indicates the amount of current added if the additional functional blocks are used.

For more information and other reference designs, please visit www.ti.com/processorpower.

### Table 1. CC43 Family Power Requirements

| DEVICE FAMILY | PIN NAME | VOLTAGE (V) | | CPU $I_{MAX}$ (μA/MHz) | ANALOG $I_{MAX}$ (μA) | SEQUENCING ORDER | TIMING DELAY | COMMENTS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | | | | | |
| F613x, F513x | $A_{VCC}$, $D_{VCC}$ (1) | 1.8 | 3.6 | 250 (2) | $I_{REF}$ = 140 | n/a | n/a | +Maximum CPU speed of 20 MHz |

(1) It is recommended to power $A_{VCC}$ and $D_{VCC}$ from the same source. A maximum difference of 0.3 V between $A_{VCC}$ and $D_{VCC}$ can be tolerated during power-up.

(2) Maximum value for CPU clocked at 20 MHz at 3 V shown. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

### Table 2. MSP430x1xx Family Power Requirements (1)

| DEVICE FAMILY | PIN NAME | VOLTAGE (V) | | CPU $I_{MAX}$ (μA/MHz) (2) | ANALOG $I_{MAX}$ (μA) | COMMENTS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | | | |
| x11x1A | $V_{CC}$ | 1.8 | 3.6 | 350 | Comp_A = 60 | C11x1: 300 μA/MHz max |
| F12x | $V_{CC}$ | 1.8 | 3.6 | 350 | Comp_A+ = 60 | |
| F11x2, 12x2 | $V_{CC}$ | 1.8 | 3.6 | 350 | ADC10 = 1200, $I_{REF}$ = 400 | |
| F13x, 14x[1] | $A_{VCC}$, $D_{VCC}$ (3) | 1.8 | 3.6 | 560 | Comp_A = 60,<br>ADC12 = 1600,<br>$I_{REF}$ = 800 | F13x, 14x: Comp_A, ADC12<br>F14x1: Comp_A |
| F15x, 16x, 161x | $A_{VCC}$, $D_{VCC}$ (3) | 1.8 | 3.6 | 600 | Comp_A = 60,<br>ADC12 = 1600,<br>$I_{REF}$ = 800, DAC12 = 1500 | DAC outputs not loaded; DAC12 currents for a single DAC, max of two DAC12s in device) |

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 8-MHz maximum CPU clock speed (ex. Imax_x11x1 = 8 MHz × 350 μA = 2.8 mA). $V_{CC} = D_{VCC} = A_{VCC}$ = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power $A_{VCC}$ and $D_{VCC}$ from the same source. A maximum difference of 0.3 V between $A_{VCC}$ and $D_{VCC}$ can be tolerated.

### Table 3. MSP430x2xx Family Power Requirements (1)

| DEVICE FAMILY | PIN NAME | VOLTAGE (V) | | CPU $I_{MAX}$ (2) (μA/MHz) | ANALOG $I_{MAX}$ (μA) | COMMENTS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | | | |
| F20xx | $V_{CC}$ | 1.8 | 3.6 | 370 | Comp_A+ = 60<br>ADC10 = 1200,<br>ADC10_$I_{REF}$ = 400<br>SD16_A + $I_{REF}$ = 1700<br>RefBuffer = 600 | 20x1: Comp_A+<br>20x2: ADC10<br>20x3: SD16_A |
| F21x1 | $V_{CC}$ | 1.8 | 3.6 | 410 | Comp_A+ = 60 | |
| F21x2 | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 350 | Comp_A+ = 60<br>ADC10 = 1200,<br>$I_{REF}$ = 400 | |
| F22xx | $A_{VCC}$, $D_{VCC}$ (3) | 1.8 | 3.6 | 550 | ADC12 = 1200,<br>$I_{REF}$ = 400<br>OA = 290 | 22x2: ADC10<br>22x4: ADC10, 2 OAs OA currents for a single amplifier |
| F23x0 | $A_{VCC}$, $D_{VCC}$ (3) | 1.8 | 3.6 | 550 | Comp_A + = 60 | |

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 16 MHz maximum CPU clock speed (ex. Imax_20xx = 16 MHz × 370 μA = 5.90 mA). $V_{CC} = D_{VCC} = A_{VCC}$ = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power $A_{VCC}$ and $D_{VCC}$ from the same source. A maximum difference of 0.3 V between $A_{VCC}$ and $D_{VCC}$ can be tolerated during power-up.

### Table 3. MSP430x2xx Family Power Requirements(1) (continued)

| DEVICE FAMILY | PIN NAME | VOLTAGE (V) | | CPU $I_{MAX}$ (2) ($\mu$A/MHz) | ANALOG $I_{MAX}$ ($\mu$A) | COMMENTS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | | | |
| F23x, 24x[1], 2410 | $A_{VCC}$, $D_{VCC}$ (3) | 1.8 | 3.6 | 445 | Comp_A + = 60,<br>ADC12 = 1000,<br>$I_{REF}$ = 700 | 224x1: Comp_A+<br>23x, 24x, 2410: Comp_A+, ADC12 |
| F241x, 261x | $A_{VCC}$, $D_{VCC}$ (3) | 1.8 | 3.6 | 560 | Comp_A + = 60,<br>ADC12 = 1000,<br>$I_{REF}$ = 700<br>DAC12 = 1500 | 241x: Comp_A+, ADC12<br>261x: Comp_A+, ADC12, two DAC12s DAC12 outputs not loaded; DAC12 currents for a single DAC |

### Table 4. MSP430x4xx Family Power Requirements(1)

| DEVICE FAMILY | PIN NAME (2) | VOLTAGE (V) | | CPU $I_{MAX}$ ($\mu$A/MHz) (3) | ANALOG $I_{MAX}$ ($\mu$A) | COMMENTS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | | | |
| x41x | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 350 | Comp_A = 60 | C41x: 300 $\mu$A/MHz max |
| FW42x | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 350 | Comp_A = 60<br>Scan IF = 650 | |
| F42x | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 500 | SD16 + $I_{REF}$ = 1550<br>Ref Buffer = 600 | SD16 current is for a single A/D (three on device) |
| FE42x[a], 42x2 | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 500 | ESP430CE1 = 4900<br>Ref Buffer = 600 | ESP430 current for 4-MHz operation |
| F43x[1], F44x | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 560 | Comp_A = 60,<br>ADC12 = 1600,<br>$I_{REF}$ = 800 | |
| F42x0 | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 520 | SD16_A + $I_{REF}$=1800<br>Ref Buffer = 600<br>DAC12=1500 | DAC12 output not loaded |
| FG42x0 | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 560 | SD16_A + $I_{REF}$=1800<br>Ref Buffer = 600<br>DAC12 = 1500,<br>OA = 290 | DAC12 output not loaded; OA current for a single amplifier (two OAs in device) |
| FG43x | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 570 | Comp_A = 60,<br>ADC12 = 1600,<br>$I_{REF}$ = 800,<br>DAC12 = 1500,<br>OA = 490 | DAC12 outputs not loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device) |
| FG46xx | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 740 | Comp_A = 60,<br>ADC12 = 1600,<br>$V_{REF}$ = 800,<br>DAC12 = 1500,<br>OA = 490 | DAC12 outputs no loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device) |
| F47xx | $A_{VCC}$, $D_{VCC}$ | 1.8 | 3.6 | 560 | Comp_A = 60,<br>SD16_A + $I_{REF}$ = 1700<br>Ref Buffer = 600 | 16 MHz max CUP frequency; SD16 current is for a single A/D (four on device) |

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(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) It is recommended to power $A_{VCC}$ and $D_{VCC}$ from the same source. A maximum difference of 0.3 V between $A_{VCC}$ and $D_{VCC}$ can be tolerated.

(3) 8 MHz maximum CPU clock speed (ex. Imax_x41x = 8 MHz × 350 $\mu$A = 2.8 mA). (F47xx max CPU clock = 16 MHz) $V_{CC} = D_{VCC} = A_{VCC}$ = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately. LCD current not included.

**Table 5. MSP430x5xx Family Power Requirements**[1]

| DEVICE FAMILY | PIN NAME | VOLTAGE (V) | | CPU $I_{MAX}$ (µA/MHz) (2) | ANALOG $I_{MAX}$ (µA) | COMMENTS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | | | |
| F54xx | $A_{VCC}$, $D_{VCC}$ (3) | 2.2 | 3.6 | 348 | ADC12_A = 220,<br>$I_{REF}$ = 190 | 18 MHz maximum CPU clock speed |

(1) Additional 5-mA maximum required when writing/erasing Flash In-system.

(2) 16 MHz maximum at 3-V CPU clock speed. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power $A_{VCC}$ and $D_{VCC}$ from the same source. A maximum difference of 0.3 V between $A_{VCC}$ and $D_{VCC}$ can be tolerated during power-up.

## 4 List of Materials

Table 6 shows the bill of materials (BOM) for this design.

**Table 6. PMP4775 List of Materials**

| REF DES | QTY | VALUE | DESCRIPTION | SIZE | PART NUMBER | MFR |
|---|---|---|---|---|---|---|
| C1, C2 | 2 | 10 µF | Capacitor, ceramic, 6.3 V, X5R, 10% | 0603 | C1608X5R0J106KT | TDK |
| L1 | 1 | 2.2 µH | Inductor, SMT, 1.5A, 110 mΩ | 0.102" x 0.110" | VLF3010AT-2R2M1R0 | TDK |
| R1 | 1 | 453 kΩ | Resistor, chip, 1/16W, 1% | 0603 | Std | Std |
| R2 | 1 | 100 kΩ | Resistor, chip, 1/16-W, 1% | 0603 | Std | Std |
| U1 | 1 | | 3-MHz synchronous step-down converter, 500-mA, adjustable | QFN-10 | TPS62300DRC | TI |

## 5 Test Results

The input and output startup waveforms are shown in Figure 1 through Figure 4. The output ripple voltage is shown in Figure 5. Figure 6 shows the transient response. The switching node waveform is shown in Figure 7.

### *5.1 Test Results*

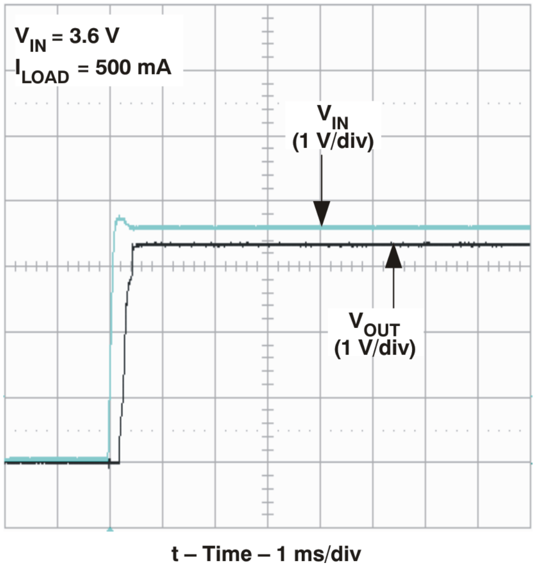

**Figure 1. Startup**

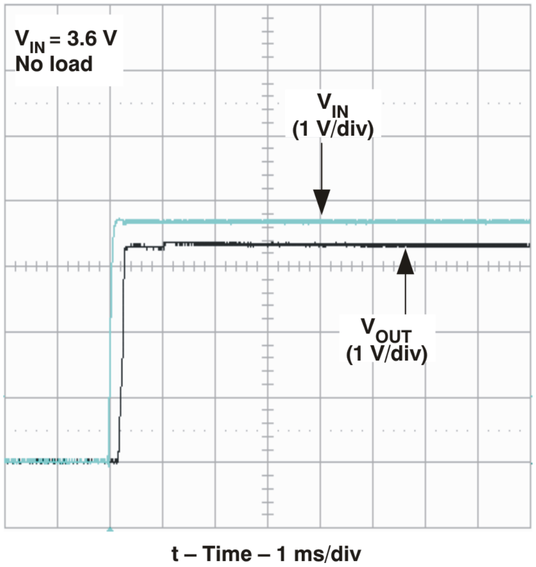

**Figure 2. Startup**

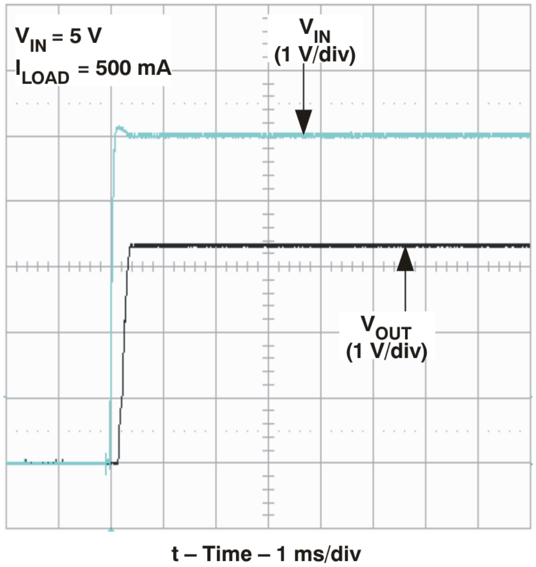

**Figure 3. Startup**

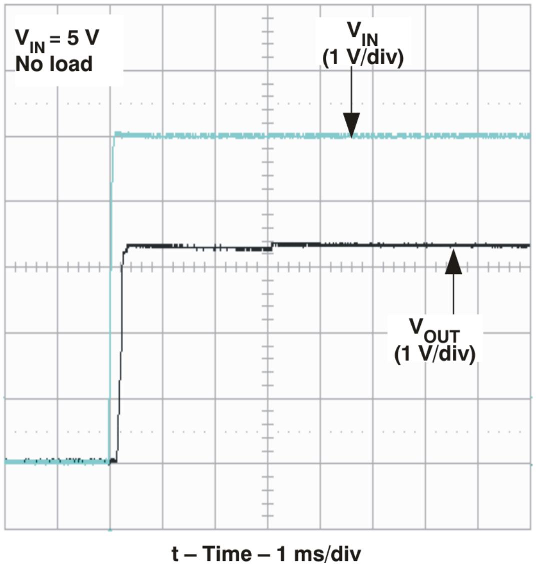

**Figure 4. Startup**

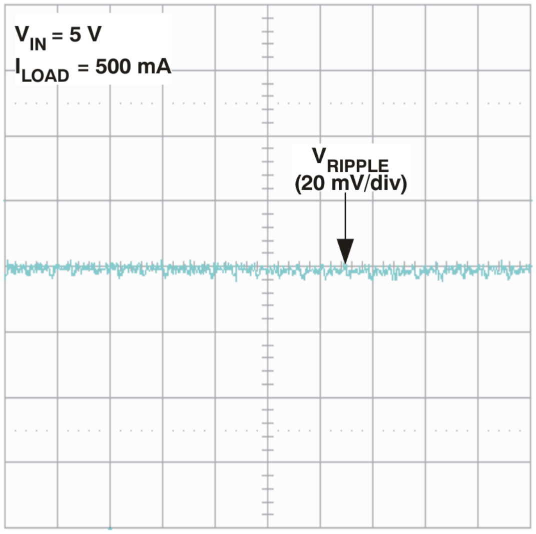

**Figure 5. Output Ripple Voltage**

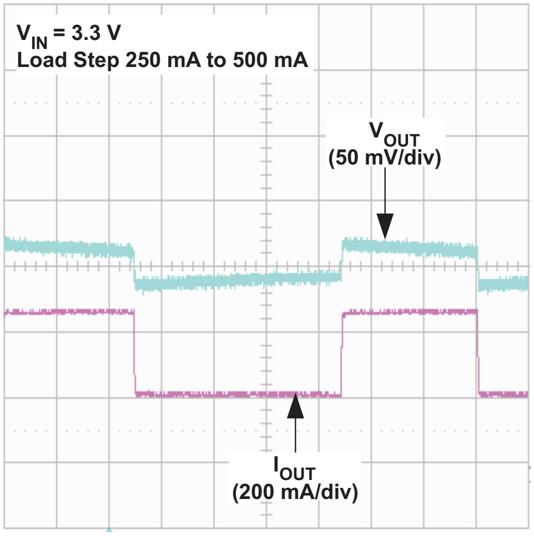

**Figure 6. Load Transient**

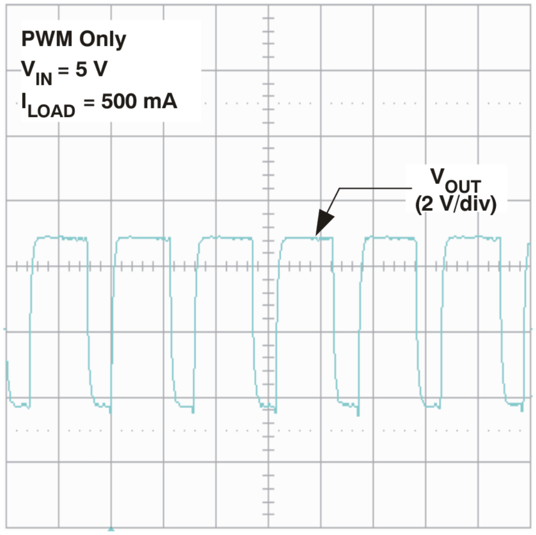

**Figure 7. Switching Node Waveform**

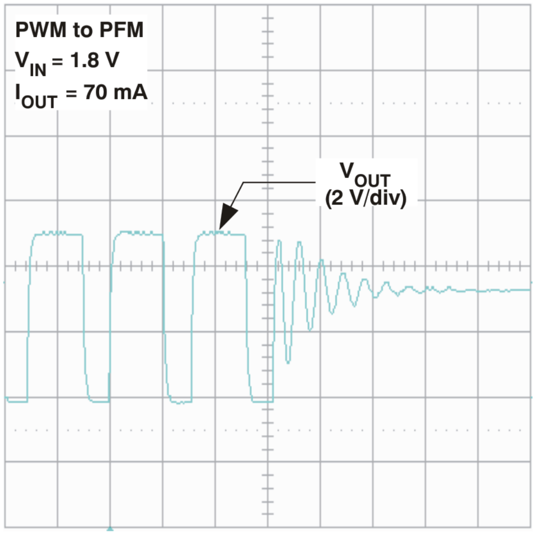

**Figure 8. Switching Node Waveform**

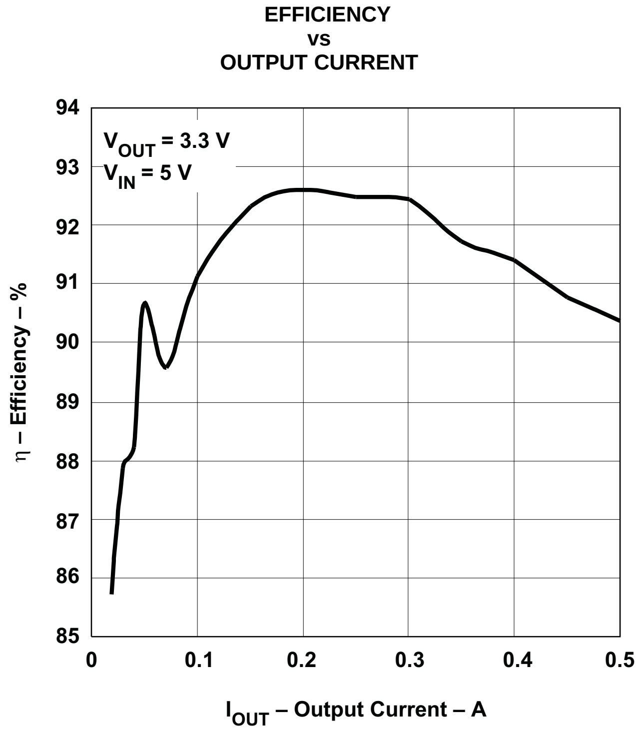

Figure . Figure 9.

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