Advanced Adapter ORing Solutions using the TPS23753

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ABSTRACT

The TPS23753 has a number of features that simplify ORing of Power over Ethernet (PoE) and ac-powered adapters. These features are integrated into the powered device (PD) and dc/dc controller to provide an integrated solution set. This application note explores these features and provides other critical information.

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1 Introduction

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used regardless of PoE availability. Whereas most applications only require that the two sources coexist, the TPS23753 is designed to ease power-source control.

The TPS23753 is a combined PoE PD interface and current-mode dc/dc controller specifically optimized for isolated converter designs. The TPS23753 supports a number of input voltage ORing options including natural high voltage, external adapter preference, and PoE preference.

Figure 1 illustrates three options for diode ORing external power into a PD. Only one of the following options would be used in any particular design. Each insertion point has unique voltage, inrush current, and power handoff (i.e., handoff from PSE to the adapter and vice versa) profiles.

The TPS23753 simplifies supply ORing through use of the V_{DD1}, APD, and DEN pins. The APD and DEN pins can be used to disable the internal hotswap MOSFET and class regulator while the separate V_{DD1} pin allows isolation of the PoE input and converter supply voltages. The ability to disable the internal hotswap MOSFET is necessary for both option 2 and 3 adapter preference configurations while the independent V_{DD1} pin simplifies PoE preference configuration for option 2.

Adapter input ORing diodes are shown for all the options to protect against a reverse input voltage or short on the input pins, protection of low-voltage adapters from 48V, and to allow a natural ORing of PoE and auxiliary voltage. ORing is sometimes accomplished with a MOSFET in option 3.

2 Power Insertion

Option 1 applies power to the TPS23753 PoE input, option 2 inserts power between the TPS23753 PoE section and the converter, and option 3 applies power to the output side of the PoE power converter. Each of these options has advantages and disadvantages. The wall adapter must meet a minimum 1500-Vac dielectric withstand test voltage between the output and all other connections for options 1 and 2. The adapter only needs 1500-Vac isolation for option 3 if it is not provided by the converter.

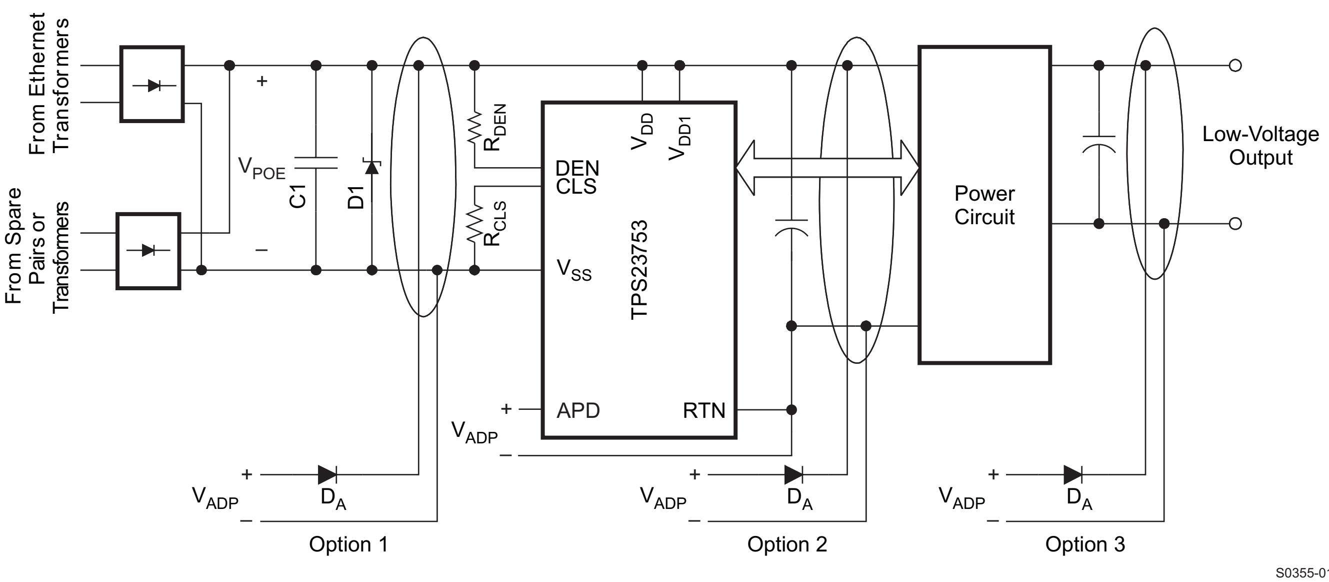

Figure 1. Power Insertion Options

Considerations for each ORing option and source preference is outlined below.

Option 1

- General
  - Requires 48-V, isolated output (from mains and ground) adapter
- Benefits
  - Adapter inrush current is managed when the PoE source (PSE) is not present.
- Limitations
  - The PSE cannot detect and power the PD if adapter power is present first.
    - PSE priority is difficult
    - Adapter priority requires circuitry to disable the PoE input.
  - Adapter inrush current is not managed when PSE is present.
    - Plugging in a higher-voltage adapter causes a large momentary current surge.
    - Insertion of a higher-voltage-magnitude adapter may cause the PD to restart due to PD current limit.
  - The larger-voltage-magnitude source (PoE or adapter) provides power when both sources are present.
    - Natural ORing effect
    - Adapter priority requires a relay-like solution to open the PoE input.
    - A lower-voltage PSE may power off.

Option 2

- General
  - Requires 12-V–48-V, isolated output (from mains and ground) adapter.
  - Lower-voltage adapters typically used when product family predates PoE.
- Benefits
  - Using the APD feature feature is a simple way to achieve adapter power preference.
  - Separating V_{DD} and V_{DD1} with a diode is a simple way of achieving PoE preference.
    - Easiest with 12-V or 24-V adapters
- Limitations
  - Adapter hot-plug (adapter powered before insertion into PD) can cause large inrush current from adapter.
    - This is not generally viewed as an issue.
  - Wide input operating voltage (12-V–48-V) converters typically are larger and/or less efficient than a 48-V-only converter.
  - The PD will usually restart when adapter preference is used and adapter power goes away.
  - Many adapter voltage and loading combinations guarantee that PoE preference will cause a restart as PoE takes over.
  - PoE preference and 48V adapters require extra circuits to over-ride natural diode ORing.
  - Option 3 provides a more optimal solution for 12-V adapters.

Option 3

- General
  - Power is ORed to the PoE converter output.
  - Grounded output adapter may be used if the converter isolates the primary to the secondary.
  - PoE and adapter may be ORed with diodes or MOSFETs for better efficiency.
  - PoE operation may be disabled when secondary power is present using DEN.
- Benefits
  - Most optimal and efficient method of ORing 12-V (or lower) adapters.
  - Permits wider choice of low-voltage adapters.
- Limitations
  - Adapter preference using DEN requires extra circuit.
  - Difficult to use with synchronous rectifiers in the converter.

3 TPS23753 Internal Support Feature

Table 1. Solution Summary

Source Priority	Option 1	Option 2	Option 3
PoE priority	PoE present first and $V_{POE} > V_{ADP}$, APD < 1.0 V No viable solution if ADP is present first.	APD < 1.0 V, $V_{POE} > V_{ADP}$, Separate V_{DD} and V_{DD1} with diode Requires additional circuit when $V_{POE} < V_{ADP}$	$V_{OUT} > V_{ADP}$ Use Diode ORing or MOSFET ORing on adapter.
Adapter priority	Adapter present first. Requires additional circuit to handle PoE present first and $V_{POE} > V_{ADP}$. APD < 1.0 V	APD > 1.5 V, V_{DD} connected to V_{DD1}	$V_{DEN} = V_{SS}$ disables the internal hotswap MOSFET Synchronous converter requires output blocking MOSFET

3.1 Option 1 ORing

Figure 2 shows a simple implementation for ORing option 1. Because ORing option 1 furnishes power through the internal hot-swap MOSFET, the PD selects the source based on the voltage and order.

3.1.1 Case 1: PSE Powers PD

The PSE powers the PD when PSE voltage is applied before, and is greater than the adapter voltage. The PSE continues to furnish power to the PD in the presence of an adapter voltage source as long as the PSE voltage is greater than that of the adapter. When the PSE and adapter voltages are nearly equal, some sharing between the sources may occur. The PSE may drop the PD due to PD current being below the dc maintain power signature (MPS) of 10 mA. Once the PSE drops the PD and an adapter source is present, PSE detection is blocked.

3.1.2 Case 2: Adapter Powers PD

The adapter powers the PD when the adapter voltage is greater than the PSE voltage. Once the adapter source is present and powering the PD, detection by the PSE is blocked.

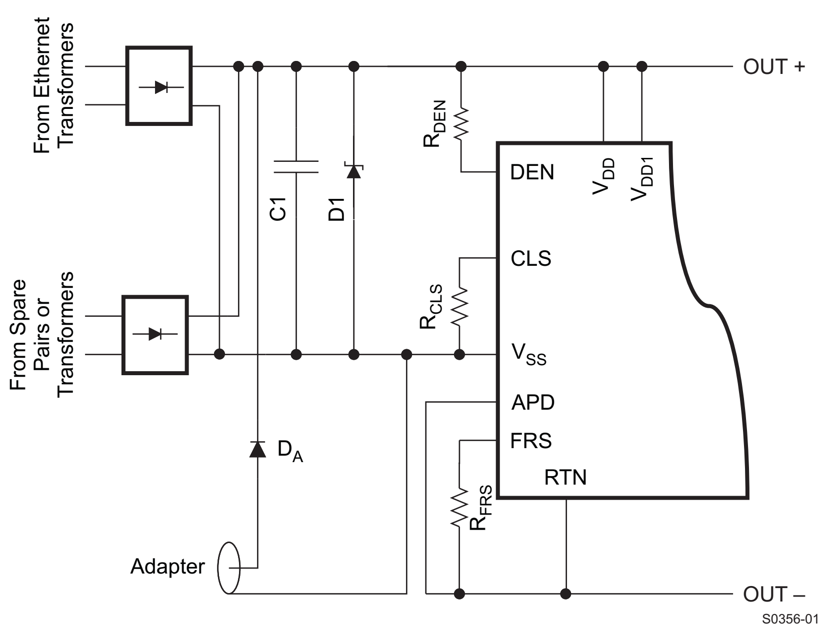

Figure 2. Option 1 ORing

3.2 Option 2, PoE Preference

Figure 3 illustrates a simple circuit for option 2, PoE preference implemented by the use of a diode, D_{VDD}. PoE preference is accomplished by blocking adapter voltage from the PD section through the use of D_{VDD}, allowing normal detection and classification to occur. Adapter and PoE voltages are diode ORed together, meaning that PSE power is drawn as long as the adapter voltage is less than the PoE-derived voltage from V_{DD1} to RTN. If the PD is adapter-powered before PSE power is applied, D_{VDD} blocks adapter voltage from V_{DD}-V_{SS}, permitting detection and classification. When the PSE applies full 48-V power, the converter momentarily turns off as the bulk capacitor is charged, then restarts. If PoE power drops while the adapter is present, converter operation should be unaffected.

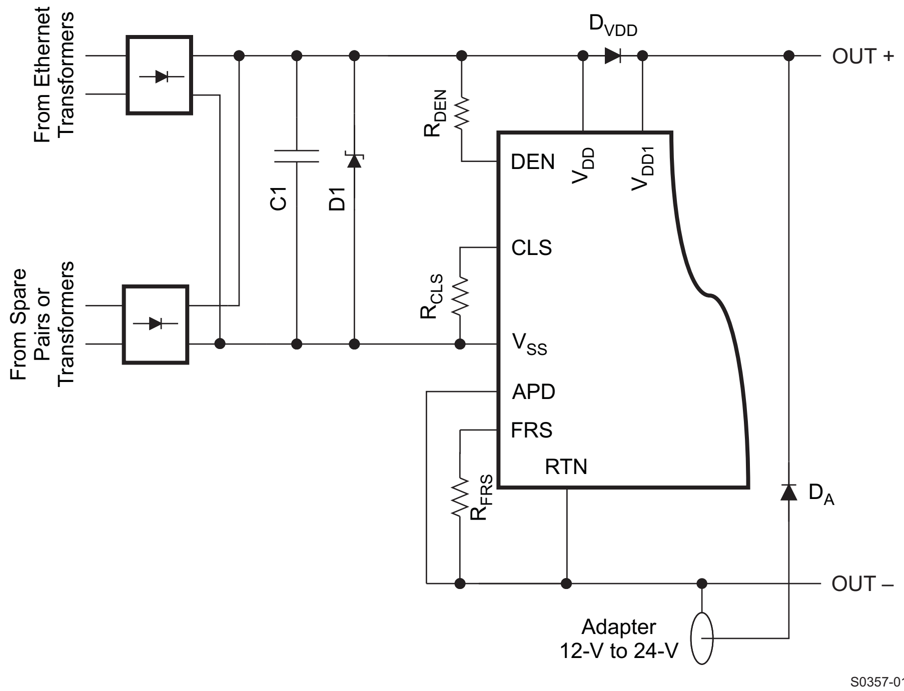

Figure 3. Use of Diode D_{VDD} for PoE Preference

The highest voltage source (as see by V_{DD1}) will supply power if a 48-V adapter is used with this solution due to diode ORing. When the adapter voltage is greater than the PoE voltage, the PSE will stop supplying current and could turn off due to dc MPS. The PSE continues to restart and drop the PD as long as adapter power is present. Figure 4 illustrates the use of additional control circuitry to open the adapter input connection if a PSE is sensed. This removes the restriction of only using lower-voltage adapter sources to achieve PoE priority.

The *PoE Present* block must be designed so that it does not interfere with the detection signature resistor. The adapter switch, SW, will be opened whenever PoE running voltage is present. This forces the power to come from PoE, even if the adapter voltage is higher.

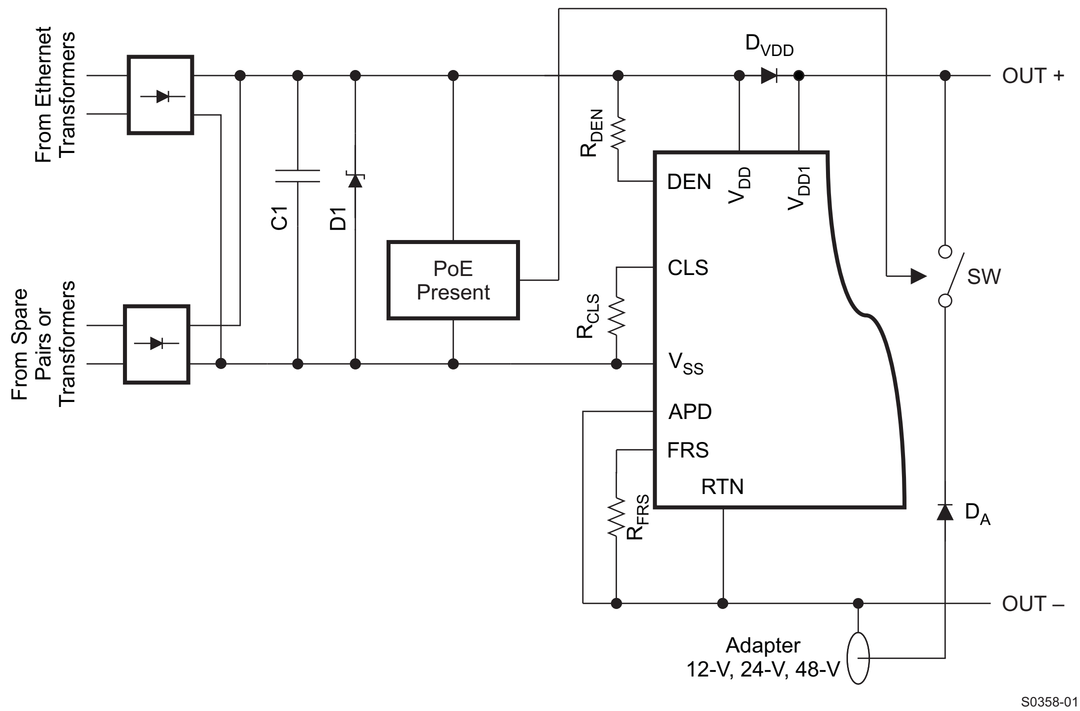

Figure 4. Use of Additional Circuitry to Provide PoE Priority Including 48-V Adapters

Several options for the *PoE present* and *SW* blocks are possible. Figure 5 illustrates the use of a zener diode (D_P), NPN transistor (Q_P), and several resistors to sense the presence of a PSE and open the adapter input connection. D_P blocks the Q_P and bias resistor impedance during PSE detection and classification. When PSE voltage is applied, Q_P turns on, which in turn opens the adapter input switch (M_A) through PNP transistor Q_A.

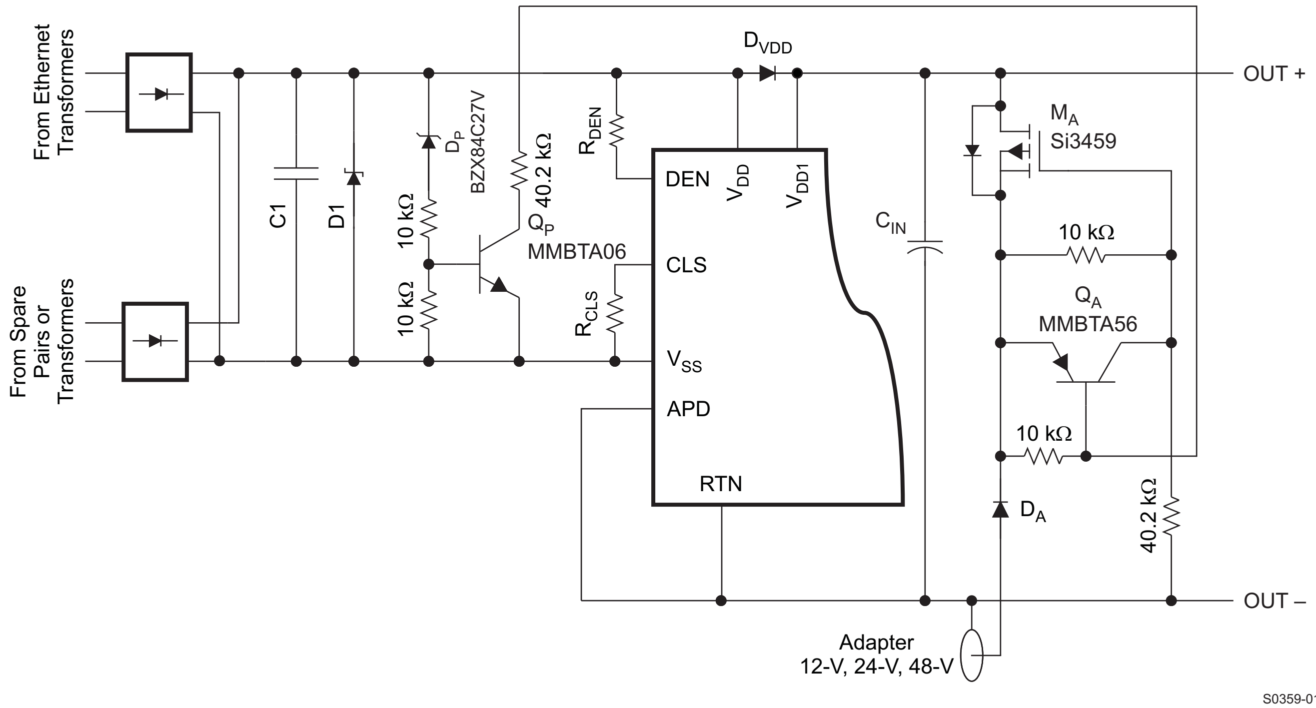

Figure 5. PoE Priority Circuit Using Controlled Adapter High-Side Switch

Figure 6 illustrates the use of a zener diode (D_P), bias resistor, and opto-isolator (U_P), to sense the presence of a PSE and open the adapter input connection. D_P blocks the U_P and bias resistor impedance during PSE detection and classification. When PSE voltage is applied, U_P turns on, which in turn opens the adapter input switch (M_A). Note that the opto-isolator (U_P) is only used as a level shifter.

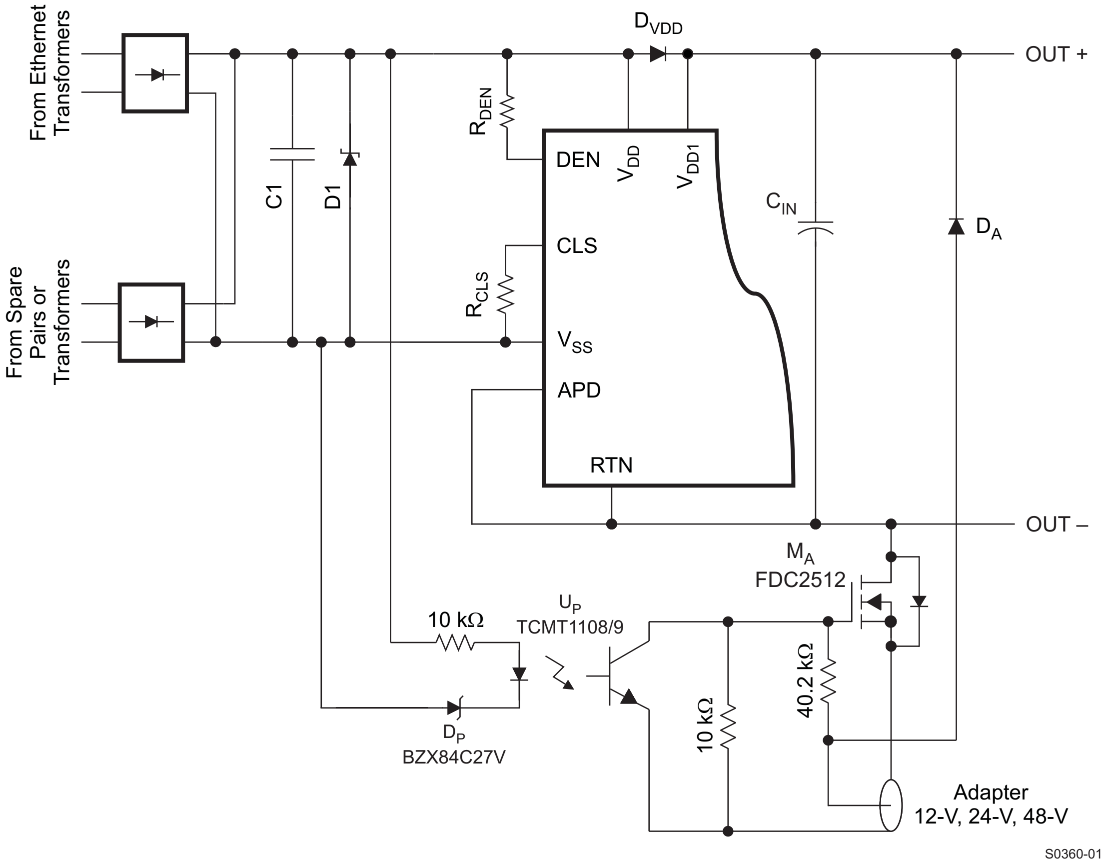

Figure 6. PoE Priority Circuit Using Controlled Adapter Low-Side Switch

When D_{VDD} is used, additional protection of the TPS23753 internal hotswap MOSFET may be required. ESD events at the equipment terminals may cause large stresses in the hotswap MOSFET if DVDD becomes reverse biased and blocks transient current flow around the TPS23753. This effect is highly dependent on the individual design. For example, some designs may not be exposed to transients applied between the converter output and PoE input. The use of C_{VDD} and D_{RTN} as shown in Figure 7 provides additional protection should over-stress of the TPS23753 be an issue. As with D1, the SMAJ58A (or a part with equal to or better performance), is recommended for general indoor applications. Outdoor applications require more extensive protection to lightning standards.

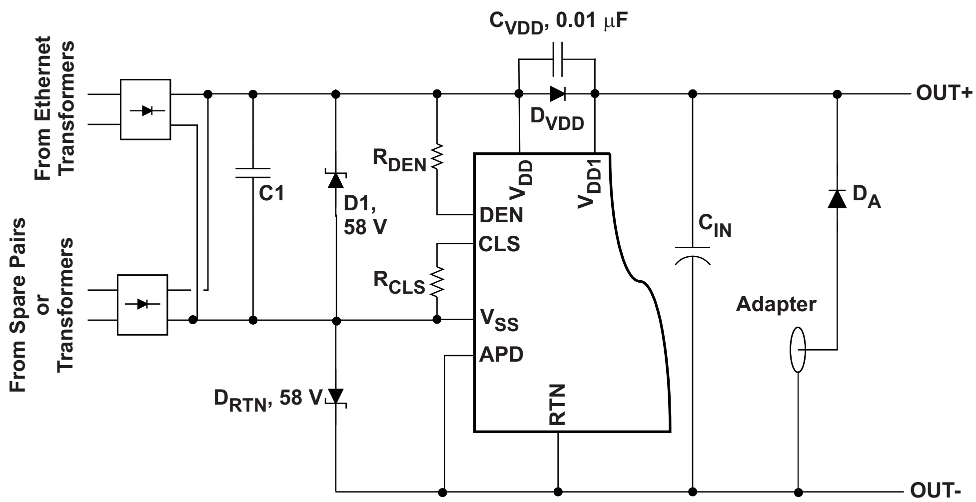

Figure 7. Additional ESD Protection With PoE Priority

3.3 Option 2, Adapter Preference and APD

Figure 8 illustrates an efficient, low-cost circuit for Option 2, adapter preference, using the APD pin function. Adapter preference is accomplished by applying voltage to the APD pin with respect to RTN, forcing the internal hot-swap MOSFET to open. If the PD is operating from PoE power before a live adapter is inserted, the internal hot-swap MOSFET opens, forcing power to come from the adapter. The PSE may then drop power due to the PD current being below dc MPS. An adapter-powered PD is not successfully detected by a compliant PSE because the reverse-biased input bridge blocks the probing.

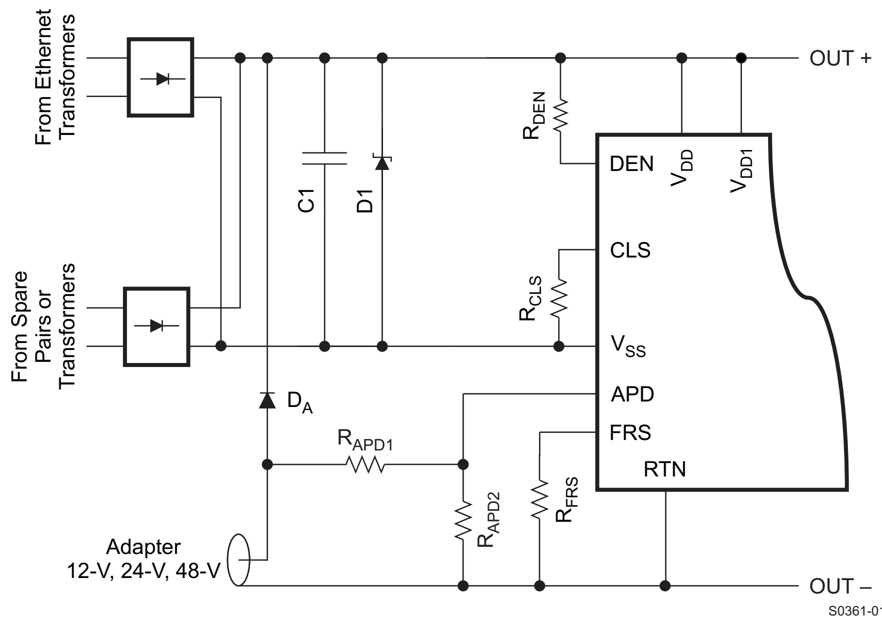

Figure 8. Adapter Preference Using the APD Pin Function

If the adapter source is removed or loses power, the PD will turn off while the PSE goes through a full detection, classification, and startup cycle. This assumes that the PSE had turned off due to a lack of dc MPS.

R_{APD1} and R_{APD2} provide ESD protection, leakage discharge for D_A, and input voltage qualification. Input voltage qualification can reduce or eliminate the occurrence of PD drop out when a slowly rising adapter input voltage is applied. Input voltage qualification can also be used to prevent converter start up issues due to operation at low voltage - high current conditions. The APD divider ratio should be chosen with consideration given to APD pin maximum recommended input voltage, class regulator and resistor power dissipation, and adapter-disable threshold. The following example illustrates selection of R_{APD1} and R_{APD2}.

1. To prevent the converter from operating at an excessively low adapter voltage, choose a startup voltage, V_{START} approximately 75% of nominal. Assuming that the adapter output is 48V +/- 10%, this provides 15% margin below the minimum adapter operating voltage.
2. Choose V_{START} = 48 × 0.75 = 36 V.
3. Select R_{APD2} considering power dissipation. Choose R_{APD2} = 3.01 kΩ

$$DR_{APD} = \frac{Vin_{MIN}}{V_{APDEN}} = \frac{36\text{ V}}{1.5\text{ V}} = 24$$

$$R_{APD1} = R_{APD2} \times \left(DR_{APD} - 1\right) = 3.01\text{ k}\Omega \times 23 = 69.23\text{ k}\Omega \quad (1)$$

4. Choose R_{APD1} = 69.8 kΩ
5. Check the adapter turnon voltage.

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \times V_{APDEN} = \frac{72.81\text{ k}\Omega}{3.01\text{ k}\Omega} \times 1.5\text{ V} = 36.3\text{ V} \quad (2)$$

6. Check the adapter turnoff voltage.

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \times \left(V_{APDEN} - V_{APDH}\right) = \frac{72.81\text{ k}\Omega}{3.01\text{ k}\Omega} \times 1.2\text{ V} = 29\text{ V} \quad (3)$$

7. Check the APD pin voltage at maximum adapter input

$$V_{APD} < \frac{Vin_{MAX}}{\left(\frac{R_{APD1} + R_{APD2}}{R_{APD2}}\right)} = \frac{48 \times 1.1\text{ V}}{\left(\frac{72.81\text{ k}\Omega}{3.01\text{ k}\Omega}\right)} = 2.19\text{ V} \quad (4)$$

8. V_{APD} is less than V_B and so is within the recommended maximum.

APD turns the class regulator off when the input voltage is above the threshold. When low-voltage adapters are to be used, the APD pin divider can be chosen with class regulator and class resistor power dissipation in mind. With lower APD divider ratios, caution must be exercised to avoid damage to the APD pin if used with a higher-voltage adapter.

3.4 Option 3, PoE Priority

In applications where a regulator is to follow the PoE converter V_{OUT}, an option-3 ORing topology can be used as shown in Figure 9. To achieve PoE preference using option-3 ORing, the adapter voltage V_{ADP} must be less than the PoE output voltage, V_{OUT}, to prevent the PSE from potentially removing power due to dc MPS. When used with a secondary-side synchronous rectifier, this circuit needs special attention to turn the rectifier off when the adapter takes over. This prevents power from flowing backwards and powering the primary side of the converter.

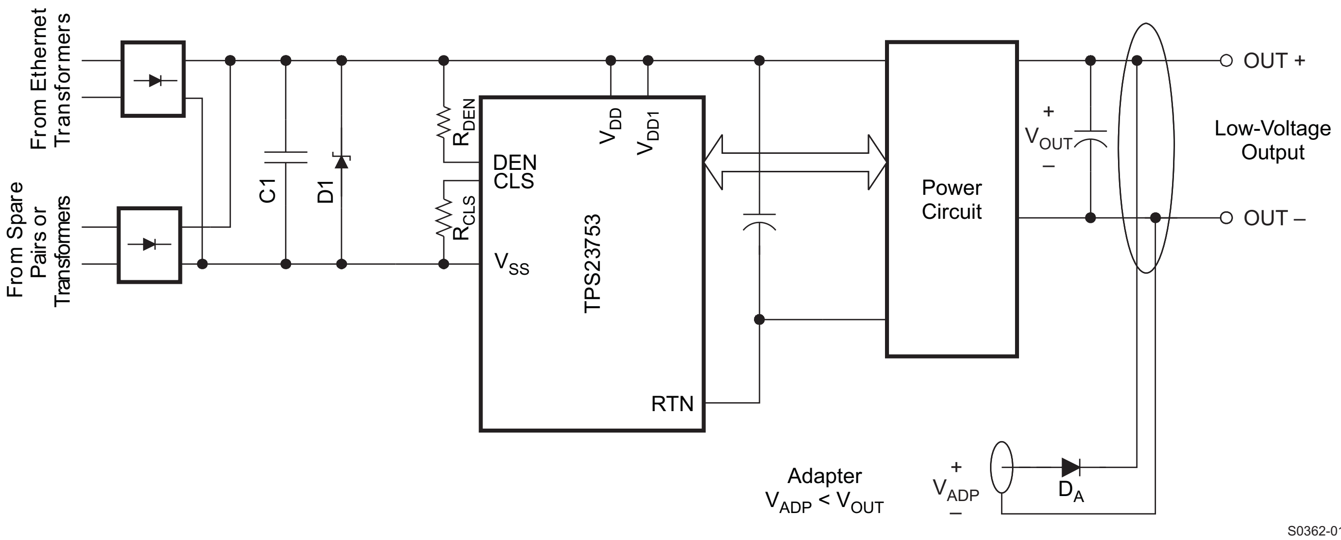

Figure 9. Option 3 With PoE Preference

3.5 Option 3, Adapter Priority

Applications using option 3 with adapter priority may want to disable the PSE source. The TPS23753 allows the PoE input to be turned off using the DEN pin, thereby disabling the internal hot-swap MOSFET and class regulator.

This may be accomplished using the circuit of Figure 10. When the opto-coupler diode is driven and the TPS23753 is powered by the PSE, the internal hot-swap MOSFET is turned off and the converter stops drawing PSE power. A PSE that monitors the dc MPS turns port power off after ~400 ms. The choice of resistors on DEN skews the detection signature outside the acceptable range, preventing a compliant PSE from re-powering the PD. When an adapter is removed, the PD will turn off until the PSE completes its detection – classification – startup sequence. This approach also has the same problem with synchronous rectifiers. Take care to disable them when the output is powered from the adapter.

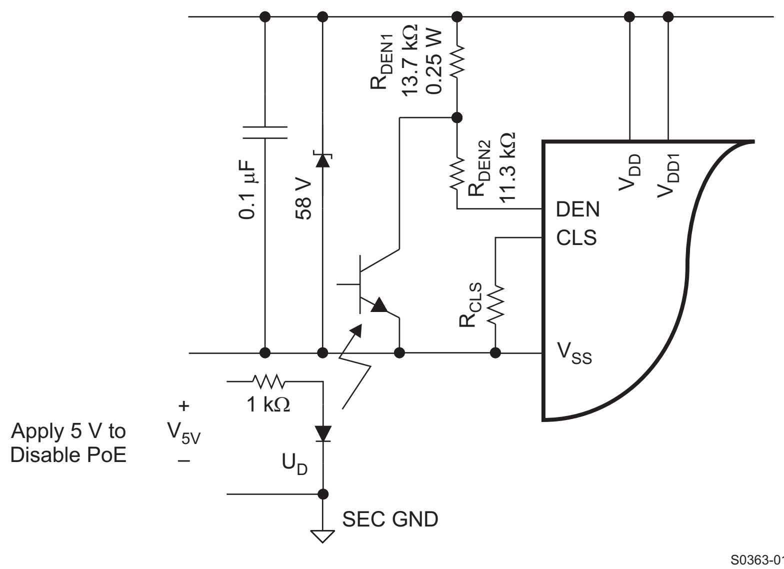

Figure 10. Use of the DEN Pin to Disable the PoE MOSFET

Selection of the resistor divider (R_{DEN1} and R_{DEN2}) on DEN takes a bit of compromise to provide both an invalid detection signature resistance, and a current below the dc MPS threshold. The PSE must reject a PD signature below 15 kΩ, and disconnect a PD drawing less than 5 mA. From the PD side, an invalid detection signature is less than 12 kΩ, and the PD must draw at least 10 mA to remain connected. The R_{DEN1} value shown causes an invalid detection signature to be presented to the PSE, and presents approximately 4 mA to the PSE at maximum PSE output voltage.

The opto-coupler (U_D) transistor must be rated for at least 70 V. A high current transfer ratio (CTR) of 300%–400% is suggested to reduce the amount of control (V_{5V}) current, but this is not a hard requirement. R_{DEN2} is chosen so that the R_{DEN1} and R_{DEN2} total resistance is approximately 25 kΩ.

3.6 Keeping the PSE Powered With Options 2 and 3

In many of the previous adapter priority sections, the PSE drops the PD when the adapter is present. To prevent this, the circuit shown in Figure 11 can be used to draw enough current to satisfy the MPS. It should be noted that this power is dissipated all the time the adapter is present. D_{VDD} is present to allow a PSE to detect the PD if it becomes active after the adapter is powering the PD. DP blocks the bias resistor impedance during PSE detection and classification. The bias resistor is chosen to provide at least 10 mA MPS current even if an adapter is powering the converter.

Alternatively, an opto-isolator could be used to detect the presence of adapter voltage (through opto LED and bias resistor) and switch in the 10mA bias current at the PoE input.

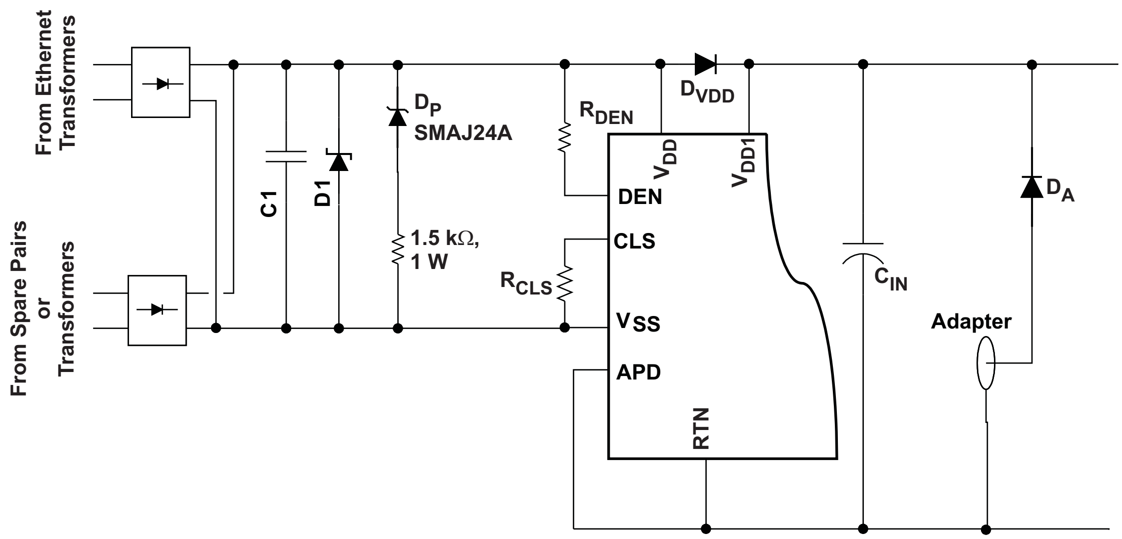

Figure 11. Keeping the PSE Source On in the Presence of an Adapter Source

This circuit works well for an Option 3, although the PoE converter has a small delay before it goes from inactive to supplying power. When used in Option 2, this works best with a 48-V adapter. If the PSE power comes up after the adapter, there is a short power interruption as the PD state machine completes its inrush cycle.

4 Conclusion

The TPS23753 provides expanded adapter ORing options through the use of the V_{DD1}, APD, and DEN pins. This high degree of flexibility simplifies adapter ORing options and provides a robust, reliable design.

5 References

1. *TPS23753 IEEE 8023-2005 PoE Interface and Isolated Converter Controller* data sheet (SLVS853)

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