Application Report
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Application of the MC34063 Switching Regulator

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ABSTRACT

This application report provides the features that are necessary to implement dc-to-dc fixed-frequency schemes with a minimum number of external components using the MC34063. This device represents significant advancements in ease of use with highly efficient and, yet, simple switching regulators. The use of switching regulator is becoming more pronounced over that of linear regulators, because of the size and power-efficiency requirement of new equipment designs. The use of switching regulators increases application flexibility and reduces the cost.

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1 MC34063 Description

The MC34063 is a monolithic control circuit containing all the active functions required for switching dc-to-dc converters (see Figure 1). The MC34063 includes the following components:

- Temperature-compensated reference voltage
- Oscillator
- Active peak-current limit
- Output switch
- Output voltage-sense comparator

The MC34063 was designed to be incorporated in buck, boost, or voltage-inverter converter applications. All these functions are contained in an 8-pin DIP or SOIC package.

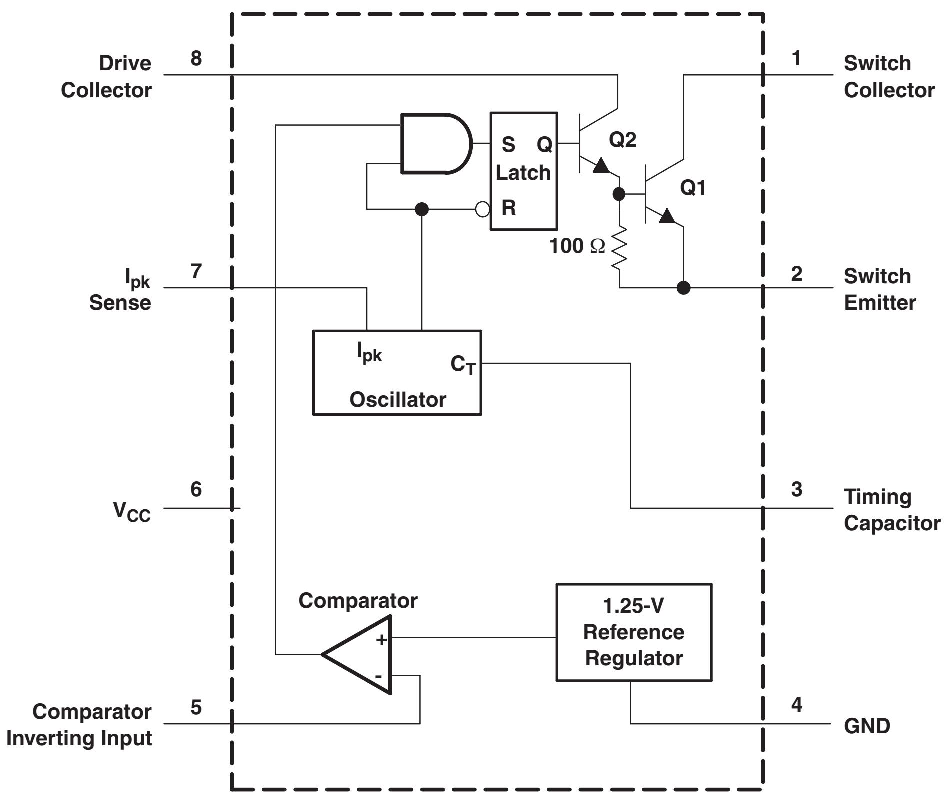


Figure 1. Functional Block Diagram

1.1 Reference Voltage

The reference voltage is set at 1.25 V and is used to set the output voltage of the converter.

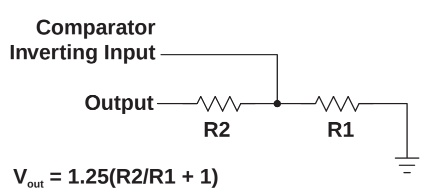


Figure 2. Reference Voltage Circuit

1.2 Oscillator

The oscillator is composed of a current source and a current sink that charge and discharge the external timing capacitor (C_T) between an upper and lower preset threshold. The typical charge current is 35 µA, and the typical discharge current is 200 µA, yielding approximately a 6:1 ratio. Thus, the ramp-up period is six times longer than that of the ramp-down period (see Figure 3).

The upper threshold is 1.25 V, which is same as the internal reference voltage, and the lower threshold is 0.75 V. The oscillator runs constantly, at a pace controlled by the value of C_T.

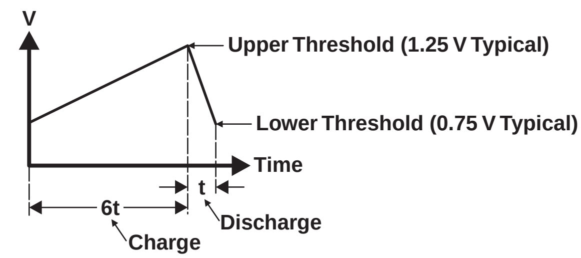


Figure 3. Oscillator Voltage Thresholds

1.3 Current Limit

Current limit is accomplished by monitoring the voltage drop across an external sense resistor located in series with V_{CC} and the output switch. The voltage drop developed across the sense resistor is monitored by the current-sense pin, I_{pk}. When the voltage drop across the sense resistor becomes greater than the preset value of 330 mV, the current-limit circuitry provides an additional current path to charge the timing capacitor (C_T) rapidly, to reach the upper oscillator threshold and, thus, limiting the amount of energy stored in the inductor. The minimum sense resistor is 0.2 Ω. Figure 4 shows the timing capacitor charge current versus current-limit sense voltage. To set the peak current, I_{pk} = 330 mV/R_{sense}.

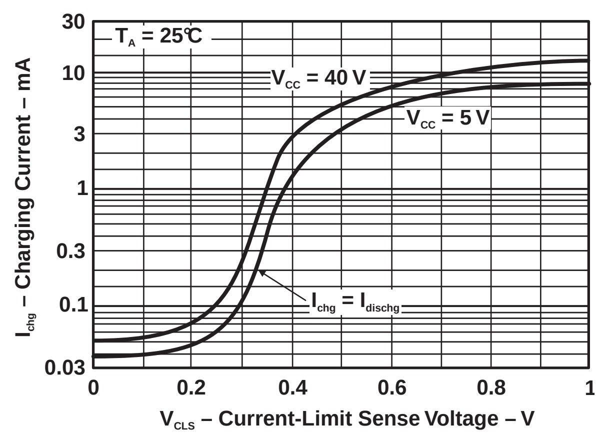


Figure 4. Timing Capacitor Charge Current vs Current-Limit Sense Voltage

1.4 *Output Switch*

The output switch is an NPN Darlington transistor. The collector of the output transistor is tied to pin 1, and the emitter is tied to pin 2. This allows the designer to use the MC34063 in buck, boost, or inverter configurations. The maximum collector-emitter saturation voltage at 1.5 A (peak) is 1.3 V, and the maximum peak current of the output switch is 1.5 A. For higher peak output current, an external transistor can be used. Figure 5 shows the typical operation waveforms.

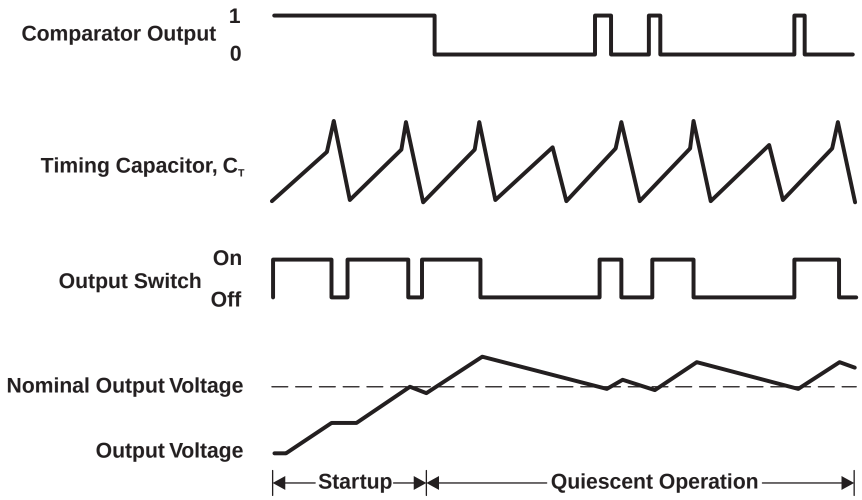


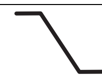
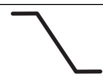
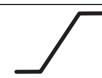
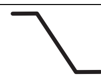
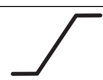
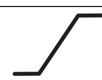
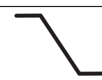
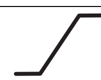
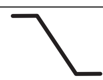
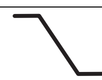
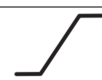
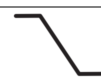
Figure 5. Typical Operation Waveforms

2 Functional Description

The oscillator is composed of a current source and sink, which charge and discharge the external timing capacitor (C_T) between an upper and lower preset threshold. The typical charge and discharge currents are 35 mA and 200 mA, respectively, yielding approximately a 6:1 ratio. Thus, the ramp-up period is six times longer than that of the ramp-down period (see Figure 3). The upper threshold is equal to internal reference voltage of 1.25 V, and the lower threshold is approximately equal to 0.75 V. The oscillator runs continuously at a rate controlled by the value of C_T.

During the ramp-up portion of the cycle, a logic 1 is present at the A input of the AND gate. If the output voltage of the switching regulator is below nominal, a logic 1 is also present at the B input. This condition sets the latch and causes the Q output to be a logic 1, enabling the driver and output switch to conduct. When the oscillator reaches its upper threshold, C_T starts to discharge, and a logic 0 is present at the A input of the AND gate. This logic level is also connected to an inverter whose output presents a logic 1 to the reset input of the latch. This condition causes Q to go low, disabling the driver and output switch. A logic truth table of these functional blocks is shown in Table 1.

Table 1. Logic Truth Table of Functional Blocks

Active Condition of Timing Capacitor, C_T	AND Gate Inputs		Latch Inputs		Output Switch	Comments
	A	B	S	R		
Begin ramp up		0	0		0	Regulator output is greater than or equal to nominal (B = 0).
Begin ramp down		0	0		0	No change, because B was 0 before C_T ramp down.
Ramping down	0		0	1	0	No change even though regulator output less than nominal. Output switch cannot be initiated during R_T ramp down.
Ramping down	0		0	1	0	No change, because output switch condition was terminated when A = 0.
Ramping up	1			0		Regulator output became less than nominal during C_T ramp up (when B changed to 1). Partial on cycle for output switch.
Ramping up	1			0	1	Regulator output became greater than or equal to nominal (B changed to 0) during ramp up of C_T. No change, because B cannot reset the latch.
Begin ramp up		1				Complete on cycle, because B = 1 before C_T ramp up started.
Begin ramp down		1				Output switch conduction is always terminated when C_T is ramping down.

The output of the comparator can set the latch only during the ramp up of C_T and can initiate a partial or full on cycle of output switch conduction. Once the comparator has set the latch, it cannot reset it. The latch remains set until C_T begins ramping down. Thus, the comparator can initiate output switch conduction but cannot terminate it, and the latch is always reset when C_T begins ramping down. The comparator's output is at a logic 0 when the output voltage of the switching regulator is above nominal. Under these conditions, the comparator's output can inhibit a portion of the output switch on cycle, a complete cycle, a complete cycle plus a portion of one cycle, multiple cycle, or multiple cycles plus a portion of one cycle.

3 Buck Regulator

Figure 6 shows the basic buck switching regulator. Q1 interrupts the input voltage and provides a variable duty-cycle square wave to an LC filter. The filter averages the square wave and produces a dc output voltage that can be set to any level less than the input by controlling the percent conduction time of Q1 to that of the total switching cycle time.

$V_{out} = V_{in}(\%t_{on})$
or
$V_{out} = V_{in}(t_{on}/(t_{on} + t_{off}))$

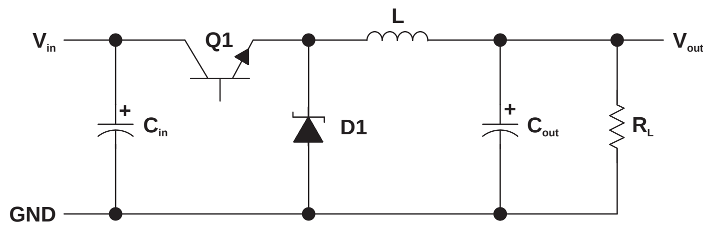


Figure 6. Buck Regulator

3.1 Buck Converter Operation

As an example, suppose that the transistor Q1 is off, the inductor current (I_L) is zero, and the output voltage is at its nominal value. The output voltage across capacitor C_{out} will ultimately decay below the nominal output level, because it is the only source of supply current to load R_L. This voltage deficiency is sensed by the switching control circuit and causes Q1 to turn on. The inductor current starts to flow from V_{in} through Q1 and C_{out} in parallel with R_L, and it rises at a rate of $\Delta I/\Delta t = V/L$. The voltage across the inductor is equal to $V_{in} - V_{sat} - V_{out}$, and the inductor peak current at any instant is calculated as shown here:

$I_L = ((V_{in} - V_{sat} - V_{out})/L)t$

At the end of the on period, Q1 is turned off. As the magnetic field in the inductor starts to collapse, it generates a reverse voltage that forward biases D1, and the peak current decays at a rate of $\Delta I/\Delta t = V/L$ as energy is supplied to C_{out} and R_L. The voltage across the inductor during this period is equal to $V_{out} + V_F$ of D1. The current as a function of time is calculated as shown here:

$I_L = I_{L(pk)} - ((V_{out} + V_F)/L)t$

Where V_F is the forward voltage of D1.

3.2 Time-On and Time-Off Calculation

As an example, suppose that during quiescent operation, the average output voltage is constant, and the system is operating in the discontinuous mode. Then $I_{L(pk)}$ attained during t_{on} must decay to zero during t_{off}, and a ratio of t_{on} to t_{off} can be determined.

$((V_{in} - V_{sat} - V_{out})/L)t_{on} = ((V_{out} + V_F)/L)t_{off}$
$\therefore\ t_{on}/t_{off} = (V_{out} + V_F)/(V_{in} - V_{sat} - V_{out})$

3.3 Switch Peak Current Calculation

The volt-time product of t_{on} must be equal to that of t_{off}, and the inductance value is not a factor when determining their ratio. If the output voltage inside a switching period is to remain constant, the average current into the inductor must be equal to the output current for a complete cycle. The peak inductor current with respect to output current is:

$(I_{L(pk)}/2)t_{on} + (I_{L(pk)}/2)t_{off} = I_{out}t_{on} + I_{out}t_{off}$
$\therefore\ I_{L(pk)} = 2I_{out}$

3.4 Timing Capacitor Calculation

The peak inductor current is also equal to the peak switch current, since the two are in series. The on time (t_{on}) is the maximum possible switch conduction time. It is equal to the time required for C_T to ramp up from its lower to upper threshold. The required value for C_T can be determined by using the minimum oscillator charging current and the typical value for the peak-to-peak oscillator voltage swing, both taken from the data sheet.

$$C_T = I_{chg(min)}(\Delta t/\Delta V)$$
$$C_T = 20 \times 10^{-6}(t_{on}/0.5)$$
$$C_T = 4.0 \times 10^{-5}(t_{on})$$

The off time is the time that diode D1 is in conduction and it is determined by the time required for the inductor current to return to zero. The off time is not related to the ramp-down time of CT. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$, and the minimum operation frequency is calculated as shown here:

$$f_{min} = 1/(t_{on(max)} + t_{off})$$

3.5 Inductance Calculation

The minimum value of inductance (L) can now be calculated. The V-known quantities are the voltage across the inductor and the required peak current for the selected switch conduction time:

$$L_{min} = ((V_{in} - V_{sat} - V_{out})/I_{pk(switch)})t_{on}$$

The minimum value of inductance is calculated assuming the onset of continuous conduction operation with a fixed input voltage, maximum output current, and a minimum charge-current oscillator.

The net charge per cycle delivered to output filter capacitor (C_{out}) must be zero (Q+ = Q–) if the output voltage is to remain constant.

3.6 Output Voltage Ripple

The ripple voltage can be calculated from the known values of on time, off time, peak inductor current, and output capacitor value:

During t_{on}

$$ic(t) = I_{pk}/t_{on} \times t, \text{ positive slope}$$
$$V(t) = 1/C_{out} \int I_{pk}/t_{on} \times t \, dt$$
$$= I_{pk}/(C_{out} \times t_{on}) \times t^2/2 + \text{constant}$$

The axis of the parabola pass was chosen by its minimum, so constant = 0.

$$= I_{pk}/(C_{out} \times t_{on}) \times t^2/2$$
$$V(t_{on}/2) = I_{pk}/(C_{out} \times t_{on}) \times (t_{on}/2)^2/2$$
$$= I_{pk}/C_{out} \times t_{on}/8$$

During t_{off}

$$ic(t) = -I_{pk}/t_{off} \times t, \text{ negative slope}$$
$$V(t) = -1/C_{out} \int I_{pk}/t_{off} \times t \, dt$$
$$= -I_{pk}/(C_{out} \times t_{off}) \times t^2/2 + \text{constant}$$

The axis of the parabola pass was chosen by its minimum, so constant = 0.

$$= -I_{pk}/(C_{out} \times t_{off}) \times t^2/2$$
$$V(t_{off}/2) = -I_{pk}/(C_{out} \times t_{off}) \times (t_{off}/2)^2/2$$
$$= -I_{pk}/C_{out} \times t_{off}/8$$
$$V_{ripple(C)} = |V(t_{on}/2)| + |V(t_{off}/2)|$$
$$= (I_{pk}/C_{out}) \times (t_{on}/8) + (I_{pk}/C_{out}) \times (t_{off}/8)$$

$$V_{ripple(C)} = (I_{pk}/C_{out}) \times (t_{on} + t_{off})/8$$
$$V_{ripple(ESR)} = I_{pk} \times ESR$$
$$V_{ripple(p\text{-}p)} = I_{pk}/C_{out} \times (t_{on} + t_{off}) + I_{pk} \times ESR$$
$$V_{ripple(p\text{-}p)} = I_{pk} \times [(1/8C) \times (t_{on} + t_{off}) + ESR]$$

Figure 7 shows a graphical derivation of the peak-to-peak ripple voltage that was obtained from the capacitor current and voltage waveforms.

The calculations shown above account for the ripple voltage contributed by the ripple current into an ideal capacitor.

In practice, the calculated value should be increased due to the internal equivalent series resistance (ESR) of the capacitor. The additional ripple voltage is equal to $I_{pk(ESR)}$. Increasing the value of the filter capacitor reduces the output ripple voltage. However, a point of diminishing return is reached, because the comparator requires a finite voltage difference across its inputs to control the latch. The voltage difference required to completely change the latch states is about 1.5 mV, and the minimum achievable ripple at the output is the feedback divider ratio multiplied by 1.5 mV:

$$V_{ripple(p\text{-}p)}(min) = (V_{out}/V_{ref})(1.5 \times 10^{-3})$$

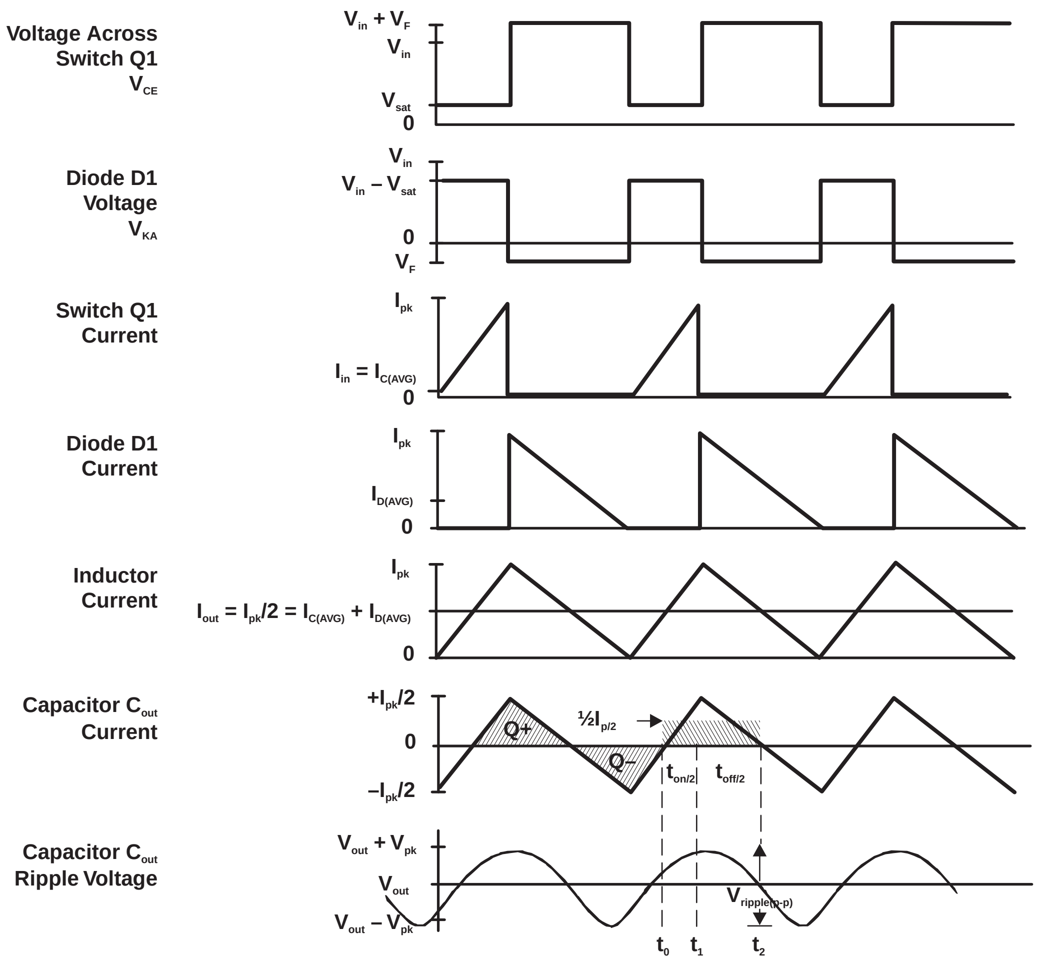


Figure 7. Buck Switching Regulator Waveforms

4 Boost Switching Regulator

Figure 8 shows a basic switching regulator. Energy is stored in the inductor during the time that transistor Q1 is in the ON state. When transistor Q1 is turned off, the energy is transferred in series with V_{in} to the output filter capacitor (C_{out}) and load (R_L). This configuration allows the output voltage to be set to any value greater than that of input. The following equations can be used to calculate the output voltage:

$V_{out} = V_{in}(t_{on}/t_{off}) + V_{in}$
or
$V_{out} = V_{in}((t_{on}/t_{off}) + 1)$

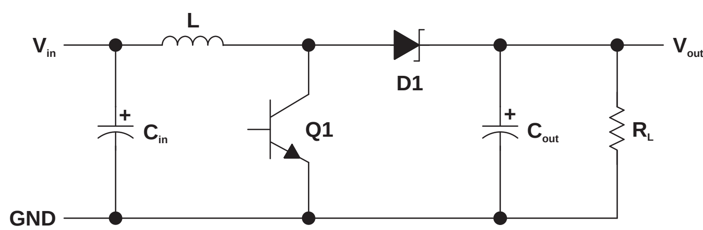


Figure 8. Boost Switching Regulator

4.1 Operation of MC34063 as Boost Converter

As an example, suppose that transistor Q1 is off, the inductor current is zero, and output voltage is at its nominal value. At this time, load current is being supplied only by C_{out}, and it will eventually fall below nominal value. When the output voltage falls below the nominal value, it is sensed by the control circuit, which initiates an on cycle, driving transistor Q1 into saturation. Current starts to flow from input through the inductor and Q1, and it rises at a rate of $\Delta I/\Delta t = V/L$. The voltage across the inductor is equal to $V_{in} – V_{sat}$, and the peak current is roughly a linear function of t, as shown here:

$I_L = ((V_{in} – V_{sat})/L)t$

When the on-time is completed, Q1 turns off, and the magnetic field in the inductor starts to collapse, generating a reverse voltage that forward biases D1, supplying energy to C_{out} and R_L. The inductor current decays at rate of $\Delta I/\Delta t = V/L$, and the voltage across it is equal to $V_{out} + V_F – V_{in}$. The current at any instant is calculated as shown here:

$I_L = I_{L(pk)} – ((V_{out} + V_F – V_{in})/L)t$

4.2 Time-On and Time-Off Calculation

Assuming that the system is operating in the discontinuous mode, the current through the inductor reaches zero after the t_{off} period is completed. Then the $I_{L(pk)}$ attained during t_{on} must decay to zero during t_{off}, and a ratio of t_{on} to t_{off} can be written as shown here:

$((V_{in} – V_{sat})/L)t_{on} = ((V_{out} + V_F – V_{in})/L)t_{off}$
$\therefore\ t_{on}/t_{off} = (V_{out} + V_F – V_{in})/(V_{in} – V_{sat})$

The volt-time product of t_{on} must be equal to that of t_{off}, and the inductance value does not affect this relationship.

The inductor current charges the output filter capacitor through D1 during t_{off}. If the output voltage is to remain constant, the net charge per cycle delivered to output filter capacitor must be zero (Q+ = Q–).

$I_{chg}t_{off} = I_{dischg}t_{on}$

4.3 Peak Current Calculation

Figure 9 shows the boost switching regulator waveforms. By observing the capacitor current and making some substitution in the previous equation, a formula for peak inductor current can be obtained.

$(I_{L(pk)}/2)t_{off} = I_{out}(t_{on} + t_{off})$
$\therefore\ I_{L(pk)} = 2I_{out}(t_{on}/t_{off} + 1)$

4.4 Inductance Calculation

The peak inductor current is also equal to the peak switch current, since the two are in series. By knowing the voltage across the inductor during t_{on} and the required peak current for the selected switch conduction time, a minimum inductance value can be determined:

$L_{min} = ((V_{in} – V_{sat})/I_{pk(switch)})t_{on(max)}$

4.5 Output Voltage Ripple

Calculate the output ripple voltage from the known values of t_{on}, t_{off}, peak inductor current, output current, and output capacitor value. The capacitor current waveforms is depicted in Figure 9, t1 being the discharging interval. Solving for t1 in known terms yields:

During t_{off}, the current is linear with negative slope, $–\Delta I_L/t_{off}$

$$ic(t) = –(I_{pk}/t_{off}) \times t$$

$$V(t) = –1/C_{out} \int (I_{pk}/t_{off}) \times t\,dt$$

$$= –I_{pk}/(C_{out} \times t_{off}) \times t^2/2 + \text{constant}$$

The axis of the parabol pass was chosen by the maximum so constant = 0.

$$= –I_{pk}/(C_{out} \times t_{off}) \times t^2/2$$

$$V(-\tau) = –I_{pk}/(C_{out} \times t_{off}) \times \tau^2/2, \; \tau \text{ is time from ic(t) = max to ic(t) = 0}$$

$$(t_{off} – \tau)/_{off} = I_{out}/I_{pk}, \text{ triangle geometry}$$

$$\tau = t_{off} \times (I_{pk} – I0)/I_{pk} \qquad (1)$$

$$V(-\tau) = –I_{pk}/2(C_{out} \times t_{off}) \times (t_{off})^2 \times (I_{pk} – I0)^2/\Delta I_L^2$$

$$V(-\tau) = –t_{off} \times (I_{pk} – I0)^2/(2C_{out} \times I_{pk}) \qquad (2)$$

Energy conservation in the output capacitor: Q+ = Q–

$$(I_{pk} – I0) \times \tau/2 = (t_{off} – \tau) \times I0/2 + I0 \times t_{on} \qquad (3)$$

Equation 1 and Equation 2 give:

$$t_{off} \times (I_{pk} – I0)^2/2\Delta IL = I0/2 \times t_{off} \times (1 – (\Delta I_L – I0)/\Delta I_L) + I0 \times t_{on}$$

$$= t_{off} \times I0^2/2\Delta I_L + I0 \times t_{on}$$

$$t_{off} \times ((I_{pk} – I0)^2 – I0^2)/2I_{pk} = I0 \times t_{on}$$

$$(I_{pk} – 2I0) \times t_{off}/2 = I0 \times t_{on}$$

The inductor ripple current:

$$I_{pk} = 2I_{out} \times (1 + t_{on}/t_{off}) \qquad (4)$$

From output capacitor ripple periodicity and continuity:

$V(–\tau) = V_{ripple(pp)}$

By substituting Equation 4 in Equation 3:

$V_{ripple}(C_{out}) = I_{out}(t_{off} + 2t_{on})^2/2C(t_{off} + t_{on})$

If $t_{on} = 6.5t_{off}$, then:

$V_{ripple}(ESR) = 2I_{out} \times (1 + t_{on}/t_{off}) \times ESR$

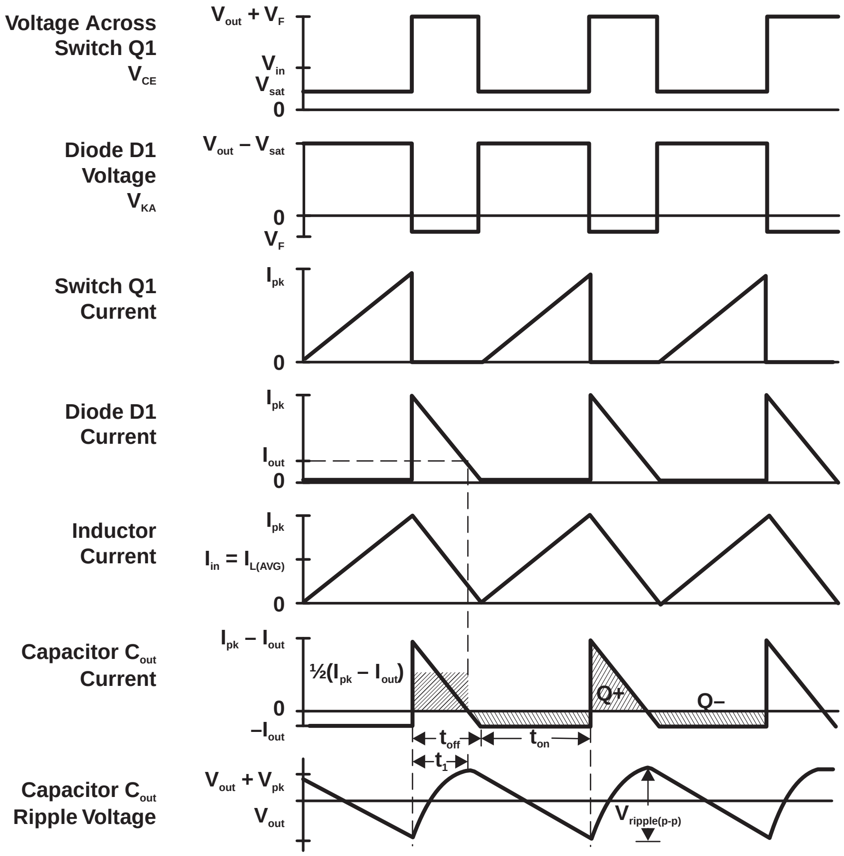


Figure 9. Boost Switching Regulator Waveforms

5 Inverting Switching Regulator

A basic voltage-inverting switching regulator is shown in Figure 10. The energy is stored in the inductor during the conduction time of Q1. Upon the Q1 turn off, the energy is transferred to the output filter capacitor and load. In this configuration, the output voltage is derived only from the inductor. This allows the magnitude of the output to be set to any value. It may be less than, equal to, or greater than that of the input and is set by the following:

$$V_{out} = V_{in}(t_{on}/t_{off})$$

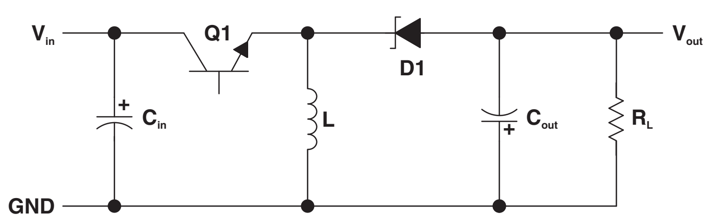


Figure 10. Switching Inverter Regulator

The inverter converter operates identically to that of the boost converter. The voltage across the inductor during t_{on} is $V_{in} - V_{sat}$ but, during t_{off}, the voltage is equal to the negative magnitude of $V_{out} + V_F$. The VLT time-product of t_{on} must be equal to that of t_{off}, a ratio of t_{on} to t_{off} can be determined:

$$(V_{in} - V_{sat})t_{on} = (|V_{out}| + V_F)t_{off}$$
$$\therefore\ t_{on}/t_{off} = (|V_{out}| + V_F)/(V_{in} - V_{sat})$$

The derivations and the formulas for $I_{pk(switch)}$, $L_{(min)}$, and C_{out} are the same as that of the boost converter. Figure 11 shows the voltage-inverter switching regulator waveforms.

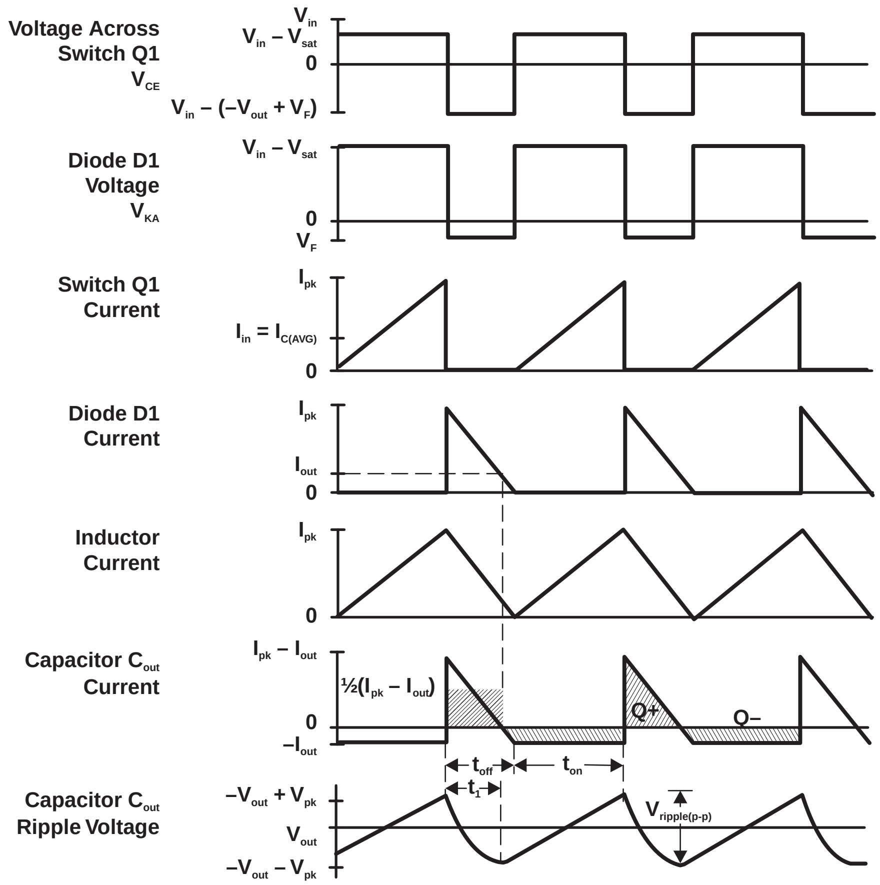


Figure 11. Inverter Switching Regulator Waveforms

6 Selecting the Right Inductor

Proper inductor selection is crucial to the performance of the switching regulator's design. The switching regulator has two mode of operation:

- Continuous mode
- Discontinuous mode

Each mode has characteristically different operating characters and, therefore, can affect the regulator performance and requirements. In many applications, the continuous mode is the preferred mode of operation, since it offers greater output power with lower peak currents, wider input range, and lower output ripple. These advantages of continuous-mode operation come at the expense of a larger inductor.

Once the minimum inductor and peak current value are determined, the inductor can be selected. Most manufacturers provide the following data in their data book:

- Inductance value
- DCR (dc resistance) of the winding
- DC saturation current
- RMS current
- Package type, size, and pattern

The geometry and the shape of the inductor chosen can have advantages and disadvantages. If high performance is a concern, then the toroid inductors are the best choices, as the magnetic flux is contained completely within the magnetic core, resulting in less EMI and noise. The EMI and noise can affect nearby sensitive circuits. In these situations, closed magnetic structures, such as toroid, pot core, or E-core, are more appropriate.

In cost-sensitive applications, the inexpensive bobbin core inductors can be used. However, the bobbin core inductors can generate more EMI, as the open core does not confine the flux within the core and can affect nearby sensitive circuits.

IMPORTANT NOTICE