

# High-Power PoE PD Using TPS2375/77-1

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## ABSTRACT

Some specialized applications require more power than the 12.95 W allowed by the IEEE802.3af standard. This application report discusses techniques for implementing nonstandard high-power systems with an emphasis on the powered device (PD). A specific design example of a 26-W, two-pair PD front end is presented along with test results. This type of solution bridges between the existing IEEE 802.3af and the forthcoming IEEE 802.3at, PoEPlus standard.

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## 1 Introduction

Some powered device (PD) applications require more power than the existing IEEE 802.3af standard can provide. The standard, referred to as Power over Ethernet (PoE), leaves a significant margin between the specified power and the amount of power that most cabling can safely deliver. The advantages of delivering power over the Ethernet cable may outweigh the simplicity of solutions like an ac mains adapter or a second power cable. All Ethernet cable-powered solutions should incorporate the benefits of PoE, including safety, fault tolerance, and protection of non-PoE devices. All solutions that deviate from the standard are, by definition, incompatible with the installed base of IEEE 802.3af-compliant devices and must be viewed as stand-alone systems.

This application report discusses a number of solutions that use as much of the existing IEEE 802.3af as possible, while delivering more power. In particular, a higher current, two-pair power solution is presented. It is important to keep in mind that, even though this application report focuses on the powered device (PD), an end-to-end system solution is required. Nonstandard solutions are normally used in special applications for relatively small numbers of devices in an installation.

This report assumes the reader has some basic knowledge of PoE. A complementary application report focusing on the power-sourcing equipment (PSE) is listed in the references.

## 2 Overview of Existing Power System and Limitations

The IEEE 802.3af standard embodies the following assumptions and characteristics:

### Assumptions:

- Power can be fed from an endpoint or the middle of a link.
- The source supply is relatively stiff within the required range of operation.
- The load has a switching power supply input
- IEC60950 must be met
- The system must work over the widest range of cabling including old telephone-style infrastructure
- The system must operate over a 100-m cable
- Powering is an independent overlay to the existing data specifications
- Management of multiple lines and power resources is not addressed

### Characteristics:

- Feeds power at 44 V to 57 V
- Operates over two pairs of 40- $\Omega$ , loop-resistance cable, yielding an effective 20- $\Omega$  power circuit
- Feeds over either of two wire-pair sets in the cable, but not both
- PD operates from either polarity
- Removes power from unplugged cable
- Does not apply more than a small probe voltage to non-PoE devices
- PSE protects against output short and overload

IEEE 802.3af specifies a minimum of 15.4 W (350 mA at 44 V) into the cable, delivering a maximum 12.95 W to the PD (350 mA at 37 V). The difference in voltage (7 V) and power (2.45 W) accounts for losses in the maximum length cable, which has a worst-case resistance of 20  $\Omega$ . The standard allows peak currents of 400 mA with a 350-mA average current.

## 3 Overview of Techniques

Increasing the delivered power requires modifying some of the limits built into the IEEE 802.3af standard. Possible approaches include raising the supply voltage, raising the supply current capacity, and reducing the cable resistance. These techniques may be used alone or in combination.

The simplest solution narrows the PSE output voltage range. The 57-V upper limit should not change to

maintain compatibility with existing equipment and to provide tolerance for overvoltage while remaining within the IEC 60950 limit of 60 V. The lower PSE output-voltage limit can be inferred by assuming a PSE input supply tolerance and an internal voltage drop. For example, a PSE tolerance might be 52 V to 57 V, consisting of a 55.5-V  $\pm 1.5$ -V supply and a control loss of 2 V. This PSE solution supplies 18.2 W minimum, with 15.75 W to the PD, while maintaining the IEEE 802.3af cabling and current.

More power can be delivered at a fixed load current by reducing the cabling resistance. The IEEE 802.3af specification assumes 40- $\Omega$  loops based on IEC 11801 Class-C infrastructure. However, structured cabling using CAT-5 or better cabling conforms to 25- $\Omega$ , Class-D loops. These limits are consistent with TIA/EIA 568-B. Class-D wiring results in a power-feed resistance of 12.5  $\Omega$ . Delivering power over all four pairs does reduce power loss at the same net current, but requires overhead and control for each pair. The high level of complexity associated with four pair solutions only makes sense when conductor heating and transformer limitations make two-pair power solutions impractical.

Combining the effects of the narrow voltage range and the CAT-5 cable delivers 16.67 W to the PD. The power gain was 0.92 W, indicating that the cabling resistance is not the dominant effect. Together, these two simple changes result in a 31% increase of available power.

One can also obtain more power by increasing the allowed operating current in the loop. This approach raises a number of issues, including:

1. The ability of cabling to carry the current
2. The ability of data transformers to handle higher offset current
3. The ability of the connectors to handle the electrical stress while plugging and unplugging
4. The ability of the cable to operate at elevated temperatures
5. The ability of jacks with integrated magnetics to sustain additional heating

A separate section discusses these issues.

As a practical example, assume that a Class-D cable can easily carry 300 mA per conductor, or a 600-mA loop current over two pairs at ambient temperatures of up to 55°C. Assuming a 52-V output, the PSE supplies 31.2 W, the PD receives 26.7 W, and the cable consumes 4.5 W. Distribution efficiency ( $P_{PD\_IN}/P_{PSE\_OUT}$ ) is actually slightly better than for the IEEE 802.3af case. Allowing for input circuit and conversion efficiency, the PD achieves in excess of 22 W of processed power.

## 4 Higher Current Considerations

Increasing the loop current raises complex issues. In some cases, existing IEEE, TIA/EIA, and ISO standards either do not address all the problems or need improvement.

The conductors and connector contacts can handle currents to 0.75 A each (Reference 3). However, cable heating in large bundles is a concern. Cables should not operate above their 60°C insulation rating for extended time. Higher temperatures may cause permanent transmission characteristic shift. The worst-case scenario involves a large bundle of cables running many meters, carrying the maximum current in every cable, in a uniformly hot environment, for extended time. The existing standards, including IEEE 802.3af, TIA/EIA568, and ISO 11801, provide no guidance in thermal derating. Cable temperature rise can be addressed with simple measures like additional ambient temperature derating, use of smaller bundles, or limiting the percentage of high current cables in a bundle.

Ethernet appliances that signal with 10/100 baseT can avoid data magnetics issues by simply powering through the unused pairs (RJ-45 pins 4-5 and 7-8). Solutions that cannot use this technique must address the limits of the magnetics.

The data transformer's current limitations are primarily due to loss of Ethernet signal quality when the transformer sees a dc current imbalance (Reference 6, Annex 33E). Current imbalances are caused by both data patterns and by PoE current differentials stemming from differences in resistance between the wire, magnetics, and contacts on each side of a pair. The wire and contact tolerances in various standards imply current imbalances in excess of existing transformer ratings, even for the currents of IEEE 802.3af. This situation makes it difficult to specify meaningful requirements for a higher-current implementation. A practical, although not rigorous approach, simply scales the required offset current withstand from the IEEE 802.3af specification of 10.5 mA with 350 mA of loop current. A larger set of data magnetics, or a center-tapped inductor, can be employed to carry the offset. Most data solutions include a common-mode choke which must also be considered.

The RJ-45 jack's contacts sustain high stress when connecting and disconnecting. The IEC 60603-1 specification uses a life test of 750 cycles with an allowed resistance shift of no more than 20 mΩ. Connection stress occurs when a PSE detecting at the open-circuit, 30-V limit instantaneously charges the PD input capacitance and cable capacitance. This problem is inherent in the standard and is not worsened by the increased current. The PD input diode bridges protect the contacts during disconnection from internal inductive currents. The contacts need only withstand the energy stored in the inductance of the cable itself. Early testing of contact wear found that a lumped 100 μH carrying 540 mA would damage the contacts beyond allowed limits over the life test (Reference 2). This model appears to have overestimated the cable inductance and also ignores the capacitance and transmission line effects. This issue is under study by the IEEE 802.3at committee.

Lastly, there is the issue of IEEE 802.3af classification. Because the proposed solutions are considered outside of the standard, the developer must provide an end-to-end solution. The proprietary nature of these solutions makes classification unnecessary, however the designer may choose to use the existing classification to distinguish between different high-power levels.

## 5 The Current Booster

Figure 1 shows a simple current booster that uses the Texas Instruments TPS2377-1 PD controller as a building block. This circuit is designed to provide 600 mA continuous with a minimum 650-mA current limit. The benefits of using this approach include the proven PoE interface, current limiting, foldback on a hard fault, thermal limiting, simplicity, and low cost. Although not the most efficient solution, it has shown itself to be robust to startup, thermal stress and load shorts.

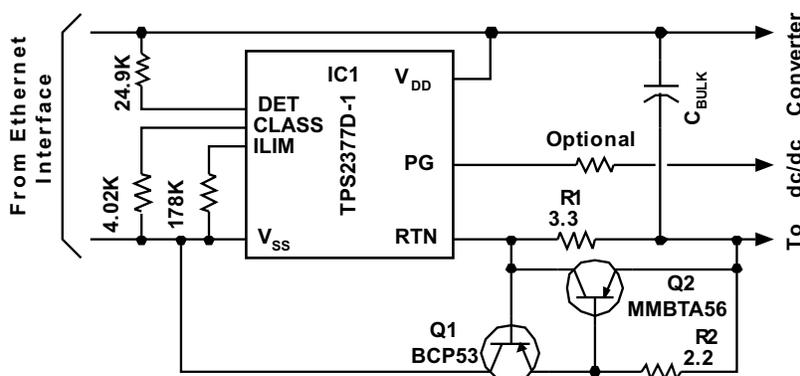


Figure 1. PD Hotswap With Current Booster

The circuit of Figure 1 illustrates a standard PD interface with the addition of a simple current booster circuit consisting of Q1, Q2, R1, and R2. The booster current flows through Q1, which adds to the current flowing through IC1, permitting greater load current than IC1 could support alone. Q1 is off when load current is less than about 200 mA due to the selection of R1. Q1 is off during PoE detection, PoE classification, and after the link is powered while  $C_{BULK}$  charges. As load current increases above 200 mA, it incrementally splits between IC1 and Q1 at approximately the ratio of  $R2/R1$ . The resistors are chosen to ensure that IC1 performs its current limit and foldback functions at the lowest practical current over the design load. Q2 serves to protect Q1 during transient load-short conditions. R1 never has more than two diode drops across it, and R2 only has one diode drop. Q1 only has a voltage corresponding to  $V_{RTN-VSS}$  plus a diode drop until IC1 goes into current limit, when it may have as much as 10 V across it before the TPS2377-1 folds back to the inrush limit or thermally cycles off.

The optional resistor connected to the TPS2377-1's PG pin may be required to protect the dc/dc converter because the PG voltage is below the dc/dc converter's ground when it is low.

When selecting the resistors, note that Q1 is near saturation because its  $V_{CE}$  is only its own  $V_{BE}$  plus IC1's  $V_{RTN-VSS}$  of about 0.28 V ( $0.7 \Omega \times 0.4 \text{ A}$ ). This means that the effective  $\beta$  is much lower than the small-signal values given in the data sheet.

Approximate values may be selected by use of the following equations.

$$R1 = \frac{V_{BE\_Q1}}{I_{RTN1}} \tag{1}$$

$$R2 = \frac{\left( I_{RTN2} - \left( \frac{I_{CQ1}}{\beta_{SAT}} \right) \right) \times R1 - V_{BE\_Q1\_SAT}}{\left( I_{TOT} - I_{RTN2} \right) \times \left[ \frac{\left( \beta_{SAT} + 1 \right)}{\beta_{SAT}} \right]} \tag{2}$$

$$R2 \leq \frac{V_{BE\_Q2}}{I_{LIM} - I_{RTN2}} \tag{3}$$

Where

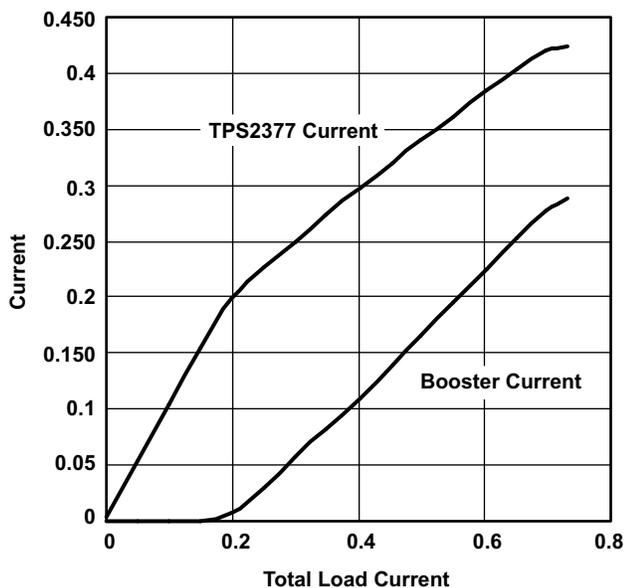
- $I_{RTN1}$  is the input current just before the booster just starts to carry current (0.2 A)
- $V_{BE\_Q1}$  is the transistor low-current turn-on threshold (0.6 V)
- $I_{RTN2}$  is the TPS2377-1 current at the design point (0.4 A)
- $I_{TOT}$  is the total design point current (0.65 A)
- $I_{CQ1}$  is just  $I_{TOT} - I_{RTN2}$
- $\beta_{SAT}$  is the anticipated Q1 gain to get a low voltage drop (0.25 A, 10)
- $V_{BE\_Q1\_SAT}$  is the transistor high-current drop (0.6 V)

These values result in R1 and R2 values of 3  $\Omega$ , for which a 3.3  $\Omega$  was used, and 2.32  $\Omega$  for which a 2.2  $\Omega$  was used. Check the R2 approximation of Equation 3 for the current limit. In this case,  $R2 \leq 2.35 \Omega$ , making the 2.2  $\Omega$  acceptable.

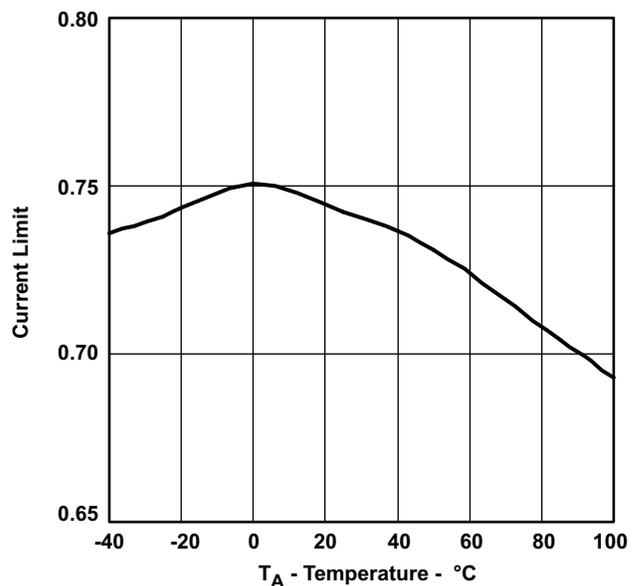
Although the target operational current was 600 mA, the design was calculated for 650 mA to allow for variations in Q1. Remember that the TPS2377-1 internal current limit may be as low as 405 mA.

## 6 Test Results

The measurements of Figure 2 show how the current divides between the TPS2377-1 and the BCP53 booster transistor. The measurements assume that IC1's current equals R1's, and Q1's current equals R2's. The effect of Q1's base current was ignored.



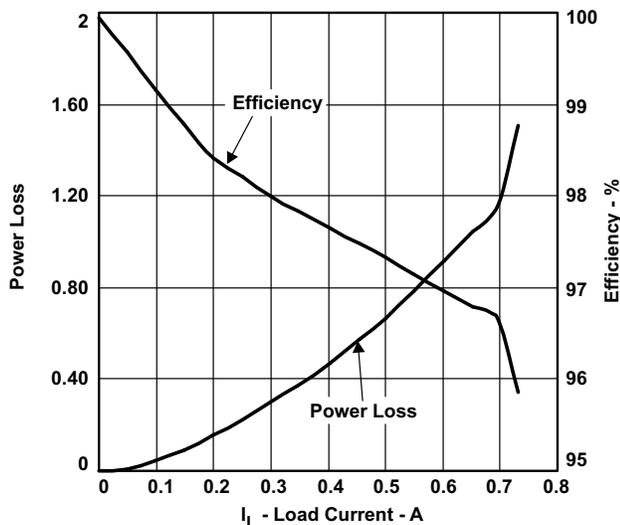
**Figure 2. Current Split Between TPS2377 and the Booster**



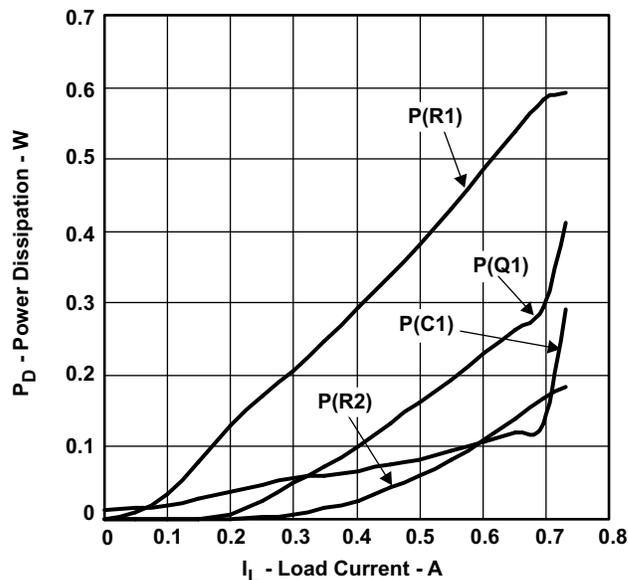
**Figure 3. Current Limit Versus Board Temperature**

Figure 3 shows the onset of current limit over temperature. A constant-temperature air stream was used to provide a uniform and repeatable environment. The IEEE 802.3af PD relies on the PSE for accurate long-term current limit. The PD only needs to protect itself against overloads and shorts. The variation in current limit depicted in Figure 3 is of little concern as long as it remains above the desired operational current. The TPS2377-1 internal current limit and over-temperature shutdown provide protection against overloads and high ambient temperatures.

Figure 4 shows the power loss and efficiency of this circuit as a function of load current. The last data point shows the effect of having just entered current limit. Figure 5 shows how the power divides amongst the various elements.



**Figure 4. Power Loss and Efficiency Versus Load Current**



**Figure 5. Component Power Dissipation Versus Load Current**

This data was obtained with a TPS2377-1 that exhibited a 450-mA current limit. The data-sheet tolerance for current limit indicates that this booster could limit current as low as 655 mA over temperature, neglecting any manufacturing variation in transistor  $\beta$  and  $V_{BE}$ .

## 7 Thermal Considerations

Table 1 lists component power dissipations at full load current. The printed-circuit board design should locate these parts on large areas of copper to dissipate the heat. In particular, Q1's tab should mount to a large, solid copper area that includes IC1 with good thermal coupling. Q2 should be well-coupled thermally to Q1 to receive the benefits of the temperature compensation. The largest power dissipater is R1. Fortunately, R1 connects to the local ground for the dc/dc converter which should be a relatively large copper fill. One of the benefits of the using the TPS2377-1 is that its thermal shutdown provides a level of protection against overheating for the entire circuit. When the TPS2377-1 overheats, it turns off, and once it cools about 20°C, it re-enables in the inrush state. This ensures that the PD must go through a complete restart cycle before Q1 carries current again.

**Table 1. Component Power Loss**

DEVICE	POWER LOSS	PACKAGE
Q1	0.231	SOT-223
Q2	–	SOT-23



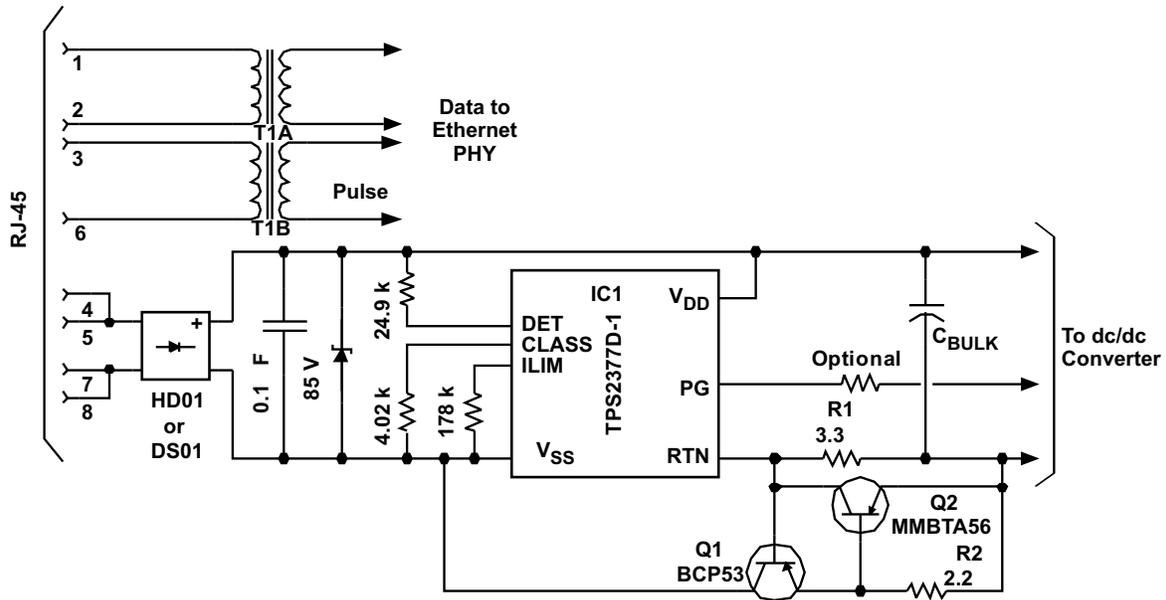


Figure 7. Feed from Spare Pairs, Polarity Insensitive

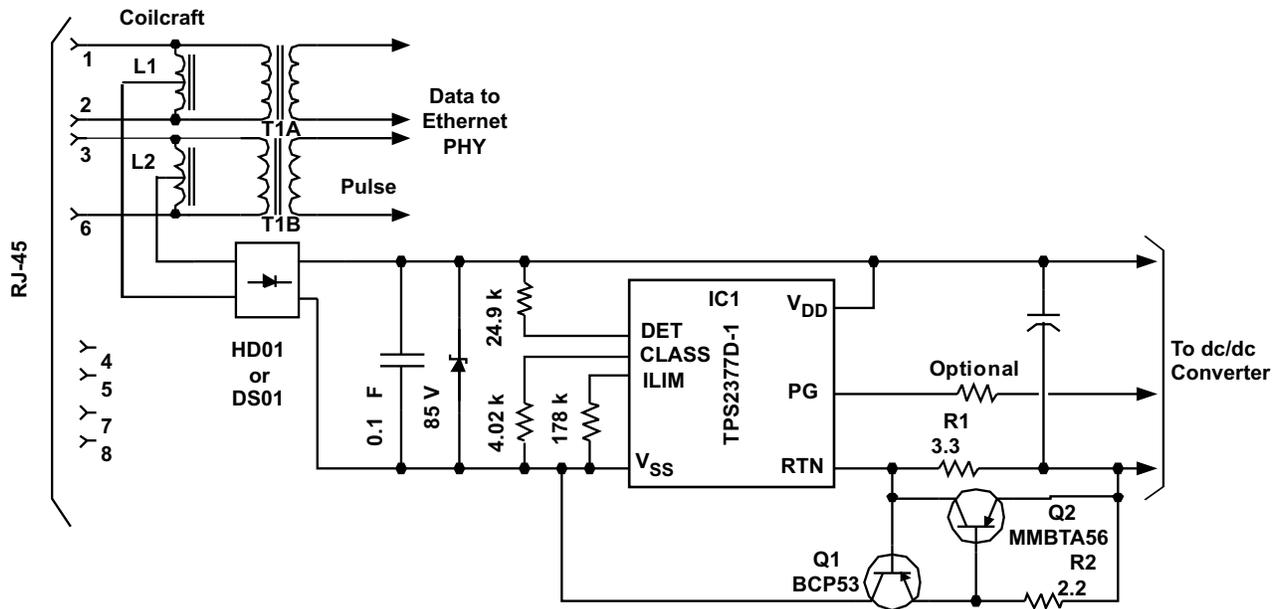


Figure 8. Feed from Data Pairs, Polarity Insensitive

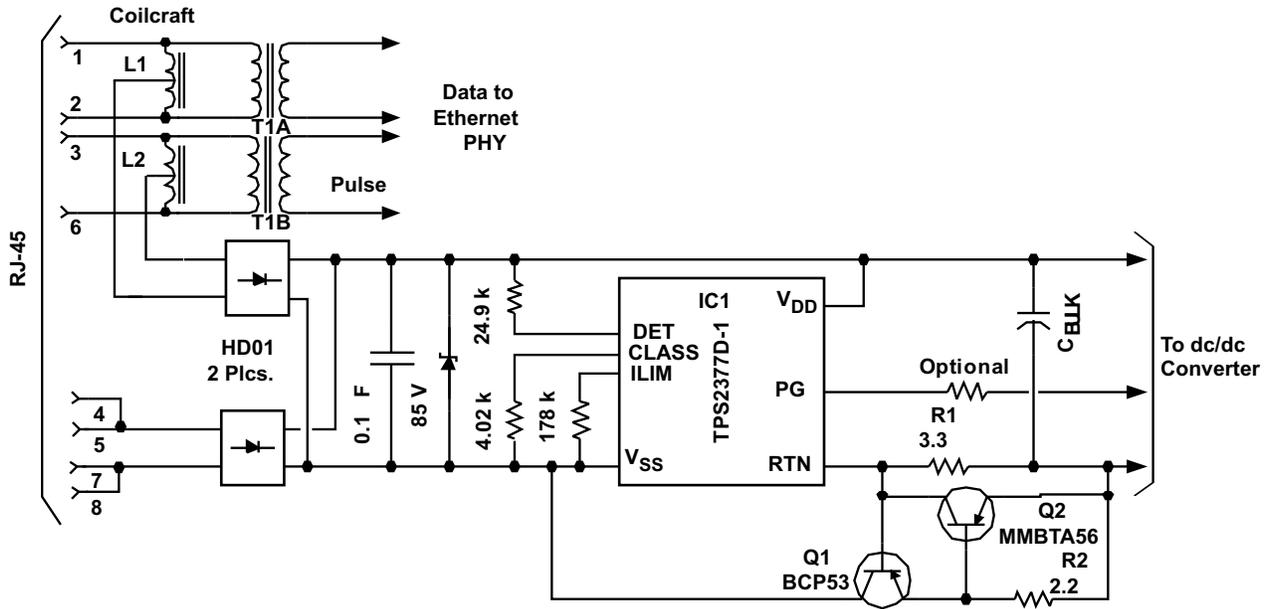


Figure 9. - Feed from Either Pair, Polarity Insensitive

## 9 System Level Performance

An end-to-end system was assembled to validate the calculations and performance, as shown in [Figure 10](#). The PSE was modified for higher current and a 55-V source supply was used. A power rheostat set to  $12.4 \Omega$  was used to simulate the cable and connectors, and the booster circuit of [Figure 9](#) was operated from it. An active load on the booster output was used to draw current through the system. Measurements were taken confirming voltage and power levels. [Figure 10](#) defines where each power measurement was performed. [Figure 11](#) shows measured power at various points in the system. These measurements are in line with those predicted earlier, with 27.8 W into the PD and 25.6 W available to be processed by the dc/dc converter. The PSE voltage drop was 1.2 V at the 600-mA load.

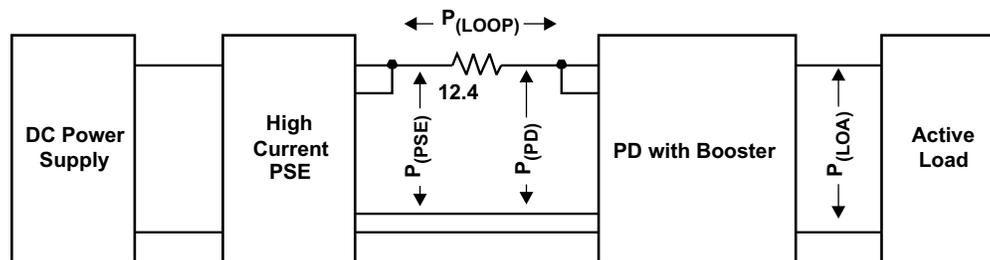


Figure 10. Definition of Power Measurement Points

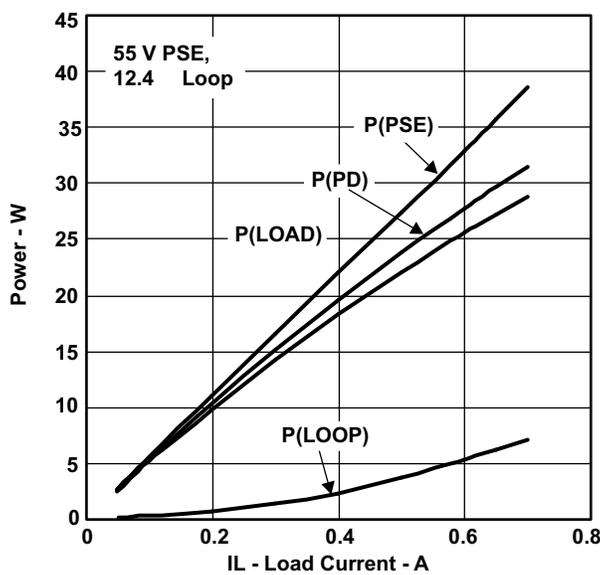


Figure 11. System Level Performance

## 10 Conclusions

A 26-W input PD can be powered over two pairs with a high-power PoE system implementation. The approach presented in this application report requires only a few low-cost modifications to existing PD front-end circuits.

## 11 References

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6. *IEEE Std 802.3af-2003*, IEEE

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