TPS6102x Boost Converter Down Conversion Mode

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ABSTRACT

The TPS61020 is a highly integrated, low-power, boost converter ideally suited for portable battery-powered equipment. The integrated down conversion mode allows the boost converter to operate with the input voltage greater than the output voltage, which is normally only possible with more complicated converters.

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1 Introduction

Boost converters use a single inductor to raise the output voltage above input voltage. However, if the input voltage range is both greater and less than the desired output voltage, a more complicated converter is required. SEPIC (single-ended primary inductor converter) or buck-boost converters use a second inductor to allow operation in both conditions. The TPS61020 boost converter makes use of a unique circuit that allows it to behave both as a step-up boost converter and step-down buck converter, while using only one inductor (see Figure 1). This operation is called down conversion mode.

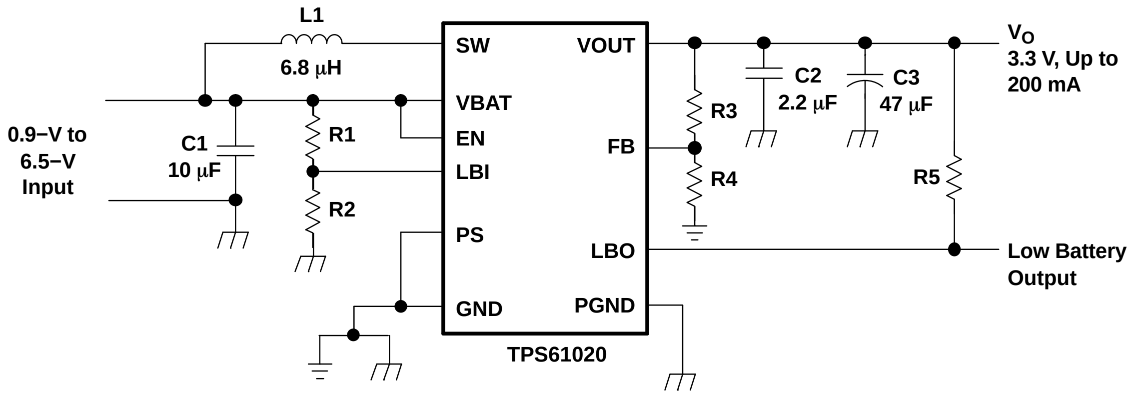

Figure 1. TPS61020 Typical Application

In portable battery-powered electronics, the battery voltage is determined by cell chemistry, discreet voltage steps per cell, and discharge conditions. Often the cell voltage and input voltage are greater than output voltage for only a small portion of the battery discharge, creating a requirement for buck-boost or SEPIC converter.

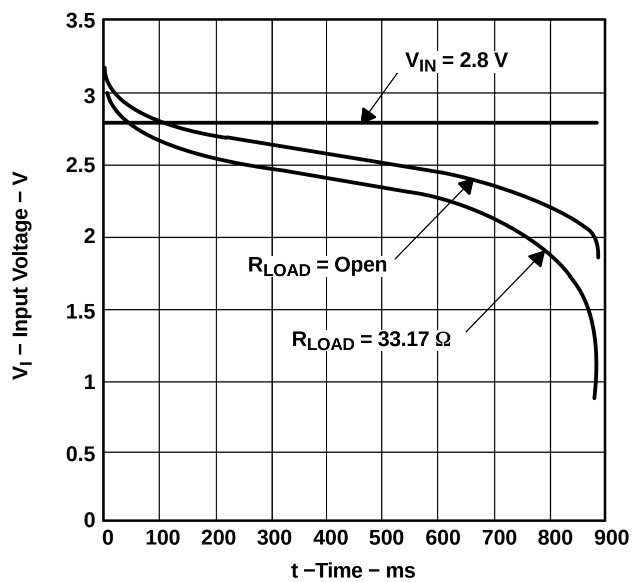

Figure 2. Dual-Cell Alkaline Discharge

If an application powered by two alkaline cells requires a 2.8-V output voltage, a typical boost converter would not be applicable for the first 20% of the discharge curve (see Figure 2). The output voltage of a typical boost converter equals the input voltage when the input is greater than the desired output voltage. A SEPIC or buck-boost converter is typically required to keep the output in regulation with these circuit parameters.

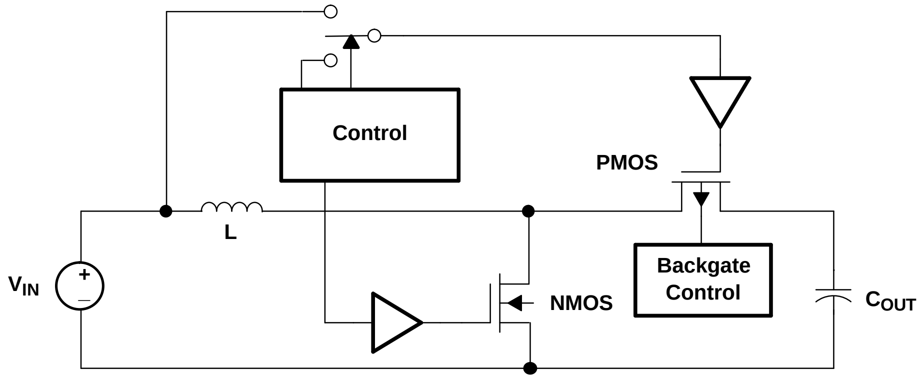

Figure 3. Boost Converter With Down Converter Block Diagram

2 Down Conversion Mode

Down conversion mode is a combination of a boost converter and LDO regulator. When input voltage exceeds output voltage, the converter enters the down conversion mode. The synchronous rectification PMOS is reconfigured to act as a pass transistor similar to an LDO (see Figure 3). The boost converter continues to switch and increase input voltage.

The PMOS gate is connected to Vin which prevents the device from turning on when the NMOS transistor is on. In this configuration, the gate voltage is fixed at Vin and the source voltage is adjusted to control conduction of the PMOS transistor by the boost converter.

The boost portion of the converter formed by the inductor and NMOS transistor continues to operate in the boost mode, increasing voltage at the PMOS transistor source (see Figure 4). Voltage gate to source is increased only enough to place the PMOS transistor into a linear region to act as a pass transistor. This threshold voltage, Vt, is about 1 V and increases as a function of output current, approximately 1 mV per 1 mA. In this configuration, the boost converter acts as a control element increasing inductor voltage, which in turn sets conduction of the PMOS transistor.

During NMOS transistor on-time (time D), the PMOS transistor is off and load current is supplied by the output capacitor, the same as occurs in boost mode. When NMOS transistor is off (time 1-D), inductor voltage increases the PMOS transistor gate-to-source voltage to Vt, and it begins to conduct. Voltage drop across the PMOS transistor during this time is Vin plus Vt.

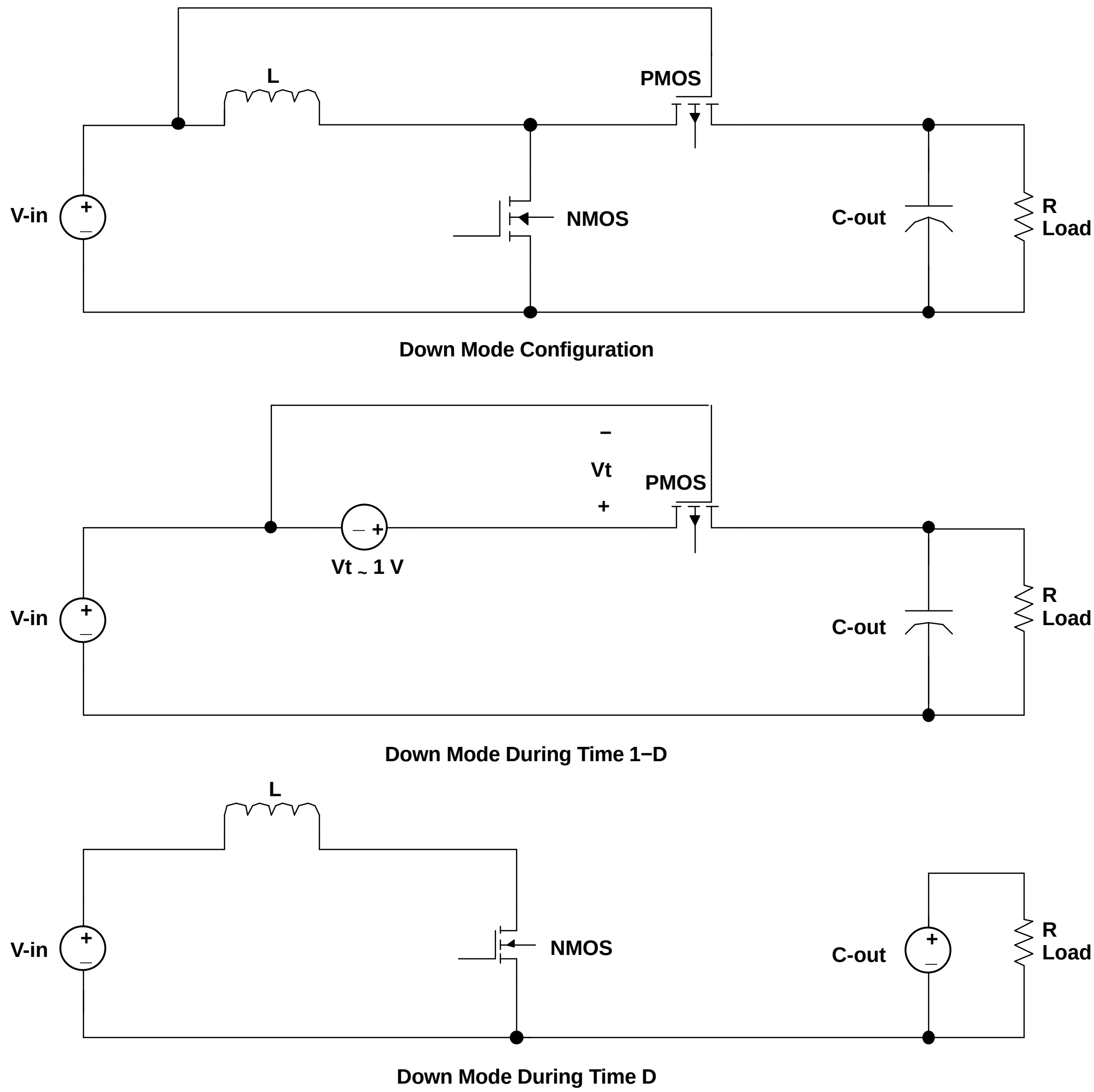

Figure 4. Simplified Down Mode Block

3 Power Dissipation

During a traditional boost mode, the converter is efficient with minimum loss in the NMOS and PMOS transistors (see Figure 5). During a down mode, the NMOS continues to switch with minimum loss but the PMOS is converted to a pass transistor with significant power dissipation (see Figure 6). Power dissipation during a down mode is dominated by loss in the PMOS transistor; therefore, loss from other sources are not included in this discussion.

Power dissipation of the PMOS transistor.

$$Pd = (Vin + Vt - Vout) \times Ipmos \times (1 - D)$$

Given that

$$Ipmos \times (1 - D) = Iout$$

This can be simplified to

$$Pd = (Vin + Vt - Vout) \times Iout$$

This results in higher power dissipation than the traditional LDO which is:

$$Pd = (Vin - Vout) \times Iout$$

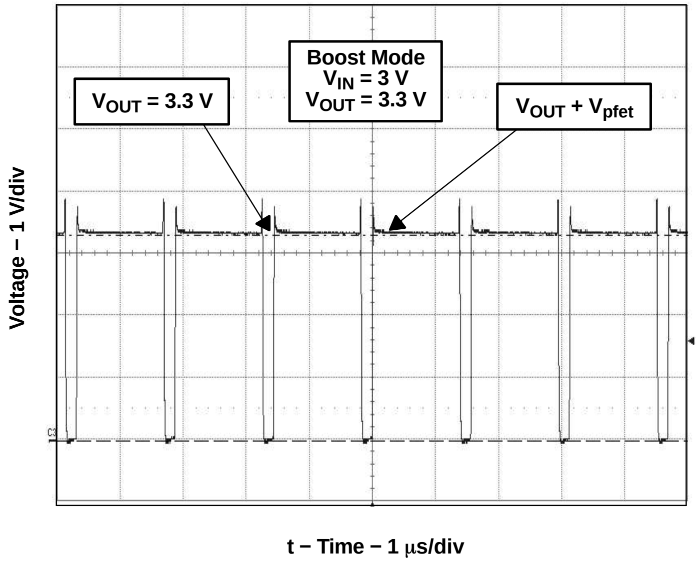

Figure 5. Switch Mode Waveform During Boost Mode

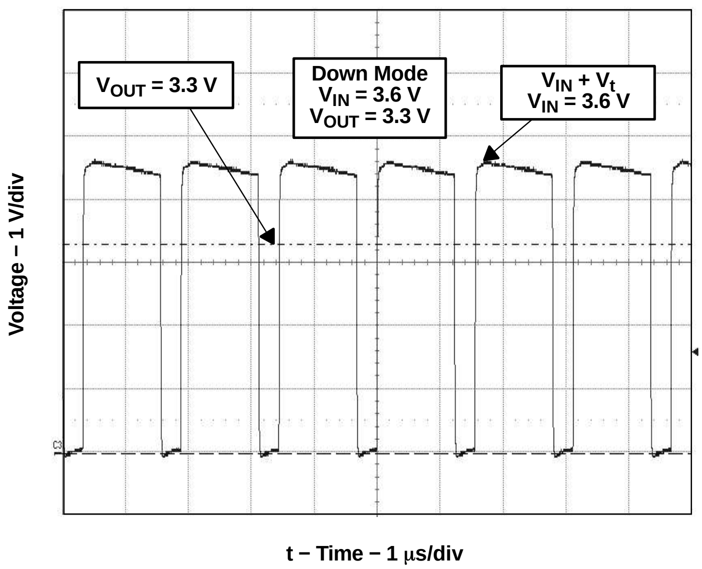

Figure 6. Switch Mode Waveform During Down Mode

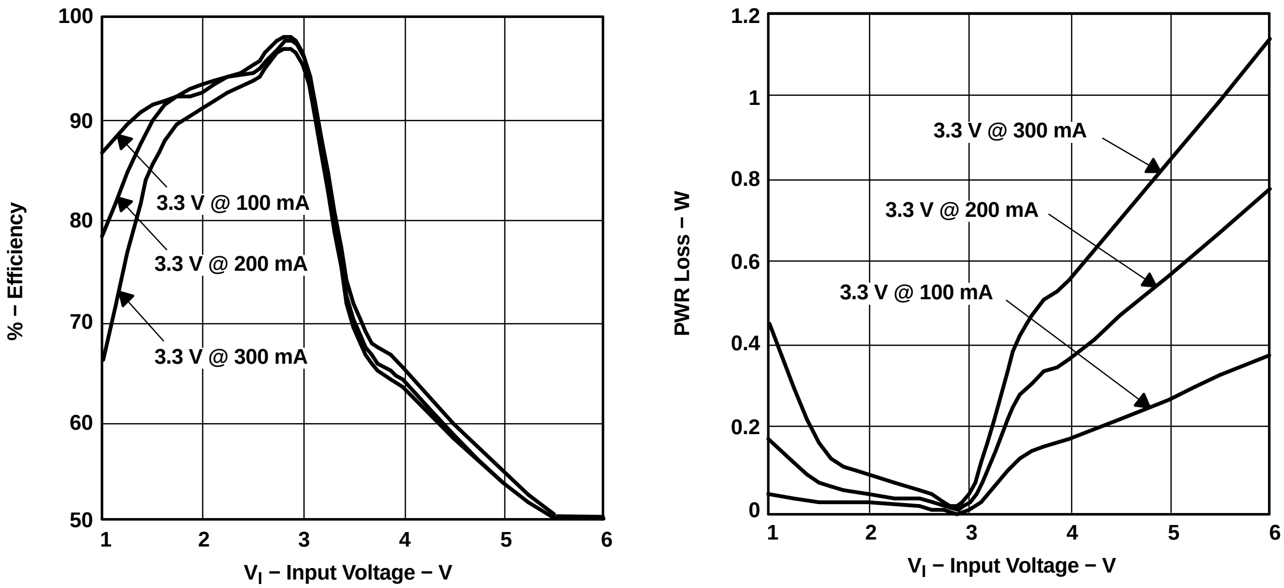

Figure 7. TPS61025 Efficiency and Power Dissipation vs Input Voltage

Figure 7 shows the onset of down mode. It is a less efficient mode of operation, resulting in a drop of 15% in efficiency. Losses increase with input voltage.

4 Power-Handling Capacity

The TPS61020 is supplied in a QFN PowerPAD™ 3 × 3 package. The maximum recommended junction temperature (T_J) is 125°C. With the PowerPAD soldered to a substantial thermal plane, the thermal resistance is 48.7°C/W. The power dissipation of the device is limited to approximately 2 W at 25°C and 850 mW at 85°C.

$$P_{d(max)} = \frac{\left(T_{J(max)} - T_A\right)}{R_{\theta JA}} \tag{1}$$

5 Conclusion

The TPS61020 boost converter with down mode is a low-cost alternative to a SEPIC or buck-boost converter in battery-powered applications where the input voltage is greater than the desired output voltage for a small portion of the battery discharge curve. However, until the input voltage drops below the desired output voltage, the efficiency of the converter is low. Power dissipation on the device during this time could be significant.

6 References

1. *A Step-Down Conversion Concept for A PWM-Mode Boost Converter*, C.V. Schimpfle and J. Kirchner
2. *TPS6102x 96% Efficient Synchronous Boost Converter With 1.5-A Switch* data sheet (SLVS451)
3. *TPS61020EVM High-Efficiency Synchronous Boost Converters User's Guide* (SLVU100)

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