Monotonic, Inrush Current Limited Start-Up for Linear Regulators

Jeff Falin *PMP Portable Products*

ABSTRACT

The output voltage of a linear regulator tends to rise quickly after it is enabled. This often results in a nonmonotonic rise of the output voltage (i.e., the output voltage overshoots, then dips), which can preclude proper operation of the load circuitry. This application report addresses methods to achieve a monotonic, inrush current limited start-up.

The simplified block diagram of Figure 1 depicts basic functional blocks of a linear regulator, consisting of a reference, error amplifier, and pass element. Note that undervoltage lockout (UVLO) is not implemented in all linear regulators.

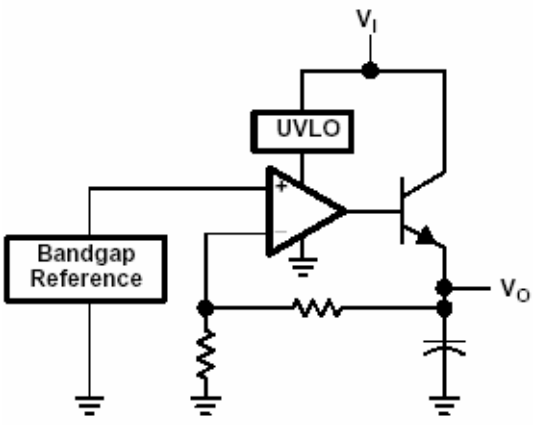

Figure 1. Simplified Block Diagram of a Linear Regulator

At start-up, the error amplifier senses that the output voltage is low and drives the pass element as hard as possible. After a short delay, the pass element pulls a large inrush current to charge the output capacitance and/or load abruptly. The delay is caused by three factors: the time required for the input voltage to rise above the UVLO circuitry, if any; the time required for the chip's internal circuitry, particularly the band-gap reference, to power up; and the time required for the regulator to sense its output voltage and turn on the pass element (i.e., the feedback loop bandwidth). The size of the regulator's output capacitance and the load resistance influences the start-up response. If the regulator starts up into a large capacitive or small resistive load, the inrush current is large, approaching the regulator's current limit in some cases. This application report discusses two methods of slew rate limiting a linear regulator's output voltage rise time and, consequently, limiting its inrush current at start-up, referred to as "soft starting" the regulator. The TPS796xx, high PSRR, low-noise family of regulators, which are designed for approximately 50-µs start-up times and thus large start-up currents, are used as examples.

Figures 2 and 3 show the simplest soft-start method in which a FET follows the regulator's output. The R_T and C_T determine the ramp time, and C_{GD} provides a smooth, linear ramp of the output voltage. A PMOS FET can be used when trying to soft start voltages that are greater than approximately 1.5 V, given current PMOS FET technology. An NMOS FET can be used when trying to soft start any voltage, provided there is a control voltage that is about 1 V larger than the voltage to be soft started, given current NMOS FET technology. Figure 3 also shows how to provide the control voltage using the TPS3803-01 supply voltage supervisor (SVS) with open-drain output.

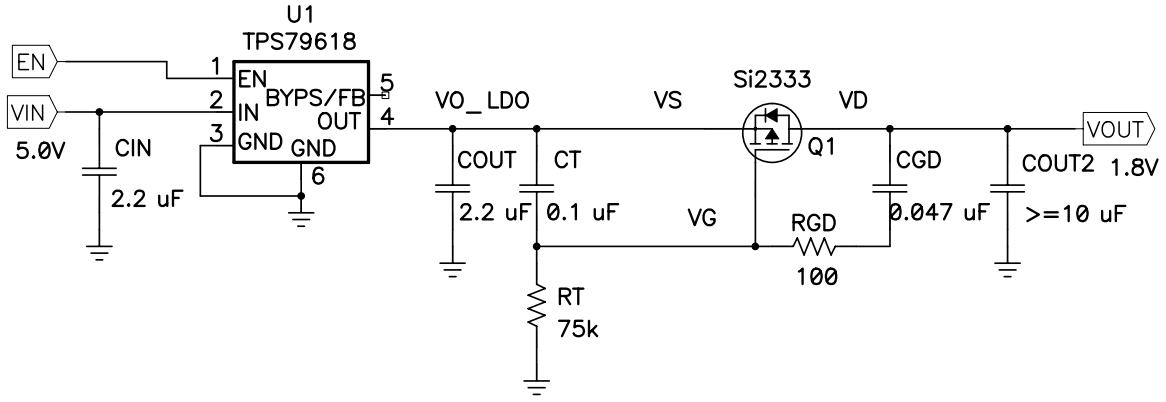

Figure 2. Soft Start Using a PMOS FET Following the Output

Note that the soft-starting FET must be placed after the regulator's minimum required output capacitance (C_{OUT}) in order to ensure that the regulator remains stable after being enabled. Also, there must be some capacitance, C_{OUT2}, after the switch that is at least an order of magnitude larger than C_T and C_{GD}. Careful component selection is critical for proper operation of the circuit. First, the PMOS FET must have a nominal threshold voltage (V_{TH}) that is less than the desired output voltage (i.e., $V_{OUT} > V_{TH}$) and the NMOS FET must have a threshold voltage that is less than the control voltage (V_{CNTRL}) minus the output voltage ($V_{CNTRL} – V_{O\ (LDO)} > V_{TH}$). Also, either FET's $R_{DS(on)}$ must be small enough so that the drop across it due to the maximum DC load current does not significantly reduce the regulated output voltage. C_{GD} is selected to be much larger the FET's inherent gate to drain capacitance ($C_{GD} > C_{rss}$). For the NMOS FET, the C_{GD} is split, with half going to $V_{O\ (LDO)}$ and the other half to ground. C_{GD2} to ground prevents the gate of the FET from charging up when $V_{O\ (LDO)}$ turns on abruptly. C_T is selected to be much larger than the gate to drain capacitance (i.e., $C_T >> C_{GD}$). R_{GD} is used primarily to prevent a capacitive path from V_{O_LDO} to V_{OUT} and should be between 10 Ω and 100 Ω. R_{T_PMOS} and R_{T_NMOS} are chosen using the following equations:

$$R_{T\_PMOS} \approx \frac{(V_{O(LDO)} - V_{TH}) * t_{SS}}{C_{GD} * V_{O(LDO)}} \quad (1)$$

$$R_{T\_NMOS} \approx \frac{(V_{CNTRL} - V_{O(LDO)} - V_{TH}) * t_{SS}}{C_{GD} * V_{O(LDO)}} \quad (2)$$

Where t_{SS} is the desired soft-start time, here 10 ms. These equations are derived in the appendix.

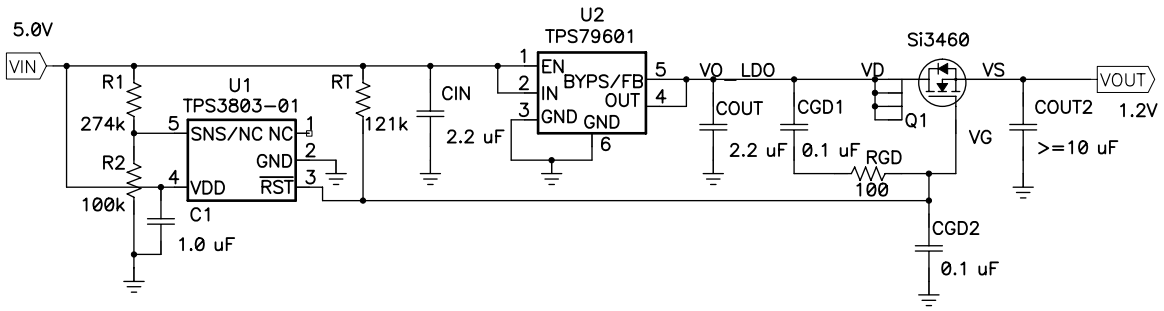

Figure 3. Soft-Start Using an NMOS FET Following the Output Being Driven by TPS3803-01 SVS

Figures 4 and 5 show the rise times of the regulator output voltage with and without the soft-start circuitry for V_{IN} = 5.0 V and I_{OUT} = 300 mA. The measured rise time is 12 ms, slightly more than the desired 10 ms, but within an acceptable margin considering the variation in Q1's threshold voltage, V_{TH}. The delay between EN going high and V_{OUT} ramping up is calculated in the appendix as t_{DELAY}. With such a long start-up delay, the variation of threshold voltage of Q1, and thus the exact time at which the switch turns on, can be neglected.

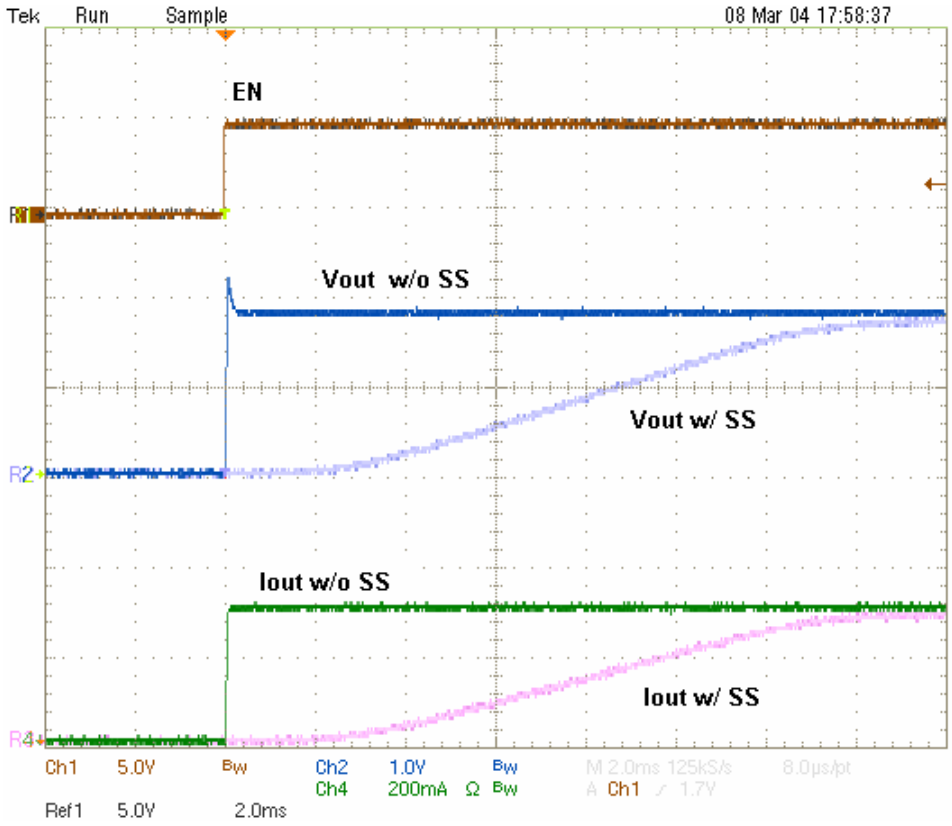

Figure 4. Results From PMOS FET Soft-Start Circuit Following the Output

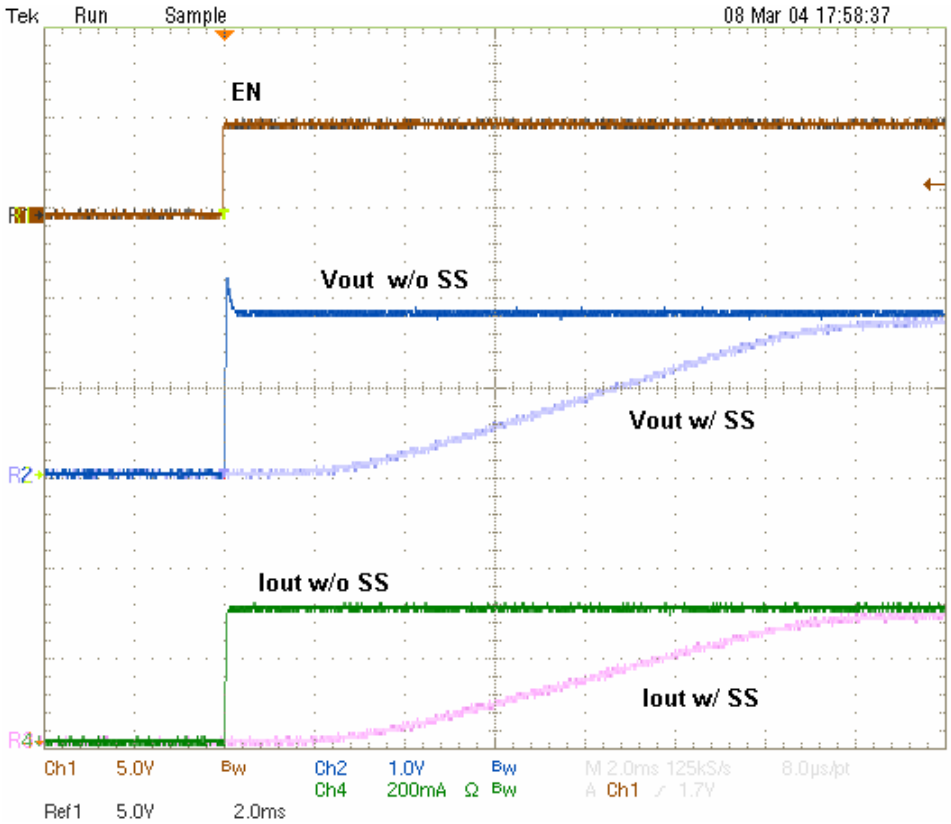

Figure 5. Results From NMOS FET Soft-Start Circuit Following the Output and TP3803-01 SVS for V_{CNTRL}

One disadvantage to this method of soft starting is the difficulty in finding FETs with low enough $R_{DS\ (on)}$ not to affect regulation under large load currents, or low enough threshold voltages for low output voltages. The Si2333 PMOS FET's $R_{DS(on)}$ is approximately 59 mΩ at V_{GS} = - 1.8 V; so, at 300-mA output current, the output voltage could be 18 mV below the nominal voltage, thus increasing the lower tolerance limit of the regulator solution from -3% to -4%. The Si3460 NMOS FET's $R_{DS(on)}$ is less than 30 mΩ at VGS = 5.0 V – 1.2 V = 3.8 V; so, at 300-mA output current, the output voltage could be 9 mV below the nominal voltage, thus increasing the lower tolerance limit of the regulator solution from -3% to -3.75%.

The second method, shown in Figure 6, forces a voltage on the feedback pin of the regulator, thereby artificially changing the start-up waveform.

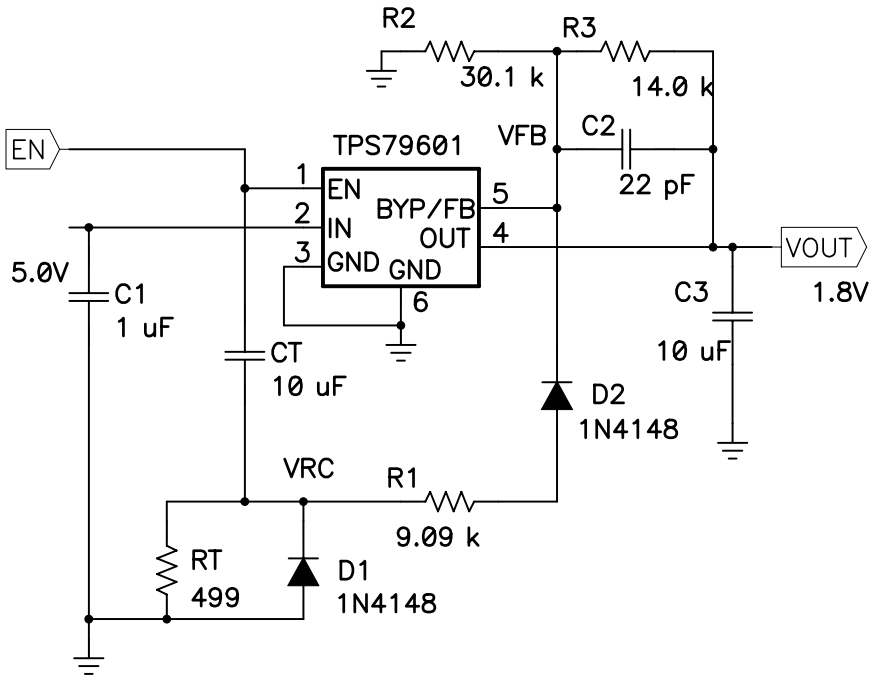

Figure 6. Soft-Start Circuit Using RC and Diode

When the enable signal goes high, node V_{RC} charges to V_{EN}. With proper sizing of R_1, the feedback node, $V_{FB,}$ artificially rises above the regulated intended feedback voltage of 1.2 V to V_{FB2}. V_{FB2} is chosen to be at least 200 mV above the intended feedback voltage but less than a diode drop below V_{EN}. Capacitor C_T then discharges through R_T and, as the feedback voltage drops, the pass element slowly turns on and the output voltage slowly rises. Diode D_2 keeps R_1, R_T, and C_T out of the feedback voltage divider and therefore prevents any degradation in output voltage tolerance or load transient response after start-up. Diode D_1 clamps node V_{RC} to a diode drop below ground when EN is taken low and is optional.

The following equation determines the appropriate size of R_1 to raise node V_{FB} to V_{FB2}.

$$R1 = \frac{V_{IN\,min} - 0.6V - V_{FB2}}{\frac{V_{FB2}}{R2 \| R3}} \tag{3}$$

In this example, V_{FB2} is 1.2 V + 0.2 V = 1.4 V and V_{INmin} is 3.3 V; so, the calculated value of R_1 is 9 kΩ. Once R_1 is determined, R_T is selected to be much smaller than R_1 (roughly a factor of 10 or more, so that it dominates the RC time constant), and then C_T can be sized to provide the appropriate rise time. In this example, in order to get a rise time of 5 ms with R_T = 499 Ω, C_T = 10 µF is required.

Figure 7 shows the rise time of the regulator with and without the additional circuitry for V_{IN} = 3.3 V and I_{OUT} = 300 mA. The measured rise time is slightly below 4 ms.

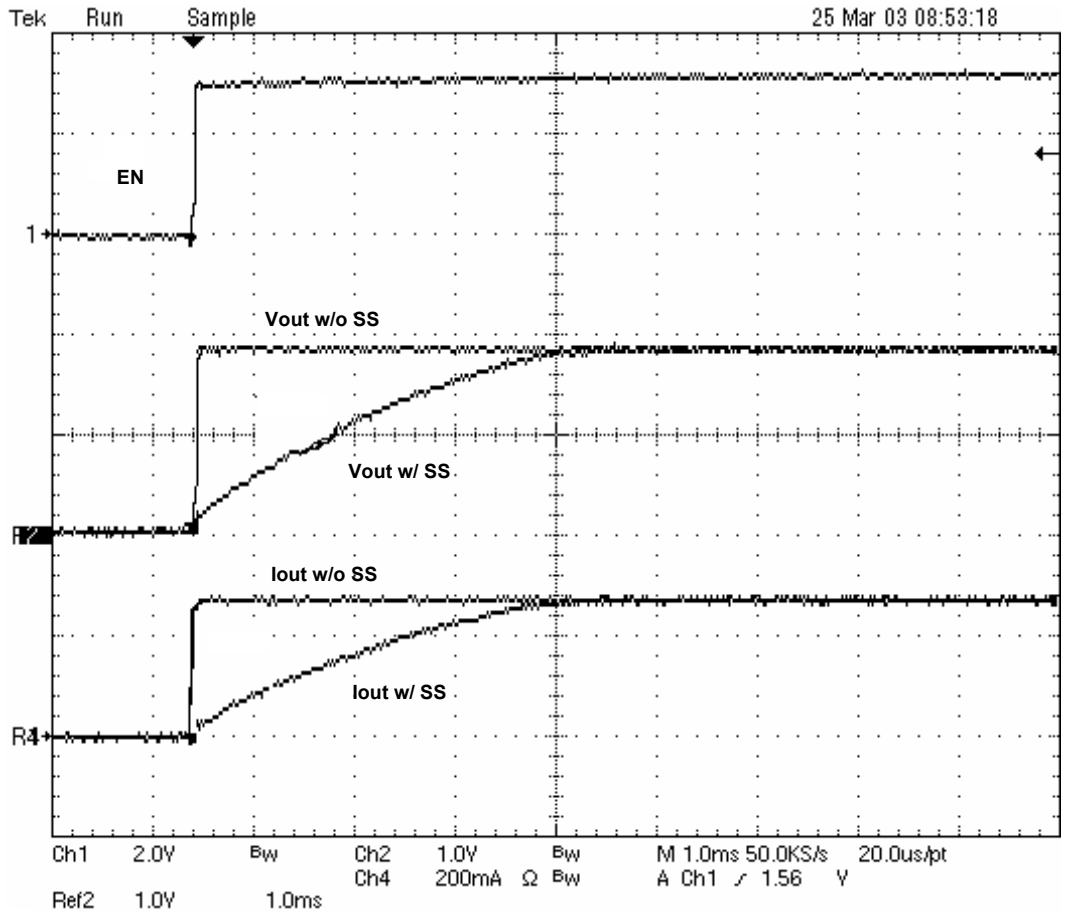

Figure 7. Rise Time of Regulator With and Without the Additional Circuitry for V_{IN} = 3.3 V and I_{OUT} = 300 mA

The advantages of this method are simplicity, cost, and isolation from the regulator after start-up due to diode D2 and due to the control voltage not being a function of the output voltage. The primary disadvantages are that this circuit requires the use of an adjustable regulator, and it does not work with some regulators (see below). Some regulators have extra features, like an integrated SVS or a fast transient assist circuitry, that require the output of the regulator be biased above ground after it is enabled. So, using this soft-start method, the start-up waveform could have an initial jump up to 1.5 V prior to the slow rise to the output voltage.

Either method limits the inrush current and, thus, slows the ramp time of the output of the linear regulator. The first method, which could theoretically be used with any dc/dc converter, is best suited for higher voltage rails with looser output voltage tolerances and fewer transients. The second method provides the best performance because the additional circuitry is effectively removed after start-up and thus affects neither load regulation nor transient response. The second method may also be effective in increasing the soft-start time of a switcher with fixed soft start. However, the second method may not work with all dc/dc converters, especially those with NMOS instead of PMOS differential pair in the error amplifier, those with integrated, digitally controlled soft-start, or those with extra circuitry, such as fast transient circuitry or integrated SVS, which is powered from the output voltage.

Appendix A. PMOS FET and NMOS FET Switching Characteristics

The PMOS FET switching characteristics are show in Figure A-1.

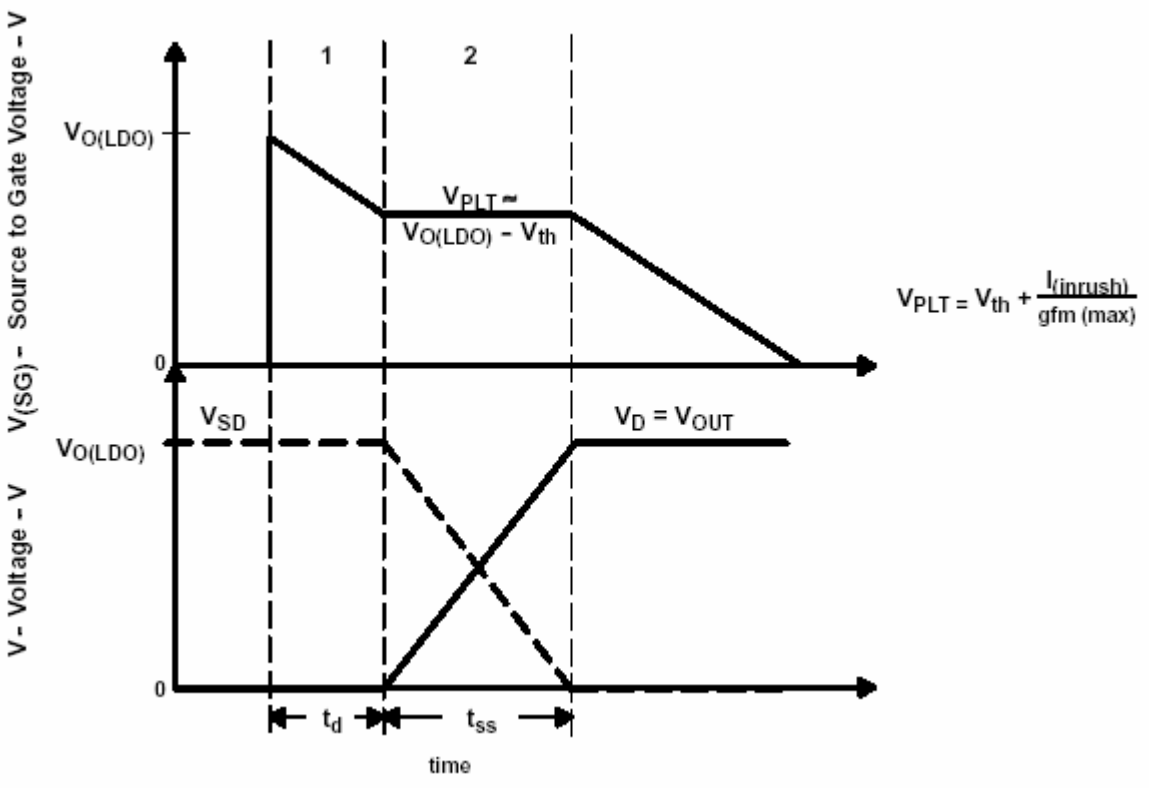

Figure A-1. PMOS Switching Characteristics

During region 1,

$$V_G \approx V_{O(LDO)} e^{-\frac{t}{R_T C_T}} \text{ and } I_D = 0$$

$$\text{So, } t_d = -R_T C_T \ln \frac{V_G}{V_{TH}}$$

Where:

V_{TH} is the FET threshold voltage.

During region 2,

$$V_G \approx V_{PLT} = V_{O(LDO)} - \left(V_{TH} + \frac{I_{inrush}}{gfm_{max}} \right) \approx V_{O(LDO)} - V_{TH} \text{ for } I_{inrush} \text{ small.}$$

$$I_{GD} \approx C_{GD} \frac{d}{dt}(V_{GD}) = C_{GD} \frac{d}{dt}\left[\left(V_{O(LDO)} - V_{TH}\right) - \frac{V_{O(LDO)}}{t_{SS}} t\right]$$

Where:

$V_D = \frac{V_{O(LDO)}}{t_{SS}} t$ is the desired profile for $V_D = V_{OUT}$.

Then,

$$I_{GD} + I_{R_T} + I_{C_T} = 0 \text{ but } I_{C_T} = C_T \frac{dV_{C_T}}{dt} = 0 \quad \text{because } \frac{dV_{C_T}}{dt} = 0$$

So,

$$I_{GD} + I_{C_T} = 0$$

$$\frac{C_{GD} V_{O(LDO)}}{t_{SS}} + \frac{V_{O(LDO)} - V_{TH}}{R_T} = 0$$

$$\frac{V_{O(LDO)} - V_{TH}}{R_T} = \frac{C_{GD} V_{O(LDO)}}{t_{SS}}$$

$$R_T = \frac{\left(V_{O(LDO)} - V_{TH}\right)\left(t_{SS}\right)}{C_{GD} V_{O(LDO)}}$$

The NMOS FET switching characteristics are shown in Figure A-2, which follows.

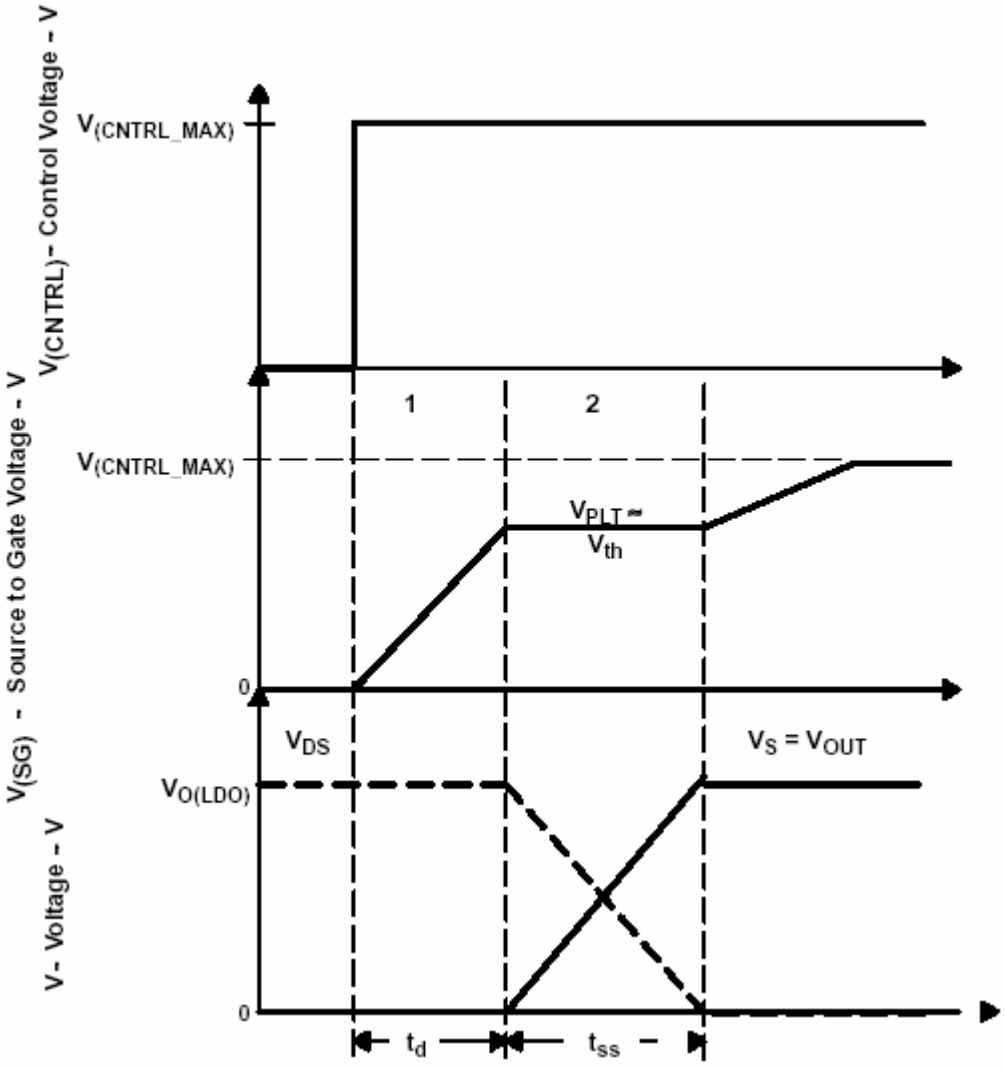

Figure A-2. NMOS Switching Characteristics

During region 2,

$$I_{GD} = C_{GD}\ \frac{dV_{GD}}{dt} = C\frac{d}{dt}\left(V_G - V_{O(LDO)}\right)$$

$$I_{GD} + I_{G-V_{CNTRL}} = 0$$

$$C_{GD}\frac{d}{dt}\left(V_G - V_{O(LDO)}\right) + \frac{V_G - V_{CNTRL}}{R_T} = 0$$

$$C_{GD}\frac{dV_G}{dt} + \frac{V_G}{R_T} - \frac{V_{CNTRL}}{R_T} = 0$$

But,

$$V_G \approx V_S + V_{TH} = V_{OUT} = V_{OUT} + V_{TH}$$

And we want

$$V_{OUT} = \frac{V_{O(LDO)}}{t_{SS}} t$$

So,

$$V_G \approx \frac{V_{O(LDO)}}{t_{SS}} t + V_{TH}$$

Then:

$$C_{GD} \frac{d}{dt}\left[\frac{V_{O(LDO)}}{t_{SS}} t + V_{TH}\right] + \frac{\frac{V_{O(LDO)}}{t_{SS}} t + V_{TH}}{R_T} - \frac{V_{CNTRL}}{R_T} = 0$$

$$\frac{V_{O(LDO)}}{t_{SS}} C_{GD} + \frac{V_{O(LDO)} + V_{TH}}{R_T} - \frac{V_{CNTRL}}{R_T} = 0$$

Need:

$$t = t_d + t_{SS}$$

Solve:

$$V_G = V_{CNTRL}\left(1 - e^{-\frac{t}{R_{GD}C_{GD}}}\right) \text{ for } t$$

$$t_d \approx -R_{GD}C_{GD}\ ln\left(1 - \frac{V_{TH}}{V_{CNTRL}}\right)$$

But for

$$t_{SS} > 100\ \mu s,\ t \approx t_{SS}$$

So,

$$R_T = \frac{V_{CNTRL} - V_{TH} - V_{O(LDO)}}{C_{GD}\frac{V_{O(LDO)}}{t_{SS}}}$$

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265