Disabling the Watchdog Timer for TI's Family of Supervisors

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ABSTRACT

In many microprocessor applications where a watchdog supervisor, such as the TPS3306, is required, it may be necessary to disable the watchdog. This is particularly true when software boot times exceed the watchdog time-out period. This application note describes a circuit that can be used to selectively disable the watchdog timer.

The watchdog timer in many of TI's supervisory circuits can be disabled by leaving the WDI pin open. In this mode, an internal signal is provided to periodically reset the watchdog time-out timer. If the WDI pin is grounded or pulled high, the internal trigger is disabled and watchdog time-outs occur. Table 1 shows several supervisors that feature a watchdog timer that is easily disabled, as well as their minimum time-out periods.

Table 1.   Minimum Watchdog Time-Outs for Supervisor Devices

Device	Minimum Watchdog Time-out (seconds)
TPS36xx	0.48
TPS3820	0.112
TPS3823/4/8	0.9
TPS3305/3705	1.1
TPS3306	0.5
TPS3705	1.1

Applications that require a watchdog timer must make sure the software boot time does not exceed the minimum watchdog time-out period. If the boot time does exceed the watchdog time-out period, the application loops through the boot cycle indefinitely. However, if the circuit shown in Figure 1 is used, the watchdog timer time-out period is effectively extended as long as the boot time requires. This circuit is ideal in applications that have long boot times, but require a watchdog with a short time-out period. Shorter watchdog time-out periods are generally preferred in applications that need to respond quickly to processor fault conditions.
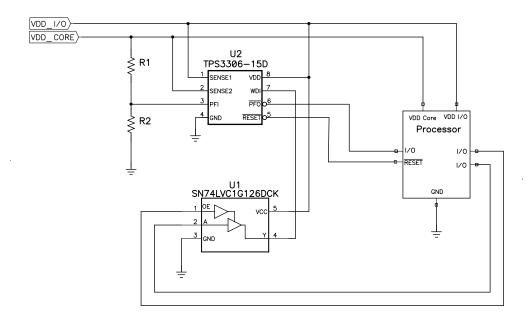
Figure 1. Typical Supervisor Application With 3-State Buffer to Disable Watchdog

In Figure 1, the output enable (pin 1) of the SN74LVC1G126DCK is set low on power-up. This disables the output of the buffer, effectively disconnecting the WDI pin on the TPS3306-15. This allows the software boot time of processor to exceed the normal watchdog time-out period. After the software is loaded, the output of the buffer can be enabled by the processor and normal watchdog time-out conditions apply. However, since the internal watchdog counter is not synchronized to the buffer enable signal, a logic high voltage needs to be present on the input of the buffer before it is enabled. This makes a low to high transition occur on the WDI input as soon as the buffer is enabled. The immediate transition on the WDI input resets the internal watchdog counter. It, also, synchronizes the internal watchdog timer with the external watchdog pulses, thus, preventing a possible watchdog timeout condition.

If the default state of the I/O on power-up is pulled up to Vdd, the SN74LVC1G125DCK can be used in place of the SN74LVC1G126DCK. This device is identical to the SN74LVC1G125DCK except that the output enable pin is inverted. On start-up, the buffer used must stay in the off state to prevent the possibility of overriding the self-generated watchdog trigger of the supervisor.

If a different 3-state buffer is desired, the output leakage when disabled must not exceed 10 µA. If a solid state switch is used the switch must have off leakage of less than 10 µA and be capable of bidirectional current flow.

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