A Step-Down Conversion Concept for a PWM-mode Boost Converter

Christian V. Schimpfle and Jörg Kirchner
Texas Instruments Deutschland GmbH
Haggertystr. 1, D-84356 Freising, Germany
e–mail: c-schimpfle@ti.com, j-kirchner@ti.com

Abstract— A new area efficient approach for regulating the output of boost converters even when the input voltage exceeds the output voltage is presented. Down conversion is achieved without using an LDO and does not require an additional inductor coil and capacitor like the SEPIC or other non-inverting buck-boost converters. The concept is based on a back-gate control of the PMOS type synchronous rectifier to avoid forward biasing of the substrate diode when the circuit is operating in the so-called *down mode*. The converter is implemented in a 10 pin MSOP package and requires only one external inductor and capacitor. The output voltage can be regulated between $1.8V$ and $5.5V$ for output currents up to $200mA$. When working in continuous boost mode, the efficiency is above 85% and goes up to 95%. In down mode efficiency is typical between 55% and 75%. An optional power save or power save mode is implemented to increase efficiency for light loads.

I. Introduction

Todays battery powered portable electronic products need highly efficient power supply solutions in order to increase battery lifetime and to reduce the problem of heat dissipation in highly integrated systems [5], [4], [1]. On the other hand, the output voltage of the supply should be kept constant over a wide range of the input voltage provided by one or more battery cells.

For example it is assumed that the required the supply voltage in a dual cell alkaline, NiCd, or NiMH battery operated system is $2.8V$. Usually a new alkaline cell provides a voltage of $1.6V$ to $1.65V$ which gives up to $3.3V$ for two cells in series for dual cell applications. Fig. 1 shows the discharging of two alkaline cells in series at the input of a boost converter circuit without load and with a resistive load of $\approx 33\Omega$. For at least 90% of the lifetime the battery voltage is below $2.8V$. In this region a boost converter would be the best choice. But since the new cells provide a higher voltage of up to $3.3V$ it is impossible to generate the correct output voltage with a standard boost converter for this case.

One possibility to generate the required $2.8V$ output would be to use a buck-boost converter like the SEPIC or Čuk converter [2], [3] which would provide step-down conversion until the battery cells are discharged to their nominal voltage of $1.5V$ each and then boost conversion until the battery supply is discharged to the minimum accepted input operating voltage of the converter. The main disadvantage of these circuits is that they need at least two inductor coils and one additional capacitor.

The output power of a buck-boost converter is

$$P_{\text{out}} = I_{L,\text{peak}} \cdot V_{\text{peak}} \cdot D \cdot (1 - D) \quad , \qquad (1)$$

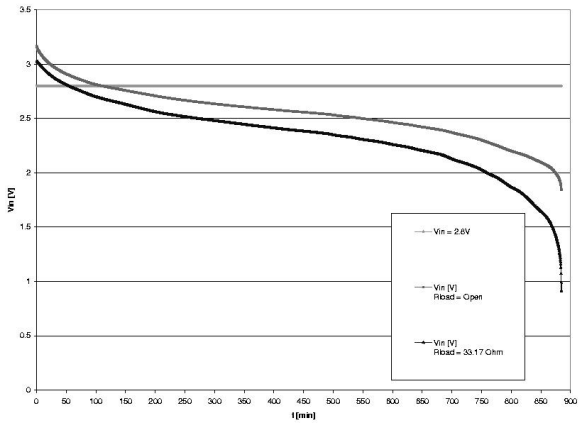

Fig. 1. Discharging of two alkaline cells in series at a boost converter input.

where $I_{L,\text{peak}}$ is the inductor peak current, $V_{\text{peak}} = V_{\text{out}} + V_{\text{in}}$ and D is the duty cycle. The maximum output power $P_{\text{out}} = P_{\text{out,max}}$ is reached for $D = 0.5$, $V_{\text{out}} = V_{\text{in}}$. For a boost converter the output power is

$$P_{\text{out}} = I_{L,\text{peak}} \cdot V_{\text{out}} \cdot (1 - D) \quad , \qquad (2)$$

and $P_{\text{out}} = P_{\text{out,max}}$ for $D = 1$, $V_{\text{out}} = V_{\text{in}}$. From (1) and (2) it can be derived that for a boost converter $P_{\text{out,max}} = I_{L,\text{peak}} V_{\text{peak}}$ whereas for a buck-boost converter $P_{\text{out,max}} = 0.25 I_{L,\text{peak}} V_{\text{peak}}$. This means that for the same values of the limiting factors $I_{L,\text{peak}}$ and V_{peak} a buck-boost converter can provide only $1/4$ of the maximum output power of a boost converter.

Another possibility is to use a low drop-out regulator (LDO) with a preceeding boost converter stage that provides an input voltage for the LDO that exceeds the required LDO output voltage ($2.8V$ in this example) at least by the drop-out voltage over the entire battery lifetime. Once the battery voltage drops below $2.8V$ a simple boost converter would be a much more efficient solution.

This paper presents a concept for a boost converter that is able to regulate the output voltage to its nominal value even when the input voltage exceeds the output voltage. This is achieved by a specific control for the synchronous rectifier and the duty cycle and does neither require any additional inductors or capacitors nor a LDO.

0-9999-9999-0/03/$17.00 ©2003

The paper is structured as follows: Section II explains the circuit architecture and the different operating modes, Section III presents the control strategy. Section IV shows the results from measurements of the chip implementation. Finally some concluding remarks are made in Section V.

II. Circuit Architecture

The circuit architecture of the boost converter is shown in Fig. 2. The integrated part on the chip (within the dotted box) includes a standard topology for a boost converter with synchronous rectifier, the back-gate control and the voltage mode control unit for the MOS switches.

For the synchronous rectifier a low dissipative PMOS transistor is used. The back-gate of the PMOS can be switched between the V_{out} and SW node. For startup where $V_{\mathrm{in}} \geq V_{\mathrm{out}}$, the back-gate is connected to the SW node and the PMOS is working as a current source in order to charge C_{out} to $\approx V_{\mathrm{in}}$. Let $V_{\mathrm{out,nom}}$ be the nominal output voltage. If $V_{\mathrm{in}} < V_{\mathrm{out,nom}}$ the converter switches into boost mode, otherwise for $V_{\mathrm{in}} \geq V_{\mathrm{out,nom}}$ the circuit starts to operate in down mode.

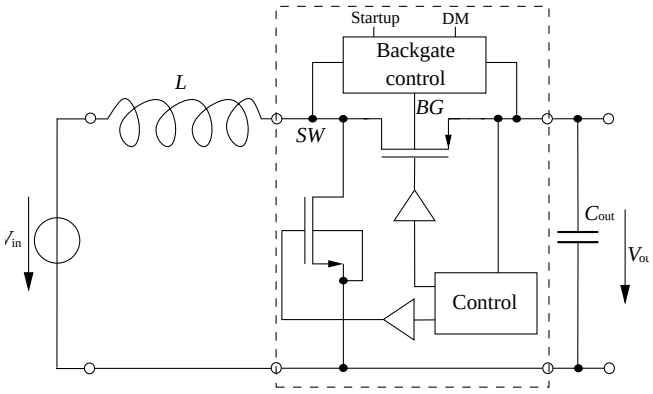

Fig. 2. Blockdiagram of the boost converter with down conversion capability.

A. Boost Mode

In boost mode the back-gate of the PMOS switch is connected to V_{out}. The PMOS gate is switched between V_{out} during the NMOS on-time t_{on} and $0V$ during the NMOS off-time t_{off}. Under the assumption that the switches are ideal the common formula for the duty cycle of a boost converter is

$$D = \frac{V_{\mathrm{out}} - V_{\mathrm{in}}}{V_{\mathrm{out}}} \quad . \tag{3}$$

Fig. 3 shows the equivalent circuit for the boost mode. The average inductor current of the boost converter is

$$I_{L,\mathrm{avg}} = \frac{I_{\mathrm{out}}}{1-D} \quad . \tag{4}$$

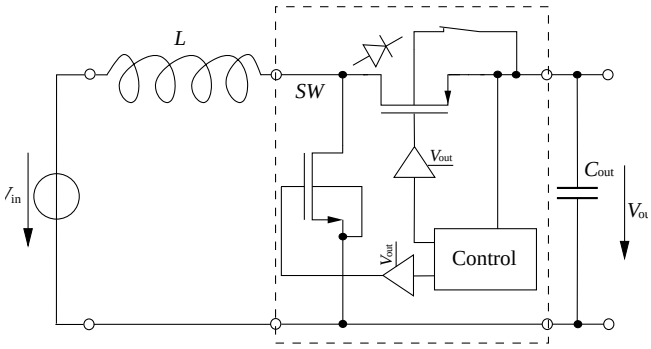

Fig. 3. Schematic of the converter in boost mode.

If the minimum of the inductor current just reaches zero as shown in Fig. 4, the peak value is

$$I_L(t_0 + t_{\mathrm{on}}) = \frac{1}{L} \cdot V_{\mathrm{in}} t_{\mathrm{on}} \quad . \tag{5}$$

Under these conditions the average inductor current within one clock period is given by

$$I_{L,\mathrm{avg(border)}} = \frac{1}{2L} \cdot V_{\mathrm{in}} t_{\mathrm{on}} \quad . \tag{6}$$

For light loads the inductor current can become negative. In

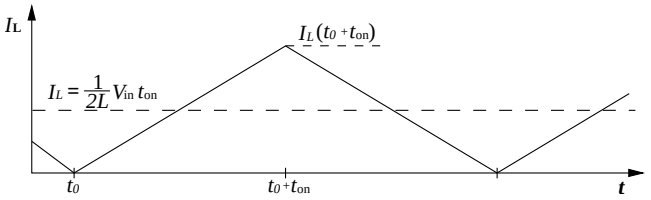

Fig. 4. Inductor current at border from continuous mode to power save mode.

order to avoid that current flows back from the output across the PMOS and the inductor to V_{in} for a certain amount of time, the circuit starts then to operate in power save mode as long as V_{out} is within the accepted tolerance. This means that rather than running in less efficient discontinuous mode the converter is switched into an idle state where both, NMOS and PMOS, are not conducting and most of the functional blocks are completely switched off in order to save power and thus improve efficiency. The converter starts working again as soon as the output voltage falls below the predefined tolerance level $V_{\mathrm{out,low}}$. From (4) and (6), the condition for power save mode can be formulated:

$$\begin{aligned} I_{L,\mathrm{avg}} &< I_{L,\mathrm{avg(border)}} \Longrightarrow \\ I_{\mathrm{out}} &< \frac{1}{L} \cdot V_{\mathrm{in}} t_{\mathrm{on}} \cdot (1-D) \\ \text{and} \quad V_{\mathrm{out}} &> V_{\mathrm{out,low}} \quad . \end{aligned} \tag{7}$$

B. Down Mode

The condition for down mode can simply be formulated by

$$V_{\mathrm{in}} \geq V_{\mathrm{out}} \quad . \tag{8}$$

During the startup phase the down mode must be disabled as long as V_{out} has not yet reached its nominal value. Fig. 5 shows the equivalent circuit for down mode. Note that if

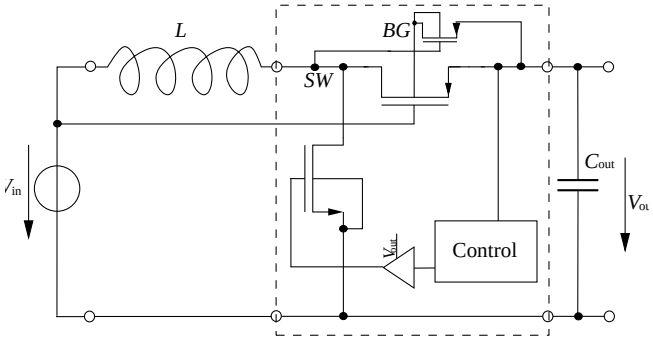

Fig. 5. Schematic of the converter in *down mode*.

the PMOS is turned on during the off-time of the NMOS as in standard boost mode, the voltage at SW is V_{out} and there is a positive voltage drop with the value $V_{\mathrm{in}} - V_{\mathrm{out}}$ across the inductor. As a consequence the current in the inductor rises by $\Delta I_L = L \cdot (V_{\mathrm{in}} - V_{\mathrm{out}})$. This means that I_L increases during the on-time as well as during the off-time of the NMOS switch and the condition of *equal volt-seconds* for PWM mode DC-DC converters is violated. Under these conditions the inductor current would rise until $V_{\mathrm{out}} \geq V_{\mathrm{in}}$.

Therefore it must be guaranteed that the PMOS switch always remains turned off in down mode. In order to achieve this, the PMOS gate is clamped to V_{in} as shown in Fig. 5. When turning off the PMOS by setting the gate to V_{out} level as in boost mode, the transistor would be turn on as soon as V_{in} exceeds V_{out} by the PMOS threshold voltage $V_{\mathrm{T,p}}$.

In down mode the back-gate pin BG of the PMOS can no longer be connected to V_{out} as it is in boost mode because the back-gate diode would be forward biased for $V_{\mathrm{in}} - V_{\mathrm{out}} > V_{\mathrm{d}}$, where V_{d} is the diode voltage of $\approx 0.7V$. The back-gate control now disconnects the PMOS back-gate from V_{out} and ensures that the back-gate diode is not forward biased. When the NMOS switch is conducting in down mode, the back-gate of the PMOS is tied to V_{out} by another small PMOS device ($M3$). A possible implementation for the switches in the back-gate control circuit is shown in Fig. 6. It consists of two PMOS transistors used as switches. Transistor $M1$ connects BG to SW during startup when $V_{\mathrm{out}} < V_{\mathrm{in}}$ and the transistor is working as a current source to charge the output capacitor. Transistor $M2$ connects BG to V_{out} in boost mode, where the signal DM = "0" indicates that down mode is not active. Connecting the back-gate of $M2$ to BG guarantees that

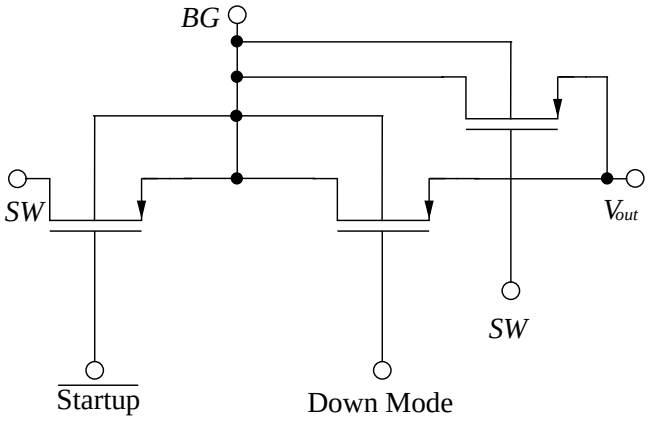

Fig. 6. Back-gate control switches .

the back-gate diode of $M2$ is not forward biased in down mode and that there is no current flowing through the back-gate. Thus the transistors $M1$, $M2$, and $M3$ can be kept small compared to the large NMOS and PMOS switches.

In continuous boost mode the voltage at SW changes between $0V$ and V_{out}. In down mode, where the PMOS is not actively turned on during the NMOS off-time, the SW voltage toggles between $0V$ and $V_{\mathrm{in}} + V_{\mathrm{T,p}}$. When the down mode is active the converter can operate in continuous mode as well as in power save mode. The conditions for power save mode are the same as described in (7). Fig. 7 shows an oscilloscope plot of the SW voltage at the changeover from boost mode to down mode. In both modes the converter is switch-

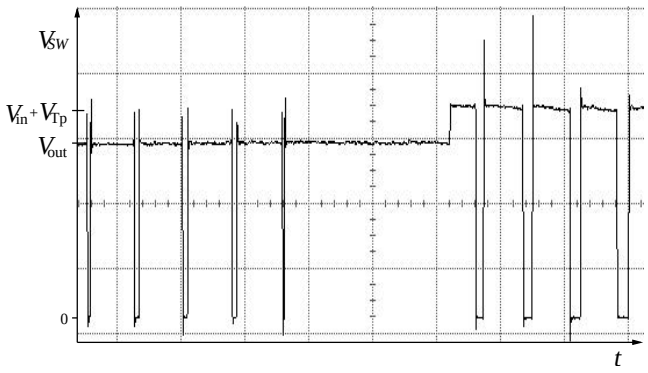

Fig. 7. Signal at SW at the changeover from boost mode (left) to down mode.

ing continously. The break between boost and down mode is generated by the control as the NMOS on-time at $V_{\mathrm{in}} \approx V_{\mathrm{out}}$ becomes so small that some pulses (NMOS switching operations) are skipped.

III. Voltage Mode Control Scheme

The output voltage regulation of the presented converter is based on a fixed frequency voltage mode control. For boost mode the duty cycle control algorithm is given in (3). The implementation of this algorithm that automatically controls the NMOS off-time $t_{\rm off}$ and thus the duty cycle consists of two blocks: A current generator and a timer unit. In boost mode the current generator block generates a current which is proportional to $V_{\rm out}$. It also provides the reference voltage for for a RC-oscillator that generates clock pulses in time intervals $T = RC$. In the timer a capacitor, also with capacitance C, is charged to $V_{\rm in}$ after each time interval T and discharged by the current I from the current generator. For better accuracy the discharging current is adjusted by an error amplifier. The capacitor voltage is compared with a fixed voltage level (for ideal MOS switches this is ground level). Once the capacitor is discharged to this level a comparator generates a pulse that indicates the end of the NMOS off-time and the NMOS switch is turned on. It is turned off again with the next clock pulse from the oscillator.

In the following the control algorithm for down mode is described in more detail. For down mode operation the duty cycle also can be derived from the principle of equal volt-seconds by inspection of Fig. 5. Neglecting the resistive losses of the NMOS and PMOS switches, the voltages across the inductor during on- and off-time of the NMOS are given by

$$\begin{aligned} V(t_{\rm on}) &= V_{\rm in} \\ V(t_{\rm off}) &= -V_{\rm T,p} \quad . \end{aligned} \tag{9}$$

Applying the principle of equal volt-seconds gives

$$\begin{aligned} 0 &= t_{\rm on} \cdot V_{\rm in} + t_{\rm off} \cdot (-V_{\rm T,p}) \\ T &= t_{\rm on} + t_{\rm off} \\ D &= \frac{t_{\rm on}}{T} = \frac{V_{\rm T,p}}{V_{\rm in} + V_{\rm T,p}} \quad . \end{aligned} \tag{10}$$

For a fixed frequency $f = \frac{1}{T}$ regulating the NMOS off-time with

$$t_{\rm off} = T \frac{V_{\rm in}}{V_{\rm in} + V_{\rm T,p}} \tag{11}$$

gives the required duty cycle from (10).

Fig. 8 explains in principle the function of the off-time controller in down mode. The current generator block provides a current that is proportional to $V_{\rm in} + V_{\rm T,p}$. In the timer a capacitor C is charged to $V_{\rm in}$ in intervals $T = RC$ and discharged with the current $I = (V_{\rm in} + V_{\rm T,p})/R$ from the current generator. A simple comparator then generates pulses in intervals of $t_{\rm off}$. Obviously R and C of the oscillator must match with the R in the current generator and the C in the timer respectively. In order to achieve a required

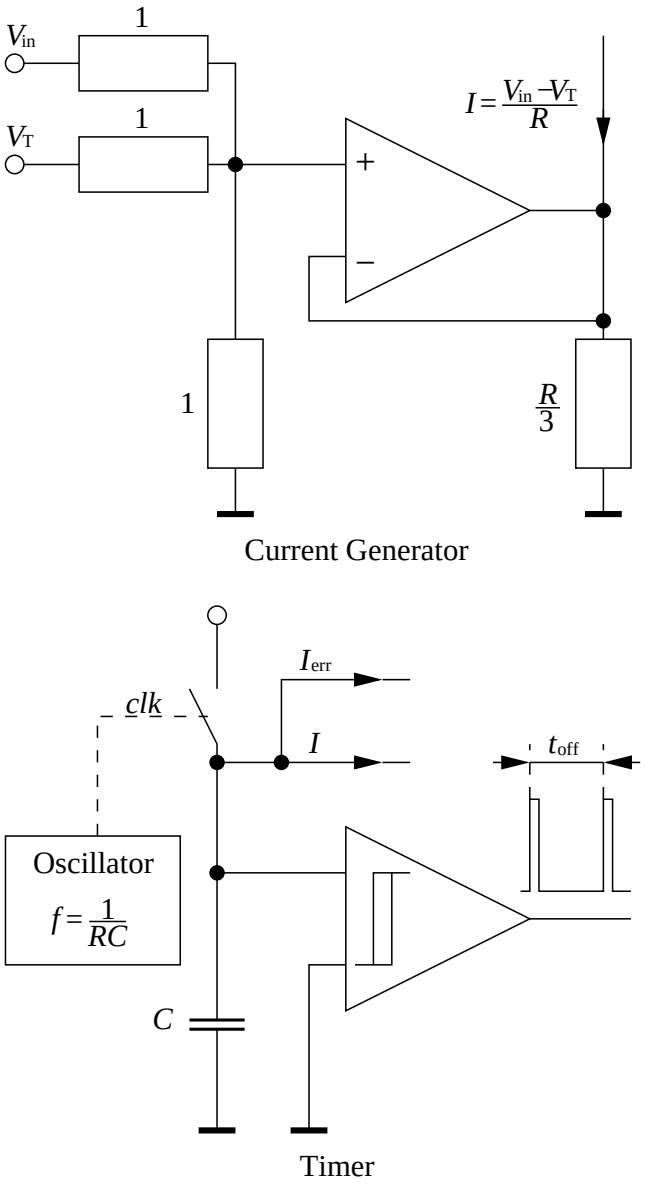

Fig. 8. Controller scheme for down mode.

accuracy, the error amplifier delivers a current $I_{\rm err}$ which is derived from an error signal proportional to $|V_{\rm out} - V_{\rm nom}|$, where $V_{\rm nom}$ is the required nominal output voltage. Note that only the current generator operation differs in boost and down mode, whereas all other parts of the controller have identical function in both modes.

IV. Experimental Results

The presented converter is implemented in a chip for 1-3 cells alkaline or NiCd/NiMH applications, e.g. internet audio players or PDA's. The input voltage range goes from $0.9V$ to 5.5 volts, the output voltage can be adjusted between $1.8V$

and $5.5V$.

In theory V_{in} can exceed V_{out} by any value. Practically the larger power dissipation in the PMOS switch in down mode operation must be taken into account. The voltage drop across the PMOS in down mode is $V_{\mathrm{in}} + V_{\mathrm{T,p}} - V_{\mathrm{out}}$. The power dissipation in the PMOS in down mode can than be calculated by

$$P_{\mathrm{PMOS,DM}} = I_{\mathrm{out}} \cdot (V_{\mathrm{in}} + V_{\mathrm{T,p}} - V_{\mathrm{out}}) \quad . \tag{12}$$

Depending on the thermal resistance of the chip environment, a maximum acceptable V_{in} can be calculated for a given V_{out} and I_{out} and must be taken into account for practical applications. For the measurements presented here V_{in} is restricted to exceed V_{out} by maximum $1.5V$.

One of the most interesting parameters of the converter is its efficiency. For the measurements made here the output voltages are fixed. Input voltage and load current are varied in order to determine the efficiency over a wide range of possible operating points and all the different modes. All measurements shown were made at 25^oC.

In Fig. 9 a 3D-plot for the efficiency with disabled power save mode is shown. The output voltage is $3.3V$. One can clearly identify the border between boost and down mode. In boost mode, the efficiency for load currents larger than $\approx 20mA$ is above 90%.

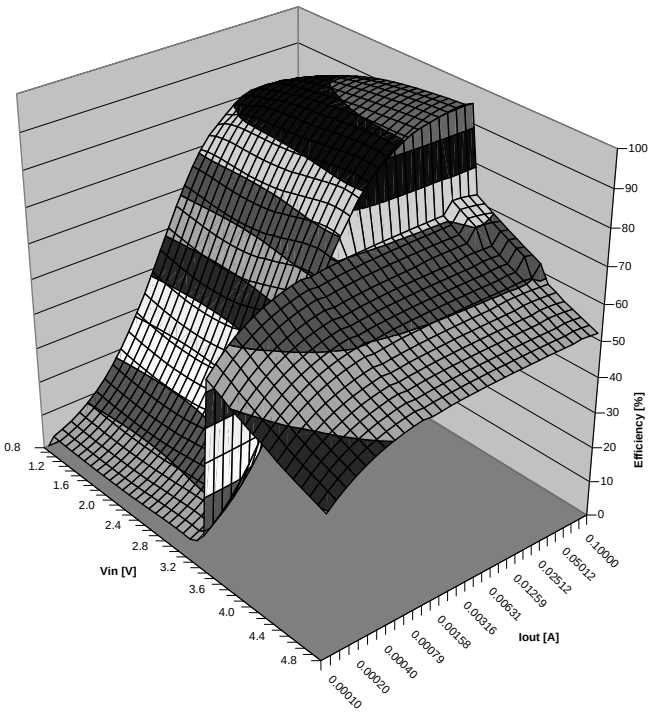

Fig. 9. Efficiency for $V_{\mathrm{out}} = 3.3V$ with power save mode disabled.

For lighter loads the efficiency falls continously as the inductor current becomes negative for certain times and flows from the output back to the input. Note that there is no discontinuous mode, where I_L would remain zero instead of falling to negative values. In down mode there is a clear gap in efficiency compared to boost mode. This is caused by the resistive losses in the PMOS channel. In down mode the converter is always allowed to go into power save mode, therefore the efficiency for light loads is higher than in boost mode if the power save mode is disabled.

A many times smoother efficiency distribution is achieved if the power save mode is enabled. Fig. 10 shows the 3D-plot again for an output voltage of $3.3V$. For light loads the converter is now temporarily in an idle state, where most of the internal blocks are disconnected from the supply and NMOS and PMOS are turned off. The efficiency is plotted

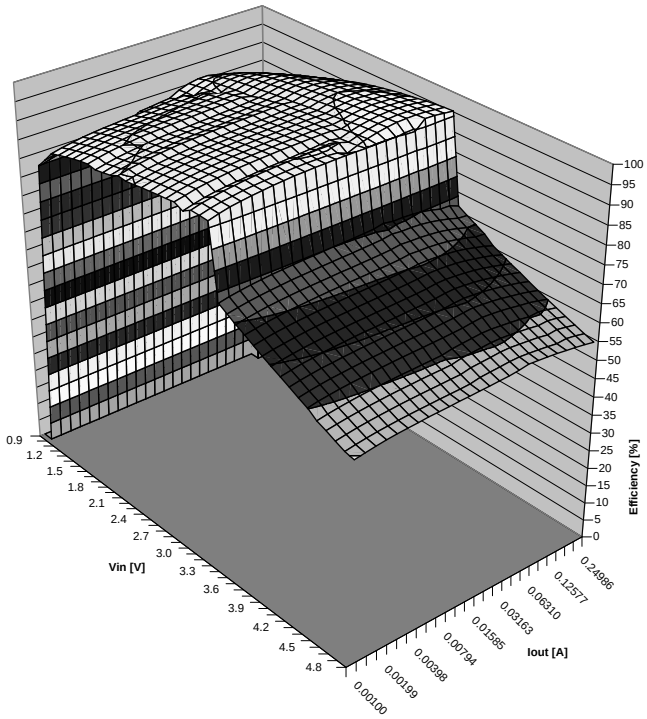

Fig. 10. Efficiency for $V_{\mathrm{out}} = 5.5V$ with power save mode enabled.

for loads up to $250mA$. This plot also shows the striking step at $V_{\mathrm{in}} = V_{\mathrm{out}}$. However, the efficiency in down mode is still in a range between 55% and 72%.

The load regulation of the converter for different input voltages is shown in Fig. 11. Under the conditions shown in the diagram the nominal output voltage of $3.3V$ is kept within -0.6% and 1.1%. The control loop is designed to regulate V_{out} within an accuracy of $\pm 1.6\%$. Taking mismatch into account the overall accuracy can be guaranteed to be within $\pm 3\%$.

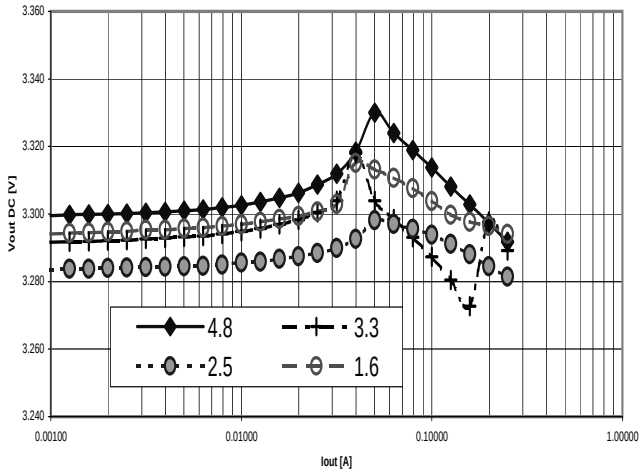

Fig. 11. Load regulation.

V. Conclusion

This paper presents a new concept for a low power DC-DC converter with step-down conversion option that does not require any additional inductors or capacitors and no LDO. The concept addresses applications where the required supply voltage is slightly below the available battery voltage when the battery is fully charged. As soon as the battery is discharged below the required nominal supply voltage, the converter works as a standard boost converter. The new down conversion mode requires a special control for the back-gate of the power PMOS device, which operates as a synchronous rectifier. As soon as V_{in} exceeds V_{out} the PMOS is no longer turned on actively by connecting the gate to ground. This guarantees that the voltage across the inductor is negative during the off-time of the power NMOS switch and therefore the principle of equal volt seconds is still valid. In this mode the resistive losses in the PMOS channel are larger than in standard boost mode. Thus the efficiency is less. Furthermore the maximum value by which V_{in} can exceed V_{out} is restricted not only by the voltage capability of the process technology but also by the thermal resistance of the environment around the PMOS device.

The presented concept is implemented in a chip which is assembled in a MSOP10 package with heat pad, allowing V_{in} to be $1.5V$ larger than V_{out} even under worst case conditions. Measurements show that the efficiency in boost mode is typically $> 90\%$ and goes up to 95%. In down conversion mode the efficiency is in a range between 55% and 75%. Due to its down conversion capability the presented converter is an area-, cost-, and power-efficient solution for a wide range of battery driven applications.

References

[1] R. W. Erkison and D. Maksimovic. *Fundamentals of Power Electronics*. Kluwer Academic Publishers, 2001.

[2] D. Maksimovic and S. Ćuk. Switching Converters with Wide DC Conversion Range. *Proceedings HFPC*, Seiten 217–225, May 1989.

[3] R. P. Massey and E. C. Snyder. High-Voltage Single-Ended Dc-Dc Converter. *Proceedings IEEE Power Electronic Specialists Conference*, Seiten 156–159, June 1977.

[4] R. D. Middlebrook. Power Electronics: An Emerging Discipline. *Proceedings IEEE International Symposium on Circuits and Systems*, April 1981.

[5] R. D. Middlebrook. Power Electronics: Topologies, Modeling, and Measurement. *Proceedings IEEE International Symposium on Circuits and Systems*, April 1981.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265