Using Low Voltage SWIFT™ DC/DC Converters With Ceramic Capacitors

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ABSTRACT

This application note investigates an adequate phase margin for stable operation of SWIFT™ regulators with the ceramic capacitors at worst-case tolerances of regulator and external parts. TI also shows how the bandwidth and gain of feedback loop impact on load-current transient-response characteristics. Measurements and analysis have shown that the voltage-mode control SWIFT™ regulators with ceramic capacitors provide reliable solution at 3-V to 6-V input voltage and up to 9-A load-current range. This note shows that the optimum between reliable stable operation and fast transient response can be achieved with 45-degrees phase margin and 100 kHz crossover frequency at nominal operating conditions, thus, successfully matching current-mode controllers in this application area.

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1 Introduction

As the capacitance-to-size ratio of modern ceramic capacitors with X5R, X7R dielectric has increased dramatically within the last few years, the use of switching dc-dc converters with ceramic output capacitors has become a very popular filter solution. This popularity is due to low cost, better filtering capability at high frequency, and thermal stability of X5R, X7R ceramic capacitors. The description and test results of converters based on SWIFT™ regulators with ceramic capacitors are provided in TI's document: *TPS54610EVM-213 6-Amp, TPS54810EVM-213 8-Amp, TPS54910EVM-213 9-Amp,* user's guide (SLVU071)[2]. The test results provided in the user's guide show that SWIFT™ regulators with voltage mode control take advantage of low-cost ceramic capacitors to provide low output voltage ripple.

For stable operation of switching dc-dc converters with ceramic output capacitors, an adequate phase and gain margin of frequency response characteristics needs to be provided. Most recommendations and design rules showing how to select bandwidth and phase-margin of feedback loops are based on industry's longtime experience with electrolytic capacitors. Usually, phase margin in the range from 45 to 60 degrees is recommended to avoid instability caused by feedback-loop variation because of components and parameter tolerances. The crossover frequency or feedback-loop bandwidth usually does not exceed 30 kHz. Output capacitor parameters and their tolerances have the most significant impact on feedback-loop bandwidth and phase-margin selection of the regulator. Most electrolytic output capacitors have significant capacitance and ESR (equivalent series resistance) variations depending on temperature, frequency, and differences from sample to sample. The capacitance and ESR of electrolytic capacitors can vary by 2 to 3 times, or even more, depending on the type of capacitor and operating condition. ESR of the output capacitor and its variation should be taken into account during the feedback loop design because one of the poles of the compensation circuit is selected to cancel the ESR related zero of the regulator frequency response. The variation of output capacitance changes the corner frequency of output L-C filter. This fact also needs to be taken into account during the compensation circuit design. Because of wide tolerances and variations, electrolytic capacitors require a rather conservative approach when selecting the phase margin. At least 60 degrees phase margin at nominal operation condition is recommended for the electrolytic output capacitors.

Ceramic capacitors with X5R or X7R dielectric have much lower parameter variations and tolerances in comparison to the electrolytic capacitors. The latest ceramic capacitors have capacitance in 10-μF to 100-μF range with extremely low ESR—about 2 mΩ to 5 mΩ only. Their capacitance has relatively low ±20% tolerance. The ESR-related frequency-response zero of ceramic capacitors is located in the MHz range. It is far above the typical crossover frequency, usually selected below 1/5 of the switching frequency, and thus the ESR-zero has no impact on the design. In the SWIFT™ regulators case, the crossover frequency never exceeds 150 kHz [3]. Low tolerances and variations of modern ceramic capacitors make it possible to increase the bandwidth of feedback loop up to 100 kHz, with 45 degrees phase-margin at nominal condition, using simple voltage-mode control. Higher bandwidth and gain improves the dynamic response of the feedback loop at large-signal transients, including load-current steps. Achieved load-current transient response, shown in this application note, meets requirements of most practical applications with the minimum number of output capacitors. Test results show that the voltage-mode control implemented in SWIFT™ regulators is very competitive in comparison with the more expensive and noise-sensitive current-mode control.

2 Main Tolerances of Feedback Loop

The SWIFT™ regulators with external compensation implement voltage-mode control with Type 3 compensation circuits. The following parameters need to be considered for the worst-case analysis:

- Operation conditions—include input voltage and load resistance range.
- Power stage parameters—include the output inductor and capacitor tolerance, resistance of power FETs and output inductor. Variations of these parameters are important because the corner frequency and damping factor of the L-C output filter depends on these parameters.
- Internal error amplifier and PWM modulator tolerances—include gain and bandwidth of error amplifier, ramp-signal variation and phase drop associated with the delays and sampling of the modulator
- External compensation circuit—3 resistors and 3 capacitors in case of Type 3 compensation, and their tolerances

The standard evaluation module with ceramic capacitors, TPS54610EVM-213 provided by Texas Instruments, has been used for measurements and analysis in this application note. First, the Bode plots of the evaluation module have been measured using the Venable system for the entire input voltage and load current range. Then, the impact of output capacitance change on frequency, and load-current transient response has been measured. It was verified in previous experiments, that modulator delays and sampling have negligible impact on frequency response in the case of SWIFT™ regulators. Because of that, the delays and sampling can be excluded from the consideration of worst-case analysis.

An analytical model of frequency response, including all mentioned variables and tolerances, has been generated and compared with measured Bode plots using Mathcad software. The analytical model and measurements match each other with practically sufficient accuracy. After the verification, this analytical model has been used for the worst-case analysis, where all remaining tolerances have been included. It is shown that 45-degrees phase margin and 100 kHz crossover frequency of SWIFT™ regulators, with ceramic capacitors at nominal operating conditions, is an optimum tradeoff for reliable, stable operation, and fast transient response.

The analysis in this application note is adequate for other modifications of evaluation module TPS54X10EVM-213 with TPS54810 and TPS54910 regulators. It can be applied also to other members of the SWIFT™ family where the similar output filter and compensation circuit is implemented.

3 Evaluation Module TPS54610EVM-213

Schematic and bill of materials of evaluation module TPS54610EVM-213 are shown in Figure 1 and Table 1 accordingly. The switching frequency during tests and analysis is selected 700 kHz.

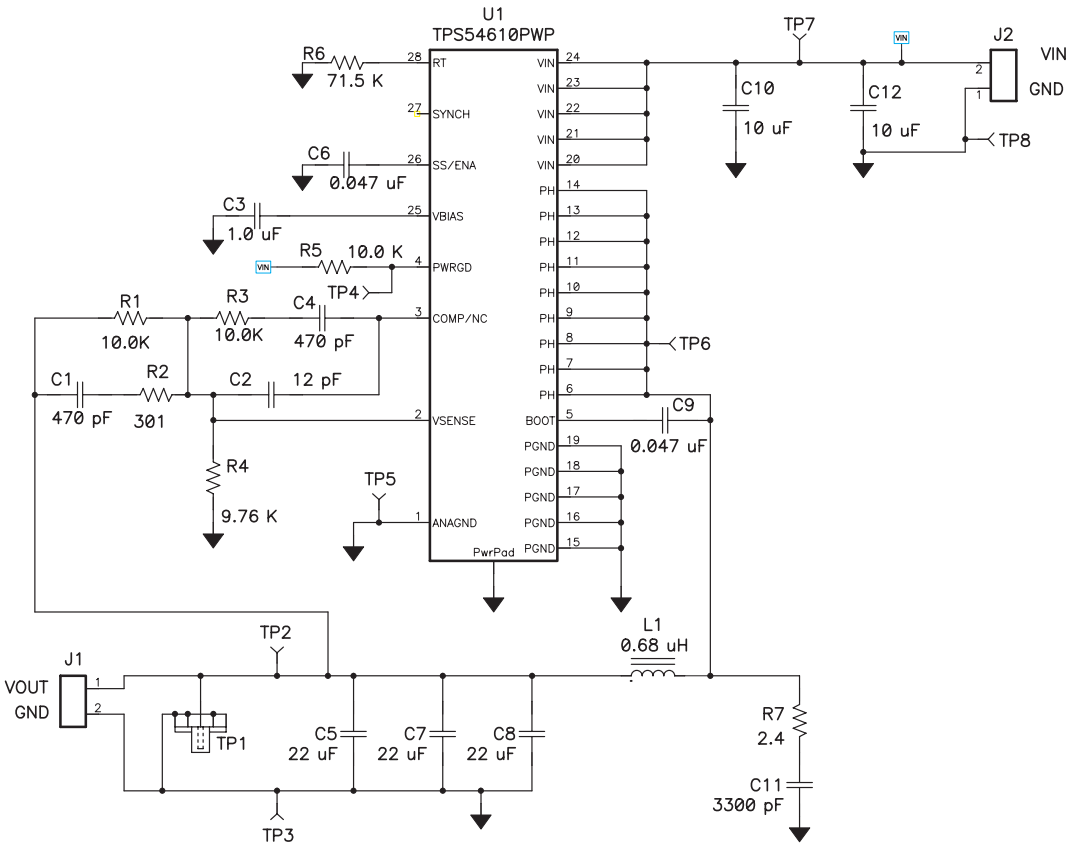


Figure 1. Electrical Schematic of Evaluation Module TPS54610EVM-213

Table 1. Bill of Materials of Evaluation Module TPS54610EVM-213

COUNT	REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
2	C1, C4	Capacitor, ceramic, 470 pF, 50 V, X7R, 10%	603	Panasonic	ECJ-1VB1H471K
2	C10, C12	Capacitor, ceramic, 10 µF, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	C11	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Panasonic	ECJ-1VB1H332K
1	C2	Capacitor, ceramic, 12 pF, 50 V, X7R, 10%	603	Panasonic	ECU-V1H120KBV
1	C3	Capacitor, ceramic, 1 µF, 10 V, X5R, 10%	603	TDK	C1608X5R1A105M
3	C5, C7, C8	Capacitor, ceramic, 22 µF, 6.3 V, X5R, 20%	1210	Taiyo Yuden	JMK325BJ226MN
2	C6, C9	Capacitor, ceramic, 0.047 µF, 25 V, X7R, 10%	603	Murata	GRM188R71E473KA01
2	J1, J2	Terminal block, 2 pin, 15 A, 5,1 mm	148830	OST	ED1609
1	L1	Inductor, SMT, 0.65 µH, 12 A, 5 mΩ	0.34” × 0.25”	Pulse	PA0277
3	R1, R3, R5	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Panasonic	ERJ-3EKF1002
1	R2	Resistor, chip, 301 Ω, 1/16 W, 1%	603	Panasonic	ERJ-3EKF301
1	R4	Resistor, chip, 9.76 kΩ, 1/16 W, 1%	603	Std	Std
1	R6	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	R7	Resistor, chip, 2.4 Ω, 1/8 W, 1%	1206	Panasonic	ERJ-8RQF2R4
1	TP1	Adaptor, 3,5-mm probe clip (or 131-5031-00)	72900	Tektronix	131-4244-00
4	TP2, TP4, TP6, TP7	Test point, red, 1 mm	0.038”, 6400”	Farnell	240-345
3	TP3, TP5, TP8	Test point, black, 1 mm	0.038”, 6400”	Farnell	240-333
1	U1	IC, IFET power controller, 3 V to 6 V, 6 A	PWP28	TI	TPS54610PWP
1	—	PCM, 3 in × 3 in × 0.065 in		Any	SLVP213

Before further analysis, it is reasonable to show why ceramic capacitors are so attractive in terms of size and ripple. The waveforms in Figure 2 show the switching waveforms and output voltage ripple of TPS54610 regulator with 3 x 22-µF output ceramic capacitors. The waveforms in Figure 3 relate to the same regulator with 2 x 150-µF output SP-type capacitors. Both regulators have the same 0.68-µH output inductor, and they are running at the same switching frequency of about 700 kHz. The input voltage is 5 V and the output voltage is 1.8 V for these measurements. One can see that the peak-to-peak ripple of much smaller ceramic capacitors is only 7.2 mV, while the overall 5 times more expensive SP capacitors have peak-to-peak ripple 24 mV.

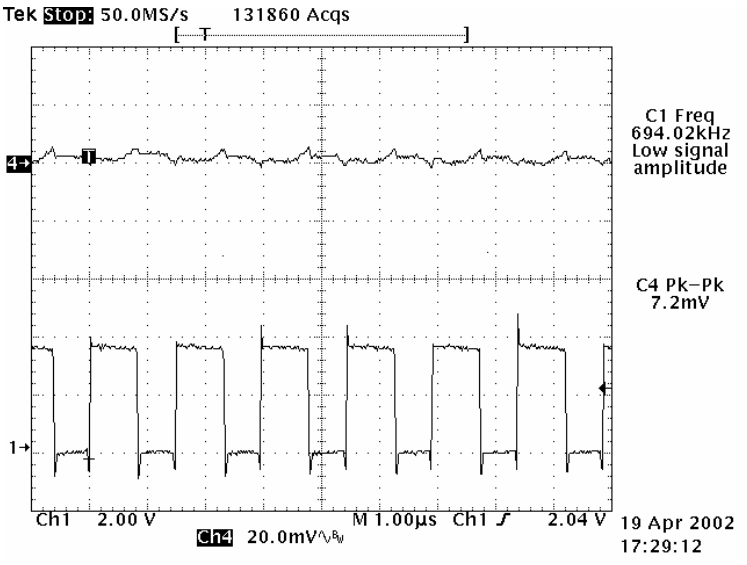


Figure 2. Output Ripple and Switching Waveforms With 3 x 22-µF Ceramic Capacitors

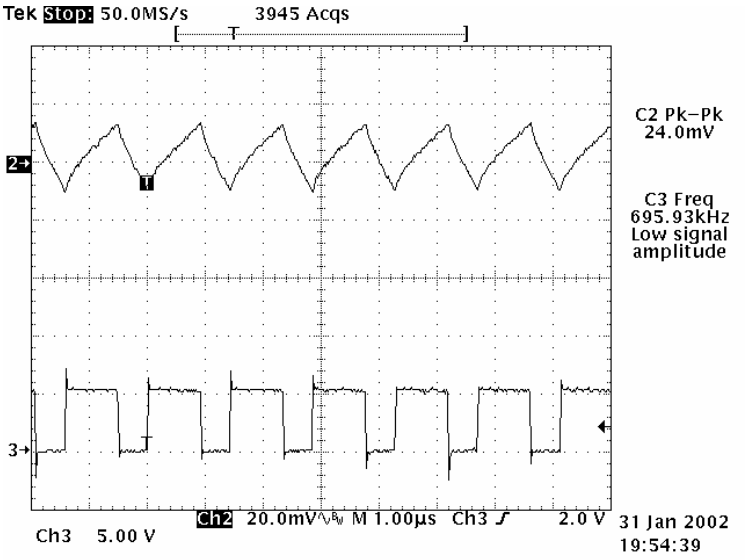


Figure 3. Output Ripple and Switching Waveforms With 2 x 150-µF SP-Type Capacitors

4 Frequency Response

Bode plots measured at input voltages 3.3 V, 5 V and 6 V are shown below for no-load (Figure 4) and R_L = 0.24 Ω (Figure 5) conditions.

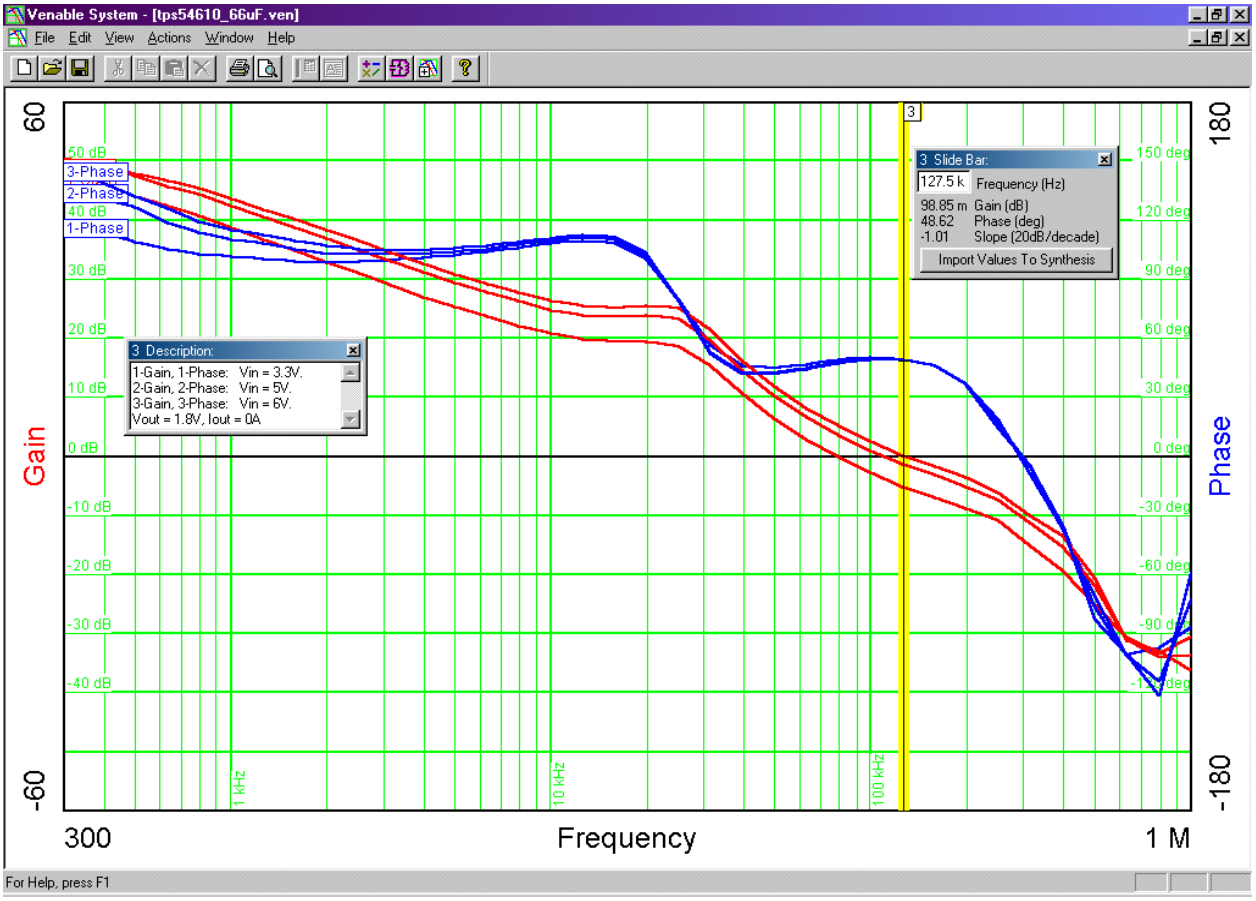


Figure 4. Gain and Phase at No-Load Condition With C_O = 66 μF

One can see that the phase does not depend significantly on input voltage. The worst-case condition in terms of phase-margin is at the maximum input voltage, where there is the highest gain and crossover frequency. The maximum crossover frequency in this measurements is 127 kHz at V_I = 6 V, while the lowest phase margin is 48.6 degrees.

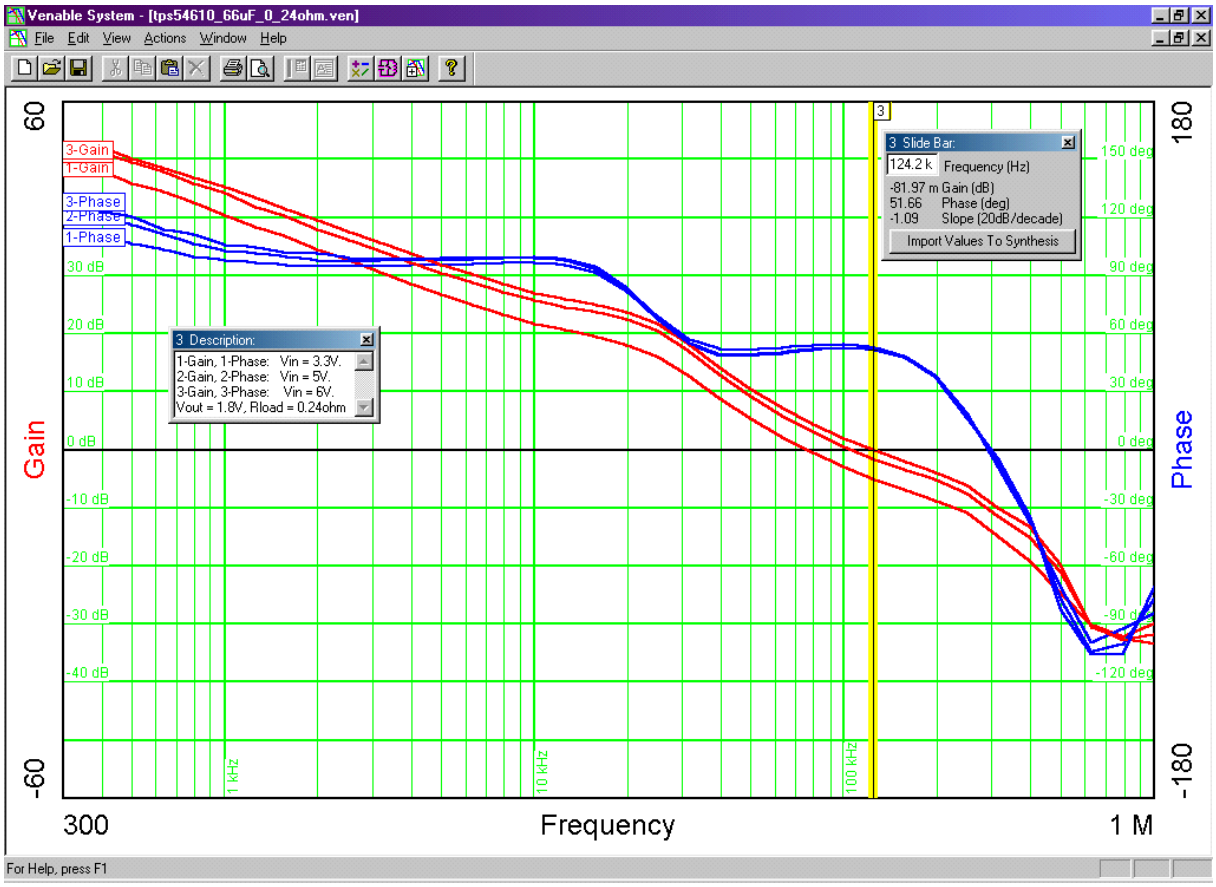


Figure 5. Gain and Phase at R_L = 0.24 Ω (I_O = 7.5 A) With C_O = 66 μF

The next step is to verify frequency response when the output capacitor has its minimum and maximum value. This particular EVM has three 22-μF capacitors in parallel for the output filter. The Bode plots with one of them removed (33.3% capacitance decrease) are shown in Figure 6. One can see that the crossover frequency has increased up to 203 kHz. At the same time, the phase-margin has decreased down to 35.8 degrees.

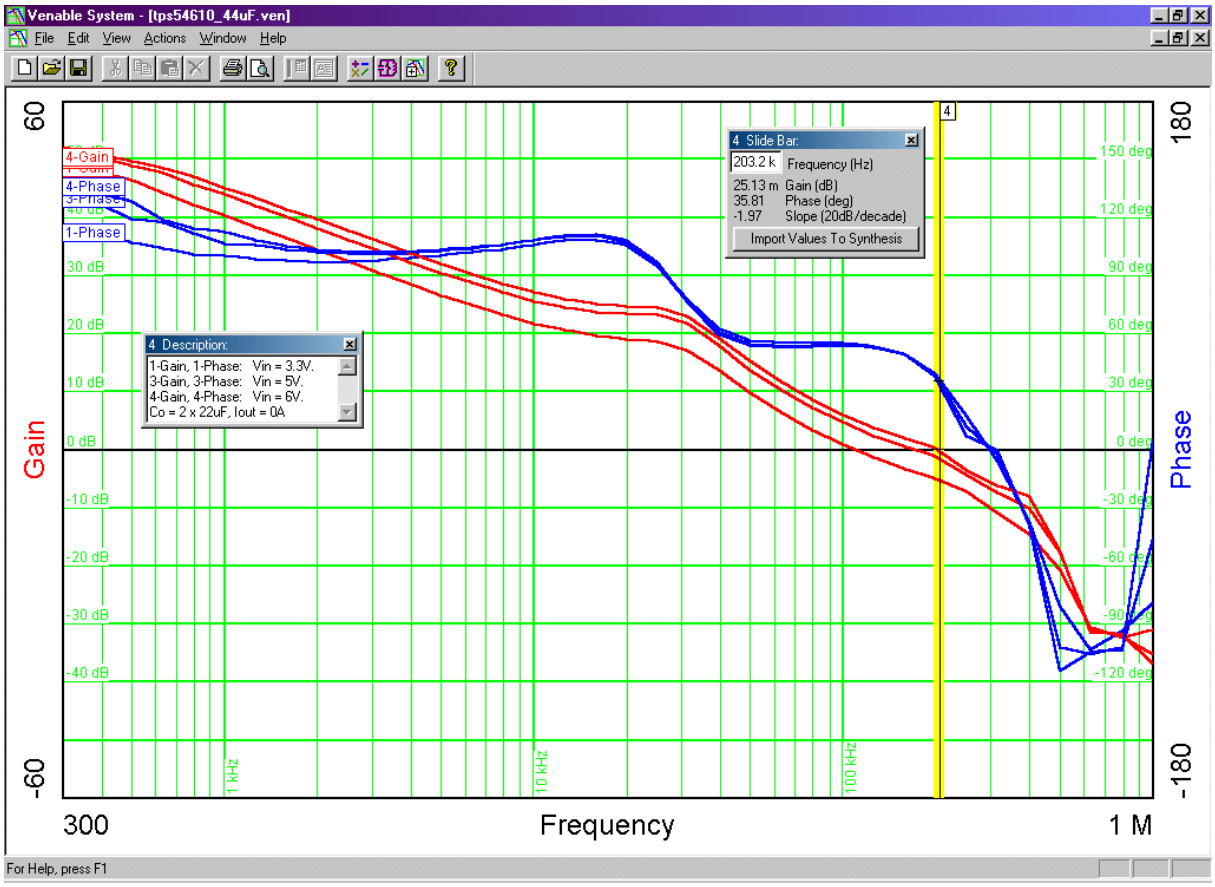


Figure 6. Gain and Phase at No-Load With C_O = 44 µF (33% Less)

Bode plots in Figure 7 show the gain and phase when the output capacitance has been increased 33.3%. That has been done by adding one more 22-µF capacitor to the original three. One can see that the crossover frequency is now 94 kHz, while the phase margin is 51.8 degrees. These two measurements have shown that for the typical tolerance of ±20% for this type of capacitors, the phase-margin is sufficient to avoid unstable condition based on capacitor tolerance. It can be seen that adding ceramic capacitors in parallel to the output capacitor should not lead to the unstable operation. This is because both the corner frequency of L-C output filter and the crossover frequency become lower and there is enough phase margin in the low frequency region. If a user must remove two ceramic output capacitors from the original three, then the regulator can be unstable because the phase margin drops quickly in the high frequency region.

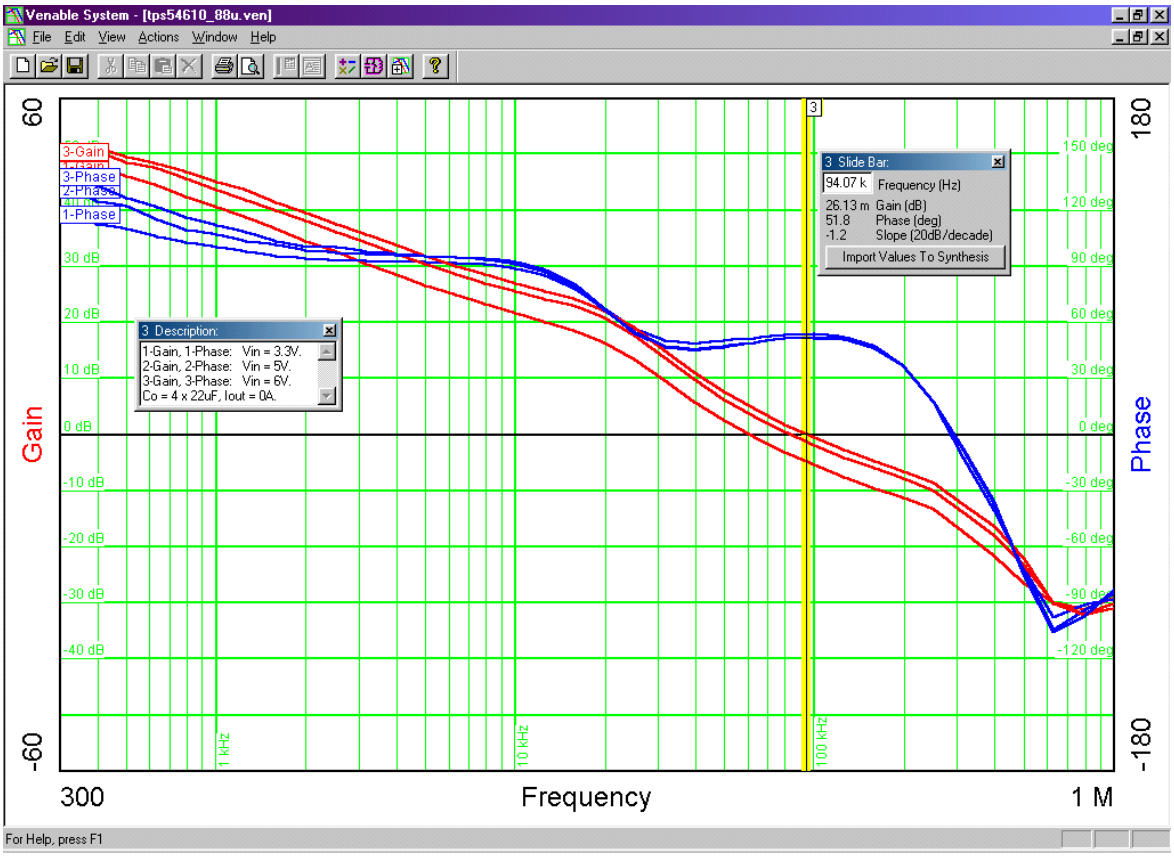
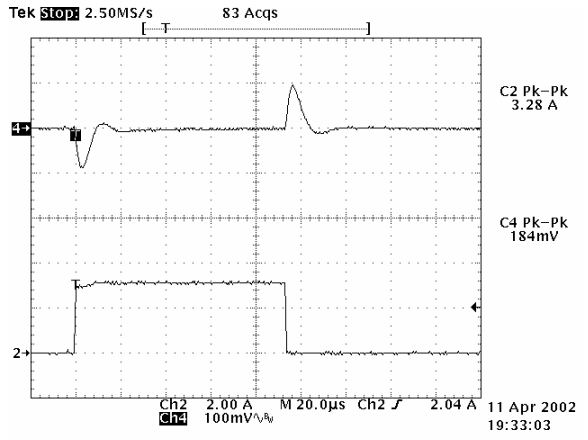


Figure 7. Gain and Phase at No-Load With C_O = 88 µF (33% More)

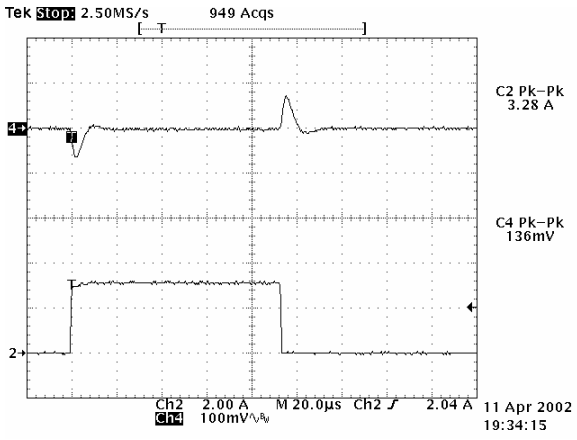
It is worth mentioning that all Bode plots related to the SWIFT™ regulators have relatively high damping characteristics even at no load condition. That means, that the required phase boost provided by the compensation circuit can be less in comparison with the low-damping output filter. This feature makes the selection of compensation circuit for SWIFT™ regulators easier.

5 Load Current Transient Response

The small-signal frequency response measurements, shown in Figure 4 through Figure 7, do not provide the whole picture of adequate gain and phase margin without knowing the circuit behavior at large-signal transient conditions. The low phase margin could cause the excessive ringing during the transient with high peak-to-peak dynamic voltage tolerance. To make sure, that it does not happen, the load current transients have been measured at input voltages 3.3 V and 5 V. These measurements, with 3.4-A current step at about 5 A/µS slew rate, are shown in Figure 8 through Figure 10 for the output capacitance 66 µF, 44 µF and 88 µF respectively. It can be seen from Figure 9, that even with 33% less capacitance and phase margin at about 40 degrees, there is no excessive ringing during the transient. One can see that the peak-to-peak transient is about 30% less at 5-V input voltage versus 3.3-V input. Frequency response has 3.6-dB higher gain, 33% wider bandwidth at the 5-V input versus 3.3-V, and that improves the transient performance. This shows how the high gain and bandwidth could save the number of required output capacitors and meet transient requirements.

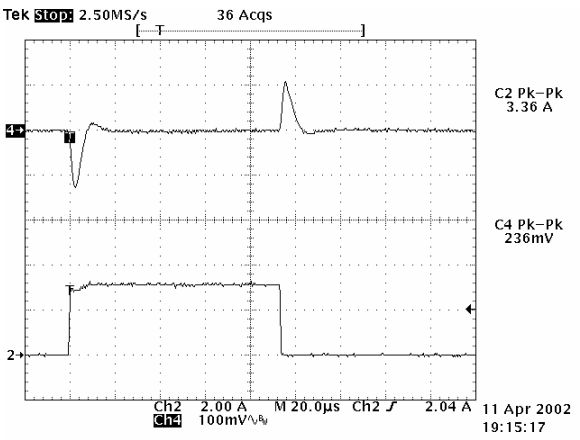


a) 3.3-V input

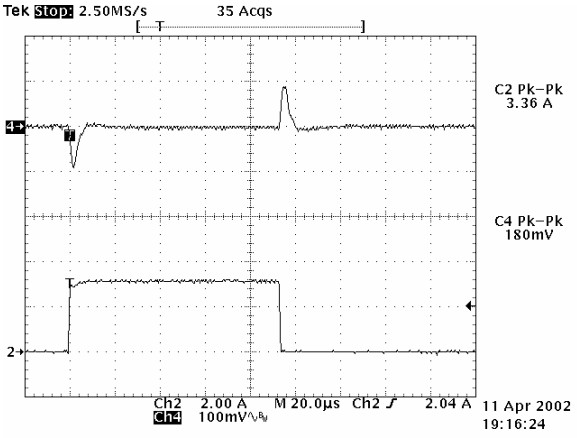


b) 5-V input

Figure 8. Transient Response With 66-µF Output Capacitance

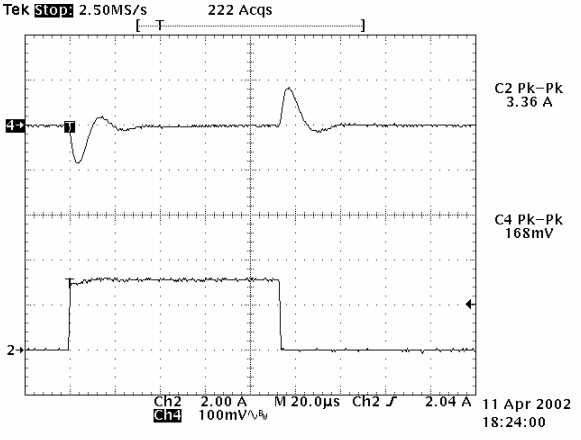


a) 3.3-V input

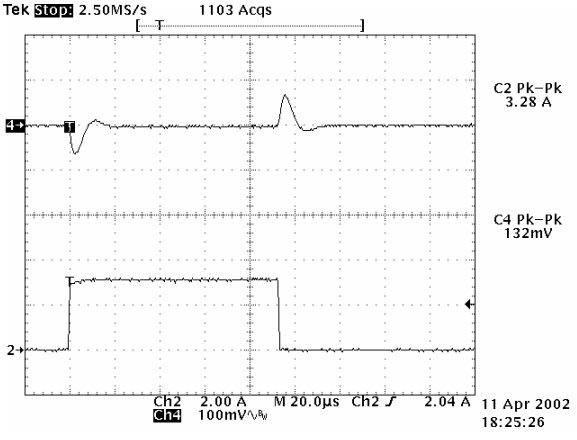


b) 5-V input

Figure 9. Load Transient Response With 44-µF Output Capacitance



a) 3.3-V input



b) 5-V input

Figure 10. Transient Response With 88-µF Output Capacitance

6 Worst Case Analysis

Further worst-case analysis is based on derived analytical model. Related Bode plots, generated using Mathcad, are shown in Figure 11 for the gain and in Figure 12 for phase. The plots are calculated for the input voltage 6 V and output current 7.5 A. The red solid line relates to the nominal values of compensation circuit components R1, R2, R3, C1, C2 and C4. Comparison of analytical curves with the related measured curves, shown in Figure 5, indicates good matching.

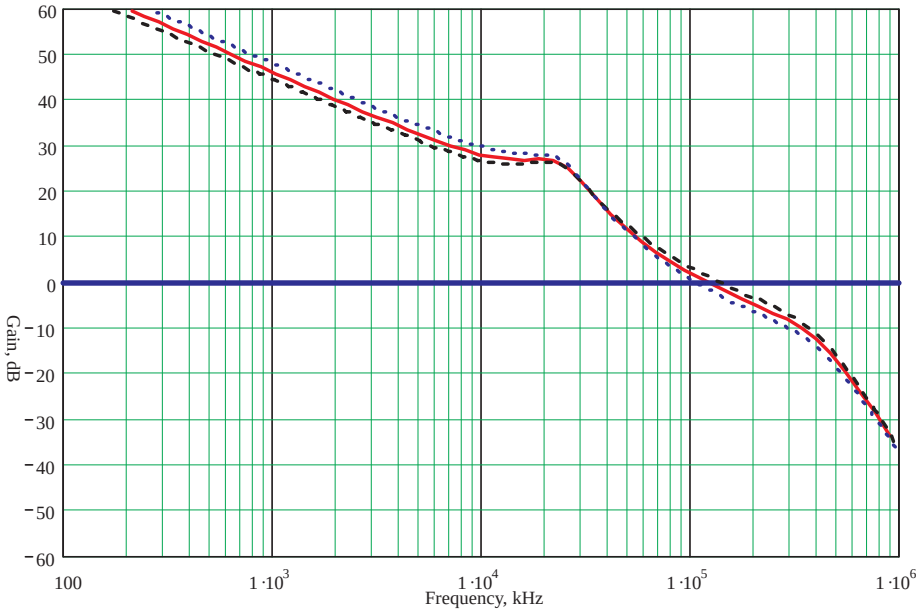


Figure 11. Gain at 6-V Input Including ±20% Variations of Capacitors C1, C2, and C4

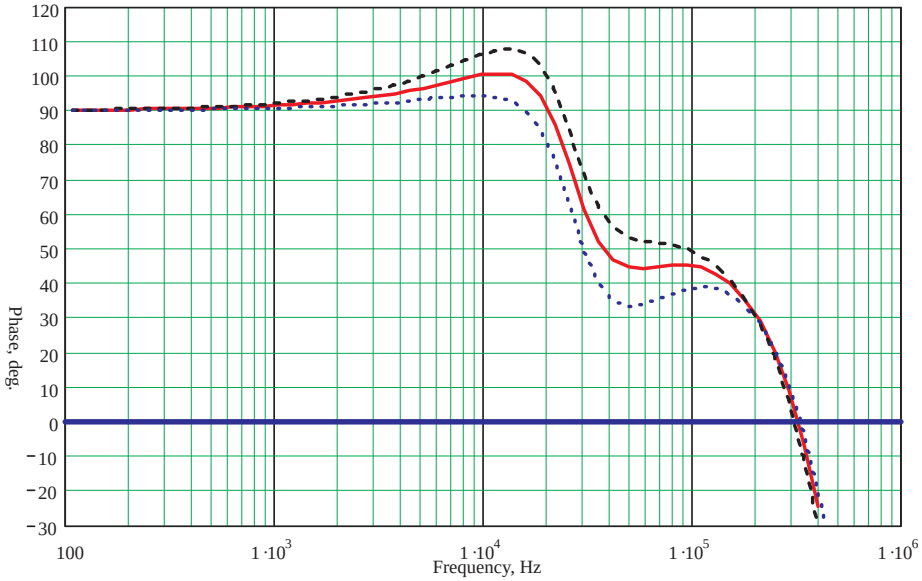
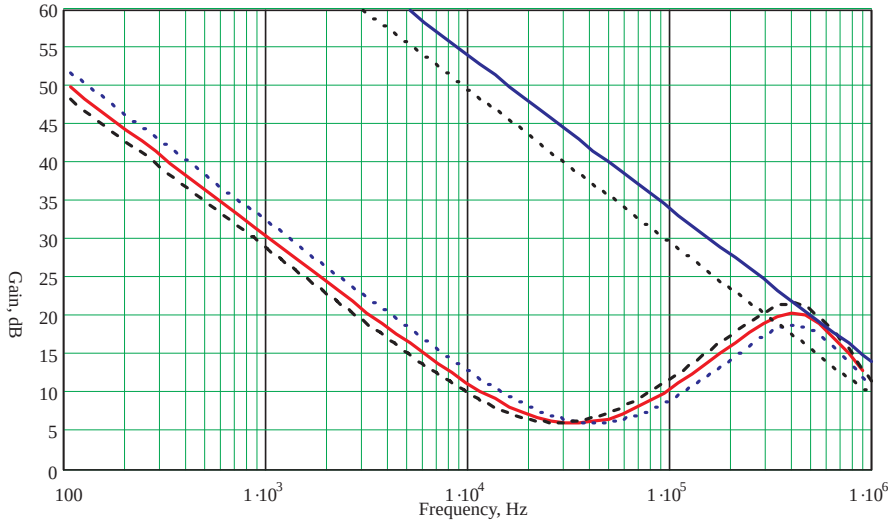


Figure 12. Phase at 6-V Input Including ±20% Variations of Capacitors C1, C2, and C4

After verifying that the theoretical and measured plots match each other, the next step is to analyze the impact of tolerances on stability using the Mathcad software tool. The ±1% tolerance resistors R1, R2 and R3 are low-cost, popular choice. It is assumed in further analysis, that the resistors have overall ±3% tolerance including variation from temperature. The low-cost capacitors usually have tolerance ±20% of their nominal value. The dashed and dotted lines in Figure 11 and Figure 12 show the Bode plots with maximum (dashed black) and minimum (dotted blue) tolerances of capacitors. These curves are for the illustration purposes and they do not include variations of other components. It can be seen that the absolute phase deviation from the nominal is about 10 degrees at frequency 50 kHz and the gain variation is below 2 dB. The phase variation is about 7 degrees for the considered crossover frequency at about 127 kHz and that gives about 38 degrees phase margin.

The impact of error amplifier gain and bandwidth variation is illustrated in Figure 13 and Figure 14.



Dotted and solid lines to the right show minimal and typical envelope of error amplifier

Figure 13. Compensation Circuit Gain Including ±20% Variations of Capacitors C1, C2, and C4

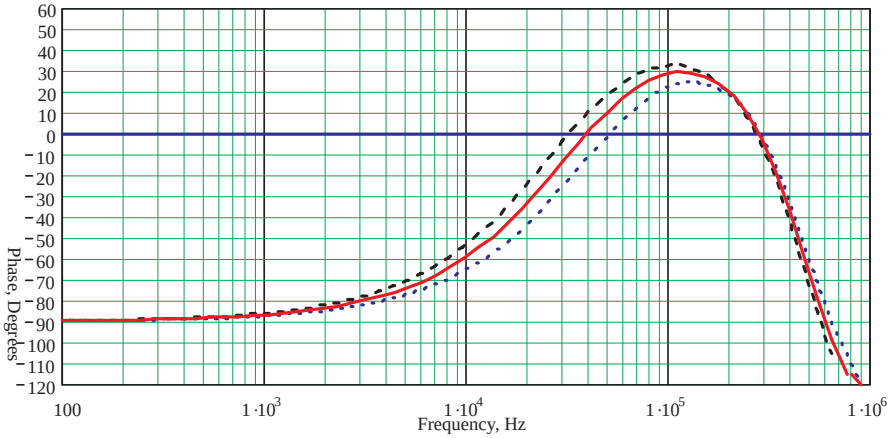


Figure 14. Compensation Circuit Phase Including ±20% Variations of Capacitors C1, C2, and C4

Figure 13 shows the gain of the compensation circuit and Figure 14 shows the phase respectively. The blue solid line to the right side of Figure 13 shows the envelope characteristic of error amplifier that can not be exceeded by compensation circuit. This line corresponds to the typical gain of 110 dB and typical bandwidth of 5 MHz, which is specified by TI's data sheet. The abrupt phase drop at frequency above 200 kHz that can be observed in Figure 4 through Figure 7 is caused by the limited bandwidth of error amplifier. One can see that at frequency 300 kHz the phase drops to zero level. The black dotted line to the right side of Figure 13 shows the envelope characteristic of error amplifier at the worst case condition when the minimum gain is 90 dB and the minimum bandwidth is 3 MHz.

To address the ramp-amplitude variation impact on Bode plots, very simple estimation can be done. The 1-V ramp has tolerance ±10% of its nominal value, so, the gain variation is going to be below 1 dB, cause 20 log(1 V/0.9 V) is about 0.92 dB only. Nevertheless, the gain change, associated with the ramp signal tolerance is included into the following worst case analysis.

7 Two Worst Case Situations

Two worst case situations look obvious observing the phase curves in Figure 12. The first one is based on abrupt phase drop at frequency above 200 kHz associated with the limited bandwidth of error amplifier. The most dangerous condition in this case is if the error amplifier has minimum bandwidth while the overall gain is maximum. This maximum gain and bandwidth relate to the maximum input voltage and to the lowest values of output inductor and capacitor. It can be seen from the Bode plots that this condition compensation circuit can not provide phase boost at frequency above 200 kHz because it is limited by the error amplifier bandwidth.

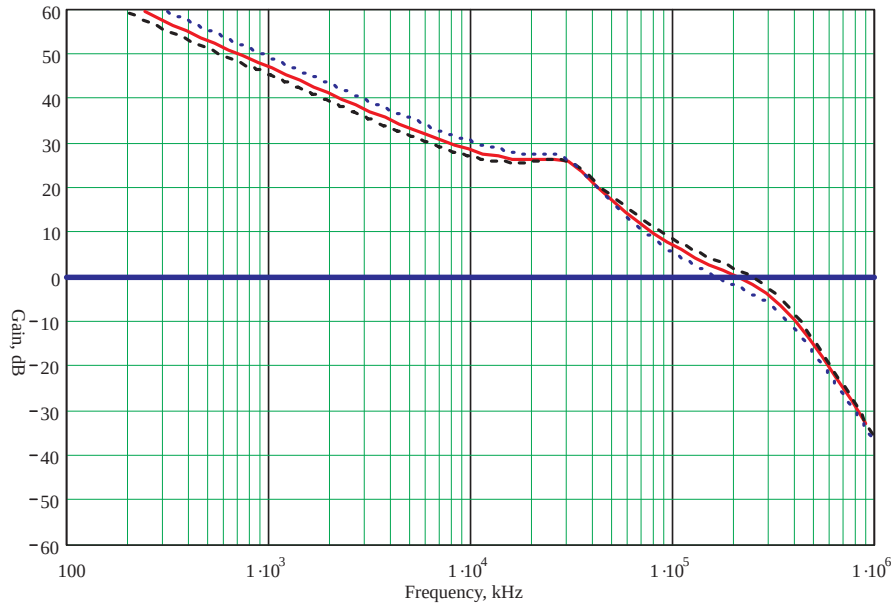
Another worst case condition is if the crossover frequency is about 50 kHz where the local phase drop is possible depending on tolerances of compensation circuit. For this condition, the gain is minimal. If the additional phase boost is necessary in this region, it can be done by proper selection of compensation circuit C1, C2, C4, R1, R2, R3.

Table 2 shows the worst case tolerances of all involved variables for these two conditions. It should be mentioned that the possibility that 14 different variables have worst case condition is very low. All variables are ranked depending on their impact on the frequency response variation. The lowest number means the highest impact. This estimation is valid only for this particular situation. The minimum load current (or high load resistance) has been selected as the worst case for both conditions because of the highest phase shift, associated with second order L-C output filter at light load.

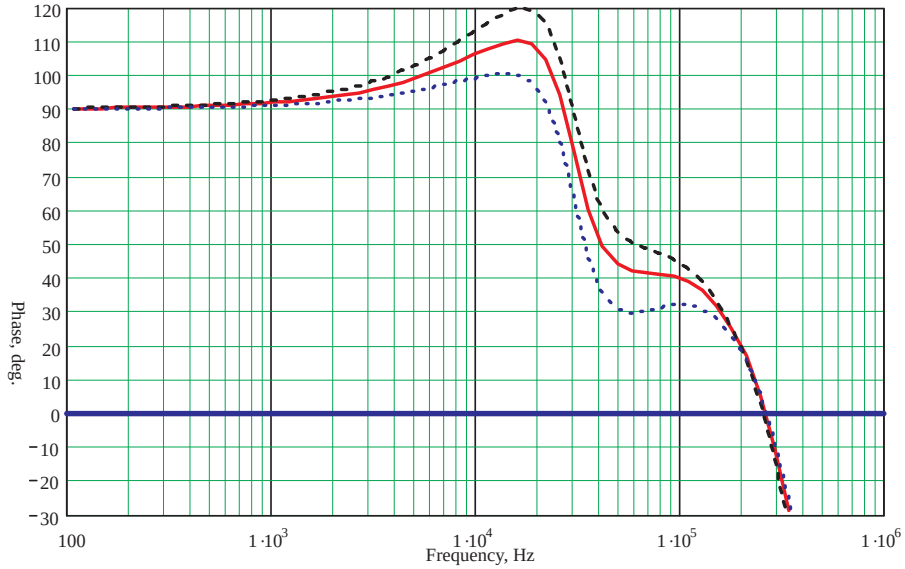
Table 2. Worst Case Tolerances for the Two Extreme Conditions

COMPONENT	RANK	CONDITION 1: MAXIMUM GAIN	CONDITION 2: MINIMUM GAIN
Input voltage	2	6 V	3 V
Load current	3	Minimum	Minimum
Error amplifier bandwidth	2	3 MHz	3 MHz
Ramp signal	4	−10%	+10%
Output ind. L1	1	−20%	+20%
Output capacitor C5, C7, C8	1	−20%	+20%
Compensation C1, C2, C4	2	±20%	±20%
Compensation R1, R2, R3	3	±1% (±3% over temperature)	±1% (±3% over temperature)

The worst case Bode plots, calculated using these assumptions, are shown in Figs. 15 and 17.



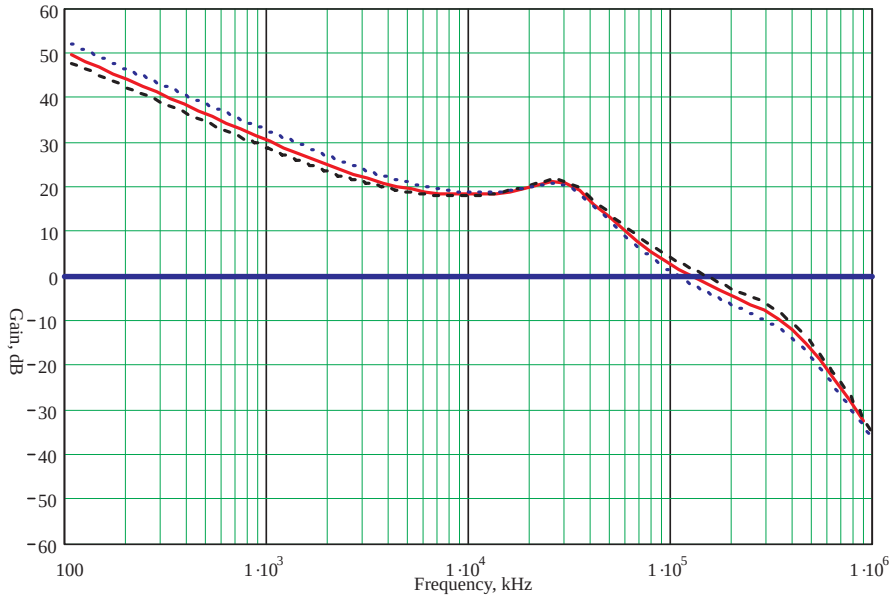
a) Gain



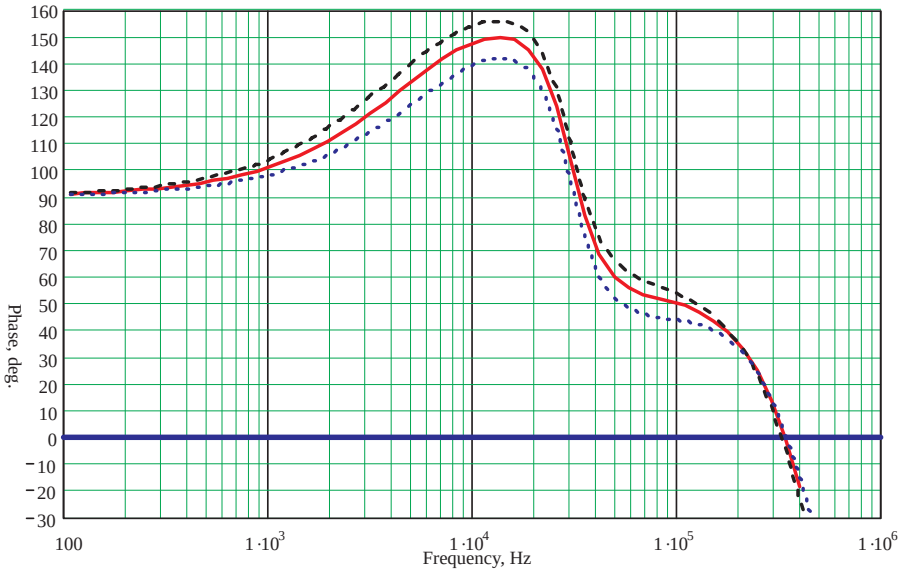
b) Phase

Figure 15. Worst Case Condition 1 in Accordance With Table 2

One can see that the worst case condition 1 results in an unstable operation. The worst case condition 2 is stable, but the phase margin is only about 18 degrees. The compensation can be designed to provide enough margin even for these two extreme conditions where the possibility, that all tolerances of 14 different variables are in the worst case, is very low. The higher phase margin for condition 1 can be provided by decreasing the capacitance of C1 from 470 pF to 270 pF. The condition 2 can be addressed by increasing the capacitance of C4 from 470 pF to 3300 pF. The worst case conditions 1 and 2 with the modified capacitors C1 and C4 are shown in Figure 16 and Figure 18 respectively. One can see that for the condition 1 phase margin is about 43 degrees (Figure 16) and for the condition 2 it is about 38 degrees (Figure 18).

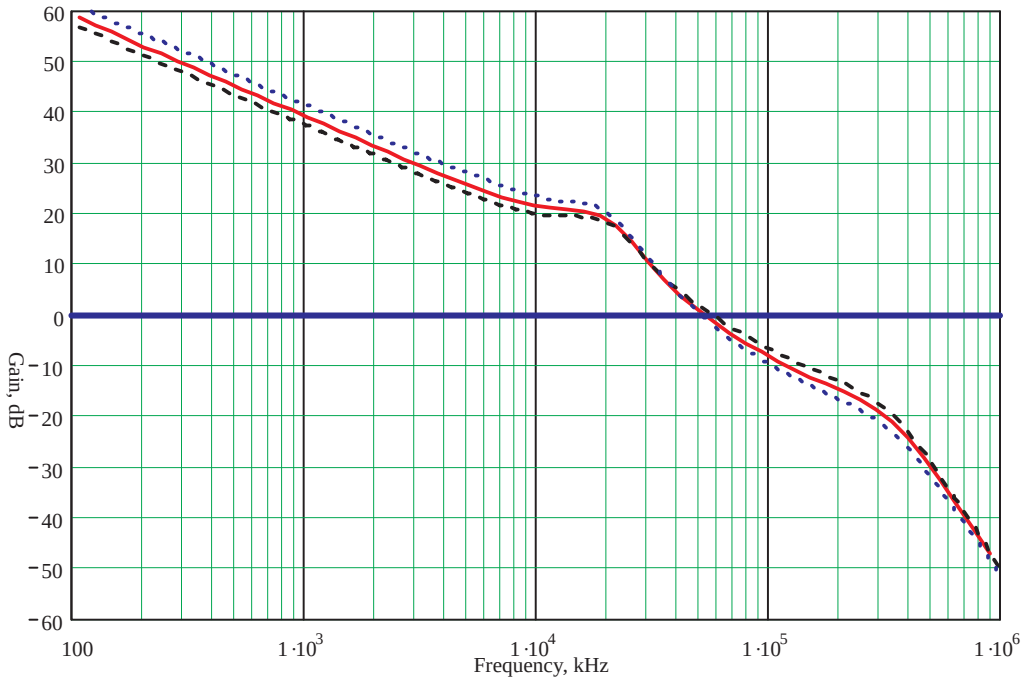


a) Gain

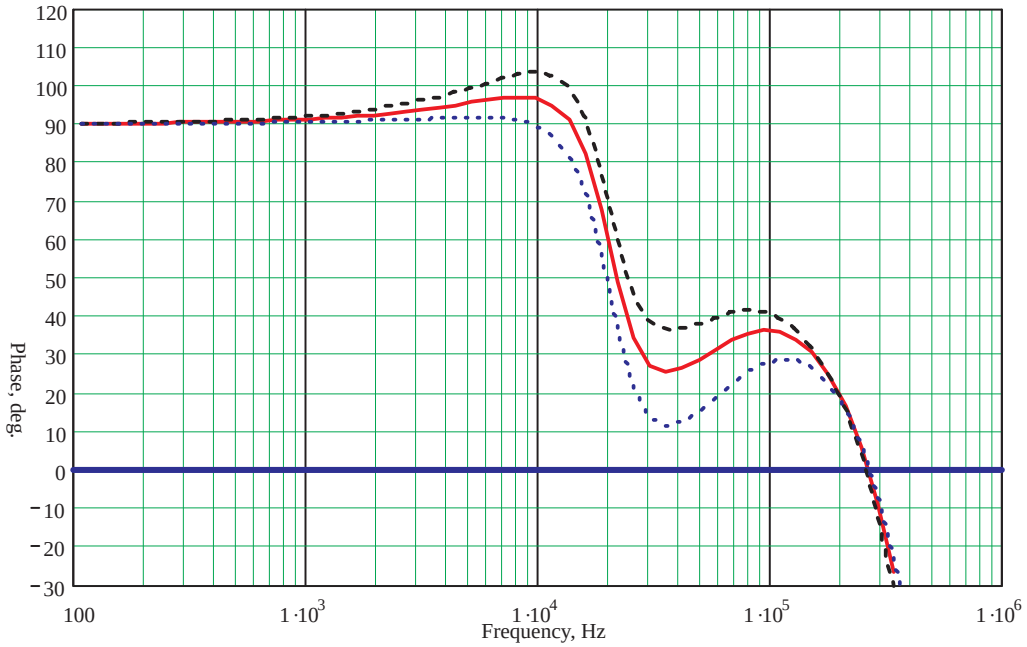


b) Phase

Figure 16. Worst Case Condition 1 With Modified Compensation (C1 = 270 pF, C4 = 3300 pF)

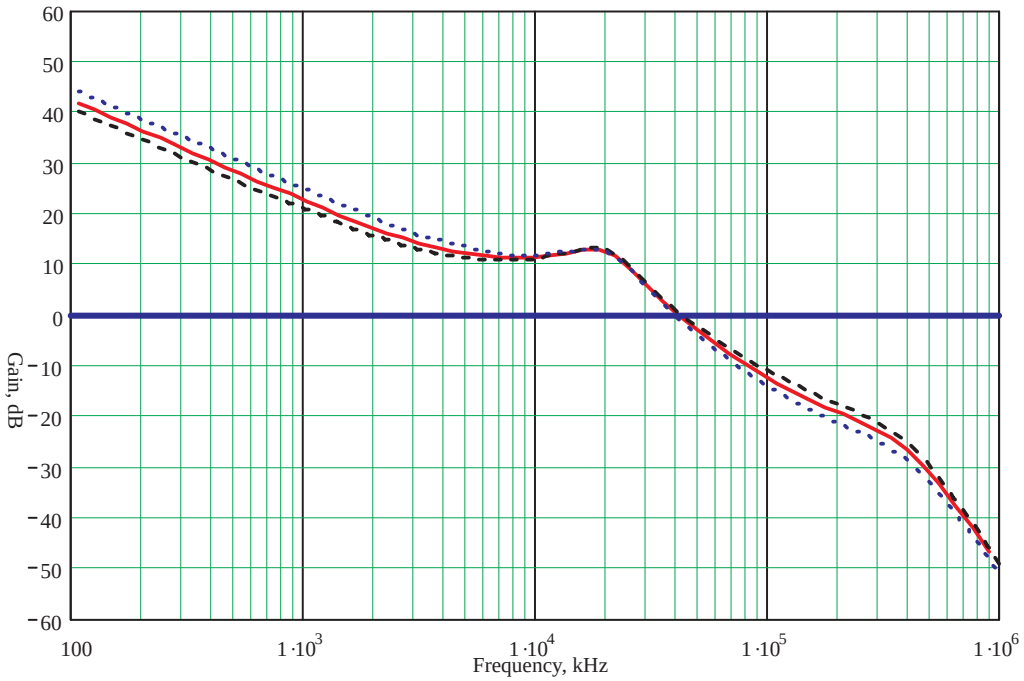


a) Gain

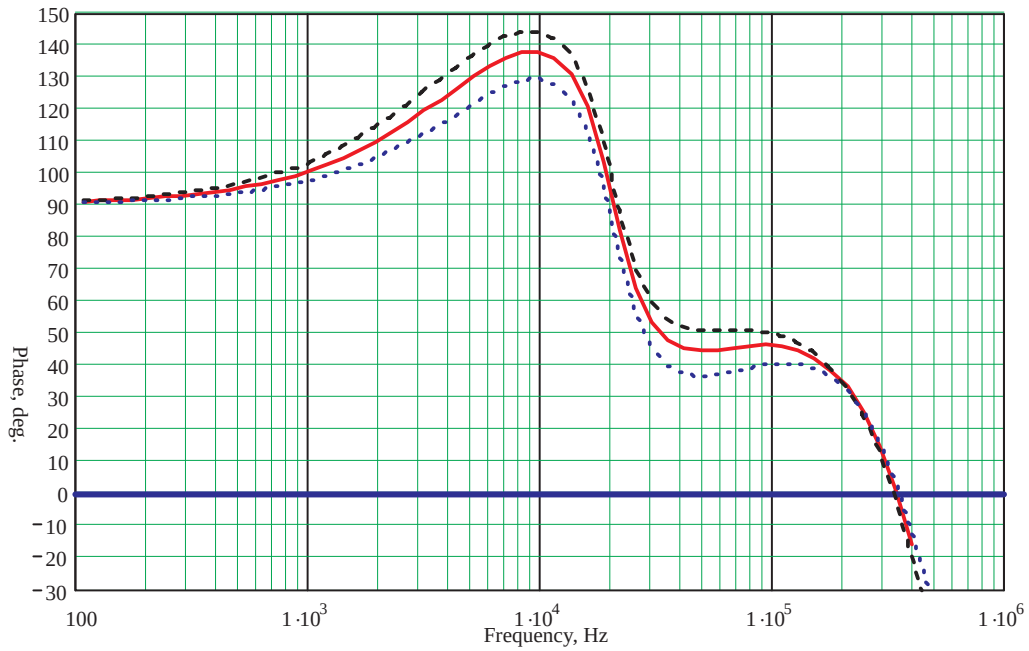


b) Phase

Figure 17. Worst Case Condition 2 in Accordance With Table 1



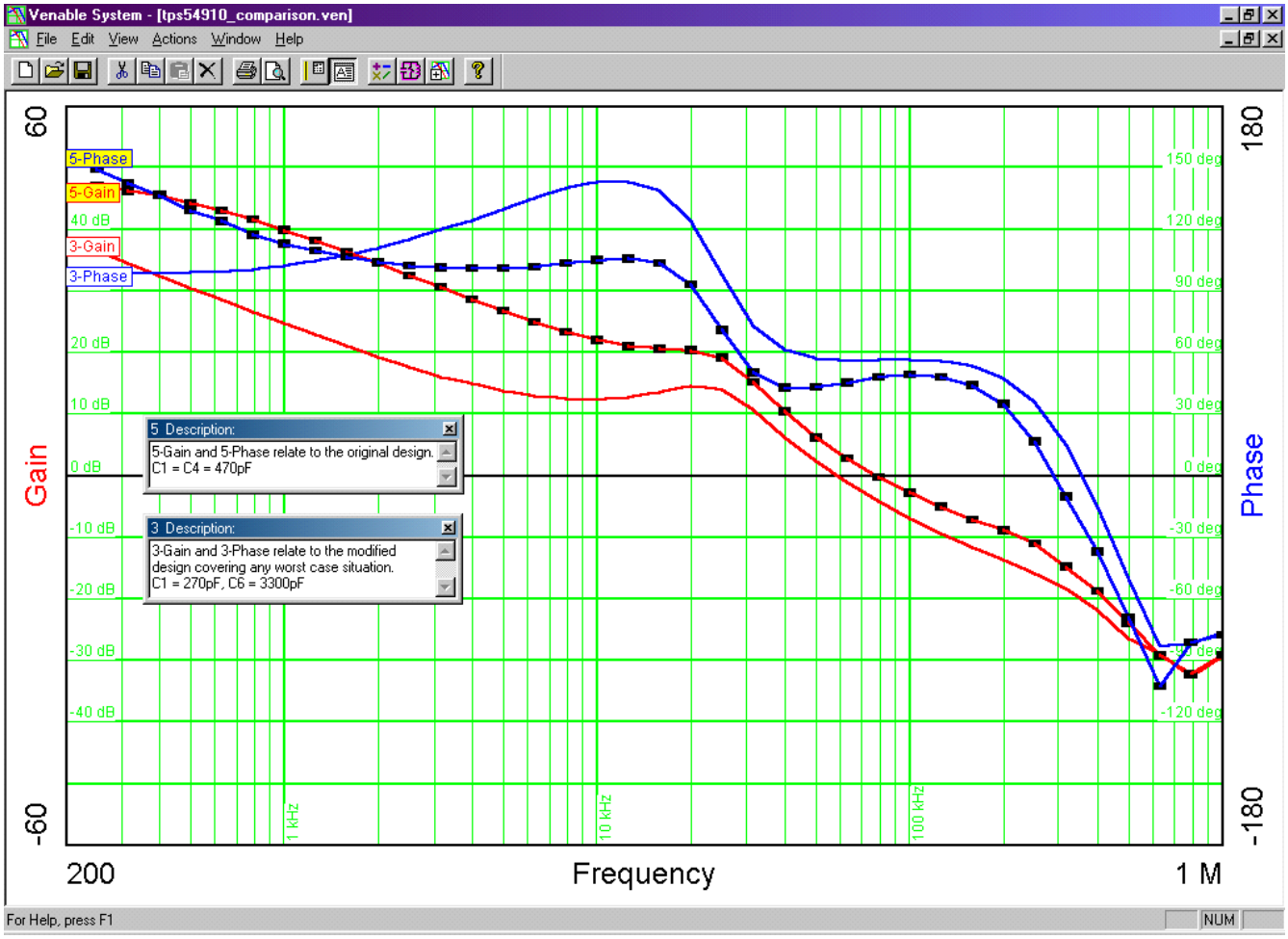
a) Gain



b) Phase

Figure 18. Worst Case Condition 2 With Modified Compensation (C1 = 270 pF, C4 = 3300 pF)

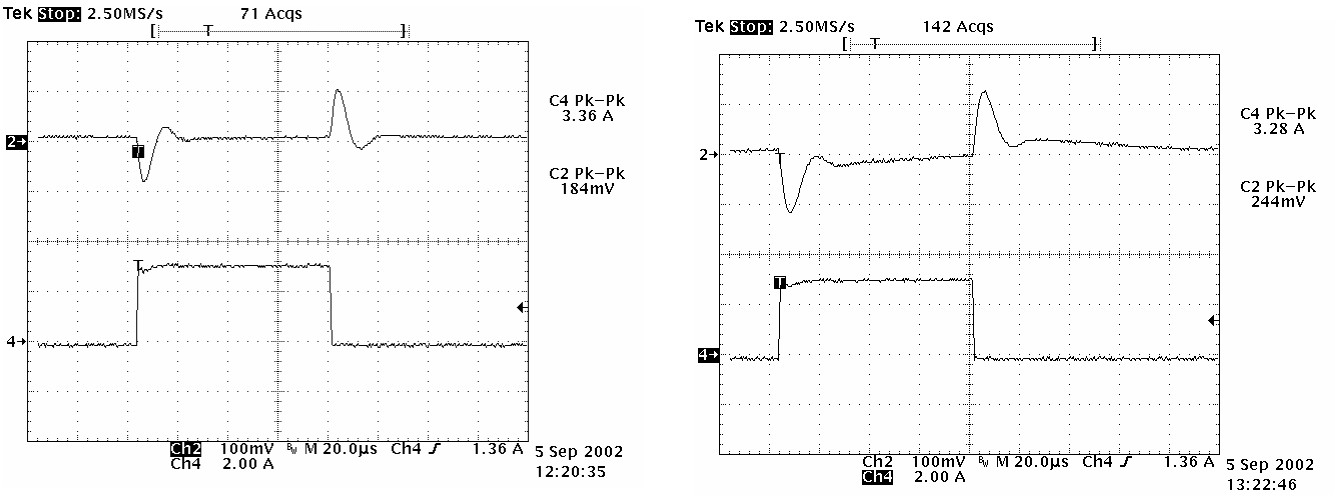
Measured Bode plots of the original design and the modified one are shown in Figure 19. The measurements are fulfilled at input voltage 3.3 V and no-load condition. The modified design provides lower bandwidth and gain and, as a result, worth transient response characteristics in comparison with the original design. It can be seen, that because of lower gain the modified design reaches the error amplifier envelope at the higher frequency, so the phase drops to zero at about 370 kHz versus previous 300 kHz.



For the original compensation C1 = C4 = 470 pF, for the modified compensation C1 = 270 pF, C4 = 3300 pF

Figure 19. Bode Plots of the Original (Marked by Rectangular) and Modified Compensation Circuit

One can see that the frequency response of modified regulator has the crossover frequency 60 kHz versus 80 kHz of the original design. The gain of the modified design is 15 dB lower than the original design. The waveforms in Figure 20 show how these changes impact on transient response.



a) Original compensation circuit **b) Modified conservative compensation circuit**

Figure 20. Transient Response With the Original (a) and Modified (b) Compensation Circuit

One can see that the peak-to-peak transient response of modified design is 244 mV versus 184 mV of the original one. This is a 33% increase. The transient of modified design lasts much longer, over 100 µs, versus 20 µs that it was originally. To provide the same peak-to-peak transient response for the modified design, the extra output capacitors and associated cost needs to be added.

8 Conclusion

Experimental measurements and worst-case analysis have been fulfilled to show the impact of parameter variations on stability of SWIFT™ regulators with ceramic output capacitors. Two worst-case conditions, covering 14 different variations of parameters, have been considered and analyzed.

Analysis shows, that the compensation circuit design covering any worst-case condition is possible. However, this design may not be optimal in terms of transient response and cost of output filter. The possibility of 14 different parameters having worst case tolerances has to be weighted before selecting more or less conservative approach to design the compensation circuit.

In general, modern ceramic capacitors with X5R and X7R dielectrics require less phase and gain margin versus electrolytic type of capacitors because of less parameter variations. Ceramic capacitors significantly decrease the size and cost of the output filter because of their low ripple. The voltage-mode control SWIFT™ regulators with ceramic capacitors provide low ripple, good transient response solution at minimum output filter cost, thus, successfully matching current-mode controllers in this application area.

9 References

1. *TPS54610, 3-V to 6-V Input, 6-A Output Synchronous Buck PWM Switcher With Integrated FETs (SWIFT™) (SLVS398)*
2. *User's Guide: TPS54610EVM-213 6-Amp, TPS54810EVM-213 8-Amp, TPS54910EVM-213 9Amp (SLVU071)*
3. *R. Miftakhutdinov, Designing for Small-Size, High-Frequency Applications With SWIFT™ Family of Synchronous Buck Regulators (SLVA107)*

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