Using the TPS767D325 LDO Regulator

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ABSTRACT

The new dual low-drop-out (LDO) regulators on the TPS767D325 are custom designed to supply the latest DSP core and I/O system supply voltages. But the LDO regulators on this IC meet more than their new voltage requirements; specifically, they enable faster supply current transient capability. This family of LDO's also includes the TPS767D318 and TPS767D301.

This new family of 2-A regulators also achieves improved regulation using sense amplifiers for more accurate voltage correction. The design provides for a laboratory-like remote sense connection within the IC.

Power sequencing, just as important as bus or serial timing, is provided to turn on and off the micro's core and I/O to specification. This device does not have an integrated sequencing control circuit.

Power on reset is integrated onboard for both core and I/O supplies to provide a clean 200-ms delay reset.

Finally, the use of higher integration processes allows lower *Rds(on)* and thus cooler operation in its power pass output transistors.

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1 Design Problem

1.1 Short Latency Transient Current Periods

The TPS767D3xx family of dual-voltage regulators offers very fast current response time when designed with the appropriate components. Processor power requirements include very high transient currents that must be considered in the initial design. A design that uses higher-valued output capacitors to handle the large transient currents provides the solution. In addition, the metal layout of low impedance conductors from the regulator to the processor supply pins is suggested to lower series induced transients even further.

1.2 Power Sequencing of Separate Core and I/O Voltages

For increased reliability of the DSP, voltage sequencing of the I/O voltage and core voltages is recommended. The C549 and C5410 DSPs recommend powering up the I/O first and then the core and powering down the core first and then I/O, or powering up and powering down simultaneously. The power-up and power-down sequencing is opposite for other C5000 DSPs.

1.3 Dual Open Drain Power On Reset Timing

Open drains are needed to allow the setting of the upper voltage level of the micro. These could be at the 1.5-V to 3.3-V level. This correct upper voltage would then satisfy the timing needed by providing the t_{PHL} and t_{PLH} edges. The correct levels and timing then would be correctly defined for the proper reset signal.

2 Solution

2.1 Characteristic of a Dual Voltage Design and Performance of Current Transients

Figure 1 shows the TPS767D325 configured to power the VC549 using diodes to clamp the core and I/O voltages for protection. Darker schematic lines indicate the need for wider copper traces on the circuit board. These lower resistances are for less parasitic inductances.

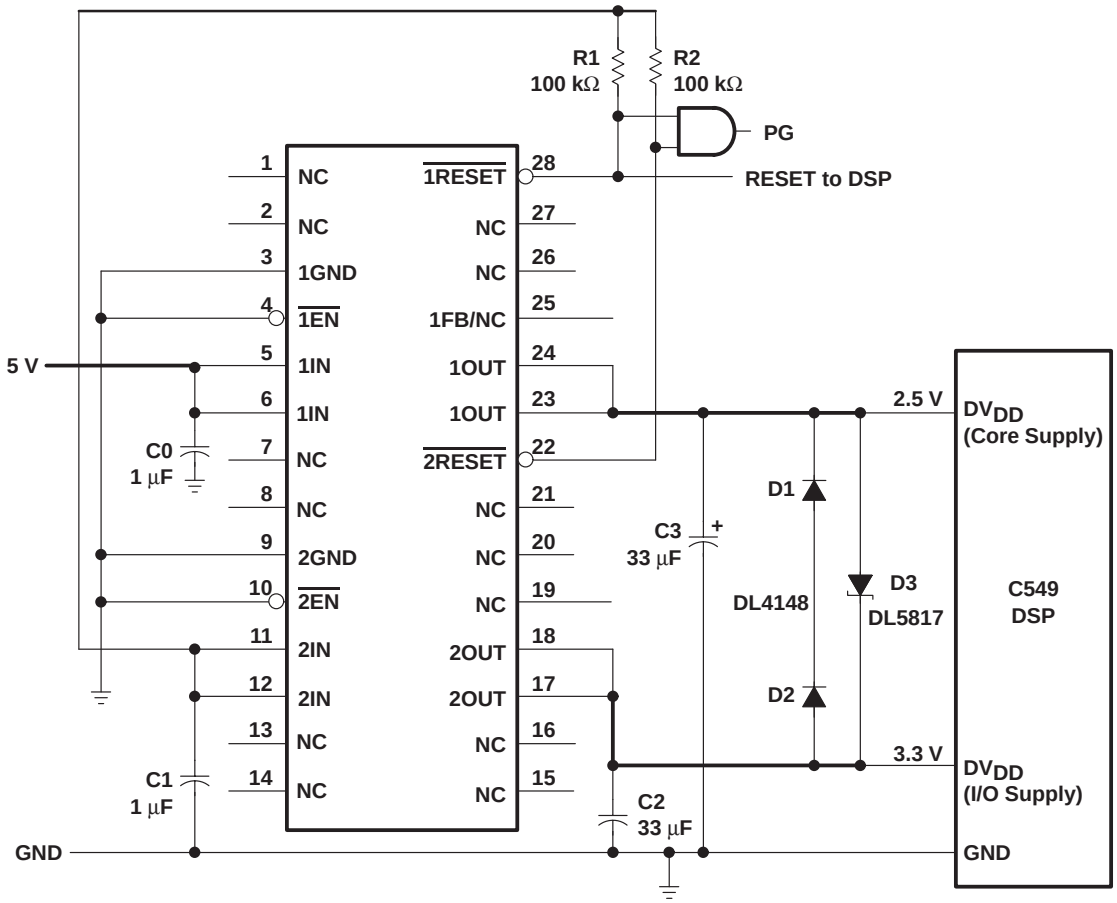

Figure 1. Typical Application Circuit Showing the Suggested Lower Impedance/Wider Copper Supply Lines and Diode Protection

2.2 The Best Case ESR Capacitors for C2 and C3 in This Circuit

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS767D325 is located more than a few inches from the power source. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS767D3xx requires an output capacitor for stability. A low ESR 33-μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range. Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD336M035R0300 and the Sprague 593D336X0035D2W work well because the maximum ESR at 25°C is 300 mΩ. Due to the reduced stability range available when using output capacitors smaller than 10 μF, capacitors in this range are not recommended. Larger capacitors provide a wider range of stability and better load transient response. For fast transient response, the low ESR is a requirement.

Figures 2 and 3 show response times of the load transient and line transients that typify the controlling regulation of the dual regulator.

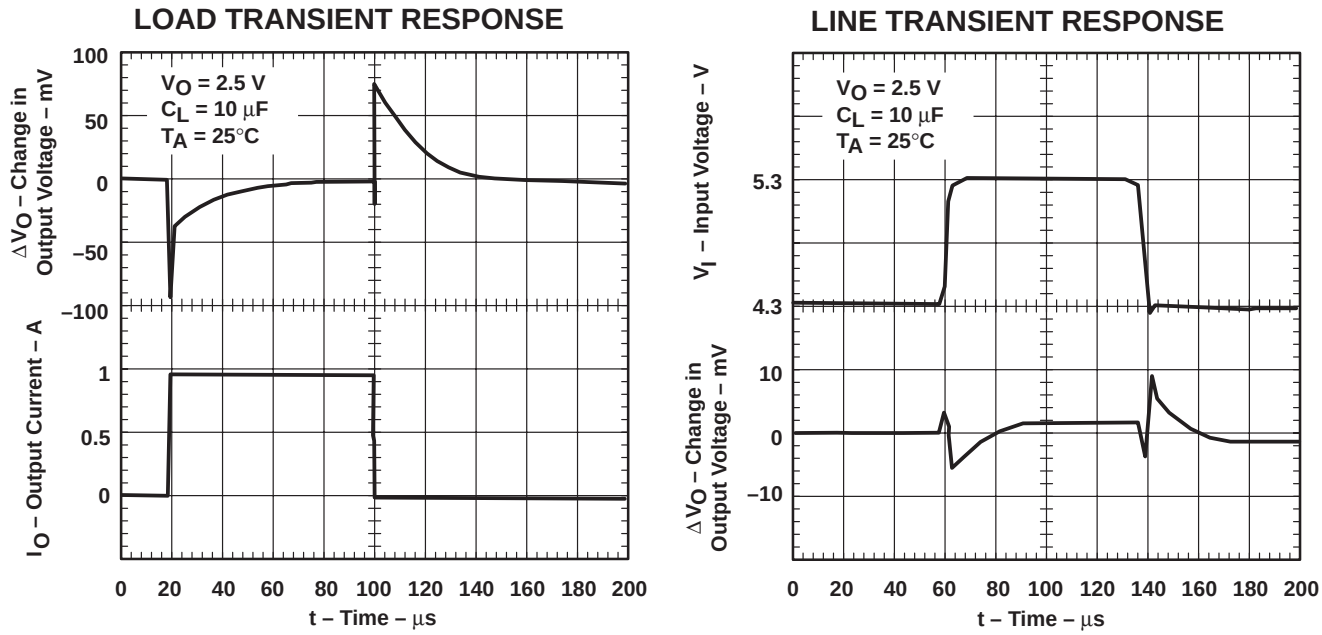

Figure 2. Graphics of Typical Current Transient Response of the 2.5-V Supply Output

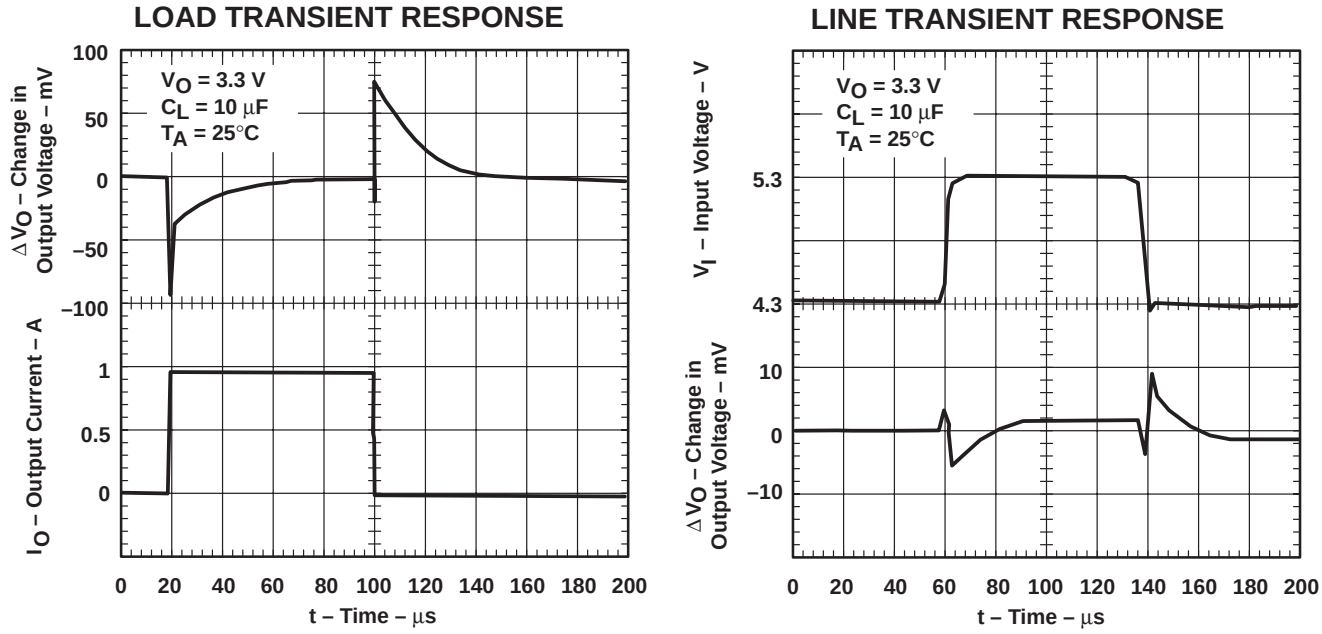

Figure 3. Graphics of Typical Current Transient Response of the 3.3-V Supply Output

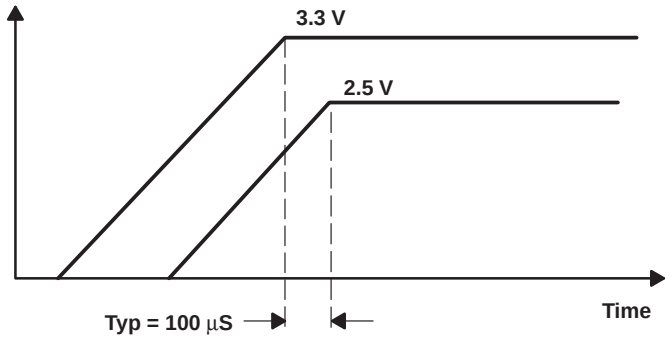

Figure 4. Suggested Power Supply Sequencing of the Core Voltage of 2.5 V and the I/O Voltage of 3.3 V

3 Summary

The TPS767D325 clearly demonstrates the next level of linear power supply control achievable with improved techniques and precision circuitry. High performance coupled with the need for simplicity and low cost have further refined the fast transient conversion process.

4 Reference

1. TI data sheet, *TPS767D301/318/325 DuaL-Output Low-Dropout Voltage Regulator*, literature number SLVS209.

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