Understanding the Terms and Definitions of LDO Voltage Regulators

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ABSTRACT

This report provides an understanding of the terms and definitions of low dropout (LDO) voltage regulators, and describes fundamental concepts including dropout voltage, quiescent current, standby current, efficiency, transient response, line/load regulation, power supply rejection, output noise voltage, accuracy, and power dissipation. Each section includes an example to increase the understandability.

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1 Dropout Voltage

Dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage. Figure 1 shows a typical LDO regulator circuit. In the dropout region, the PMOS pass element is simply a resistor, and dropout is expressed in terms of its on-resistance (R_{on}).

$$V_{dropout} = I_o R_{on} \quad (1)$$

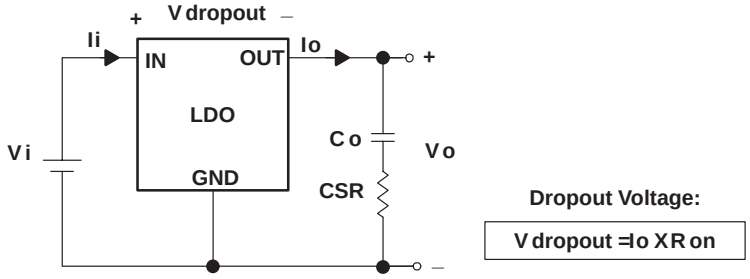

Figure 1. Typical Application Circuit of LDO Regulator

For example, Figure 2 shows the input/output characteristics of the TPS76733 3.3-V LDO regulator. The dropout voltage of the TPS76733 is typically 350 mV at 1 A. Thus, the LDO regulator begins dropping out at 3.65-V input voltage; the range of the dropout region is between approximately 2-V and 3.65V input voltage. Below this, the device is nonfunctional. Low dropout voltage is necessary to maximize the regulator efficiency.

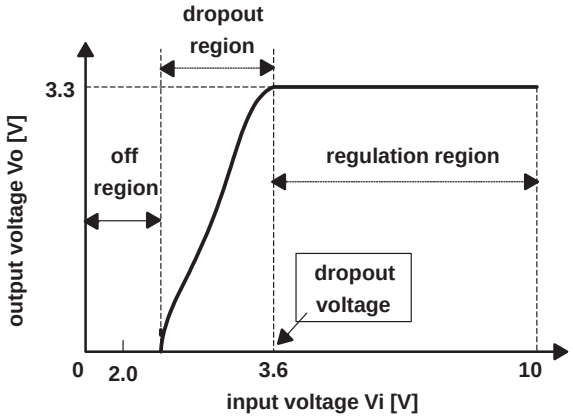

Figure 2. Dropout Region of TPS76733 (3.3 V LDO)

2 Quiescent Current

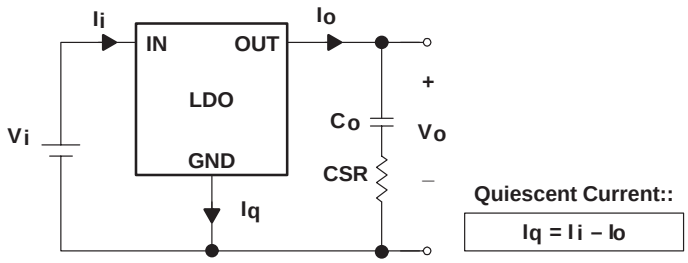

Figure 3. Quiescent Current of LDO Regulator

Quiescent, or ground current, is the difference between input and output currents. Low quiescent current is necessary to maximize the current efficiency. Figure 3 shows the quiescent current that is defined by

$$I_q = I_i - I_o \quad (2)$$

Quiescent current consists of bias current (such as band-gap reference, sampling resistor, and error amplifier currents) and the gate drive current of the series pass element, which do not contribute to output power. The value of quiescent current is mostly determined by the series pass element, topologies, ambient temperature, etc.

For bipolar transistors, the quiescent current increases proportionally with the output current, because the series pass element is a current-driven device. In addition, in the dropout region the quiescent current can increase due to the additional parasitic current path between the emitter and the base of the bipolar transistor, which is caused by a lower base voltage than that of the output voltage. For MOS transistors, the quiescent current has a near constant value with respect to the load current since the device is a voltage-driven device. The only things that contribute to the quiescent current for MOS transistors are the biasing currents of band–gap, sampling resistor, and error amplifier. In applications where power consumption is critical, or where small bias current is needed in comparison with the output current, an LDO voltage regulator using MOS transistors is essential.

3 Standby Current

Standby current is the input current drawn by a regulator when the output voltage is disabled by a shutdown signal. The reference and the error amplifier in an LDO regulator are not loaded during the standby mode, as shown in Figure 4.

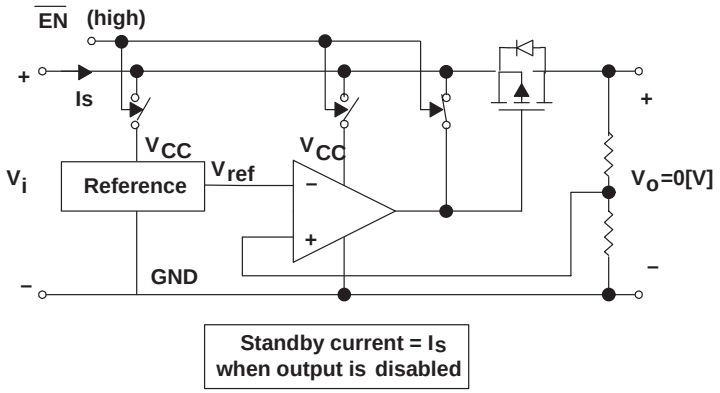

Figure 4. Standby Current of LDO Regulator

4 Efficiency

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows.

$$\text{Efficiency} = \frac{I_o V_o}{\left(I_o + I_q\right) V_i} \times 100 \tag{3}$$

To have a high efficiency, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized, since the power dissipation of LDO regulators accounts for the efficiency. (Power Dissipation = $(V_i - V_o)I_o$). The input/output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions.

Example:

1. What is the efficiency of the TPS76933 3.3-V LDO regulator with the following operating conditions? Input voltage range is 3.6 V to 4.5 V. Output current range is 80 mA to 100 mA. The maximum quiescent current is 17 μA. Then, the minimum efficiency is obtained as follows:

$$\text{Efficiency} = \frac{100\ \text{mA} \cdot 3.3\ \text{V}}{(100\ \text{mA} + 17\ \mu\text{A}) 4.5\ \text{V}} \times 100 = 73.3\ \%$$

2. What is the efficiency if input voltage range is 3.6 V to 4 V under the same conditions as the above? The minimum efficiency is improved as follows:

$$\text{Efficiency} = \frac{100\ \text{mA} \cdot 3.3\ \text{V}}{(100\ \text{mA} + 17\ \mu\text{A}) 4\ \text{V}} \times 100 = 82.5\ \%$$

5 Transient Response

The transient response is the maximum allowable output voltage variation for a load current step change. The transient response is a function of the output capacitor value (C_o), the equivalent series resistance (ESR) of the output capacitor, the bypass capacitor (C_b) that is usually added to the output capacitor to improve the load transient response, and the maximum load-current ($I_{o,max}$). The maximum transient voltage variation is defined as follows:

$$\Delta V_{tr,max} = \frac{I_{o,max}}{C_o + C_b}\Delta t_1 + \Delta V_{ESR} \quad (4)$$

Where Δt_1 corresponds to the closed loop bandwidth of an LDO regulator. ΔV_{ESR} is the voltage variation resulting from the presence of the ESR (R_{ESR}) of the output capacitor. The application determines how low this value should be.

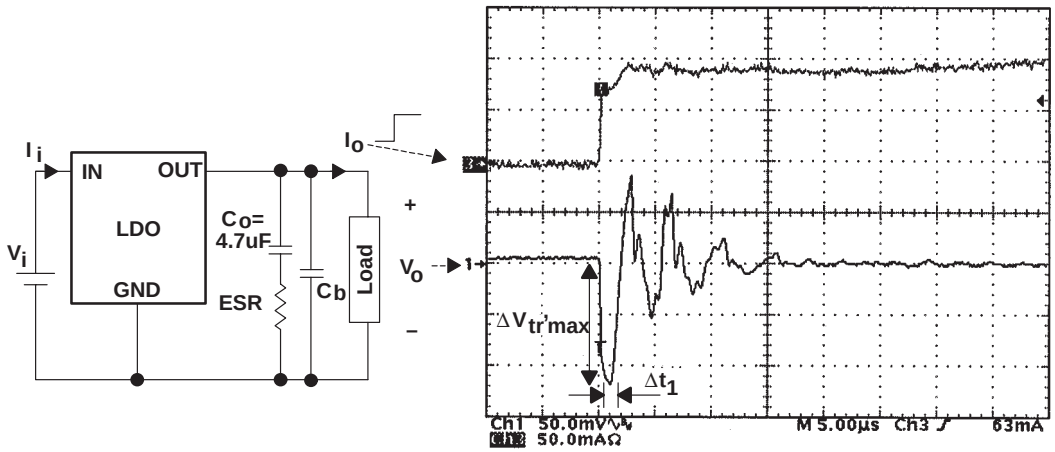

Figure 5. Transient Response of 1.2-V, 100 mA LDO Regulator

Figure 5 shows the transient response of a 1.2–V, 100-mA LDO regulator with an output capacitor of 4.7 µF. A step change of load current (near 90 mA) was applied to the regulator, which is shown in the upper trace of the figure. In the lower trace the output voltage drops approximately 120 mV and then the voltage control loop of the LDO regulator begins to respond to the step load change within 1 us (Δt_1 = 1 µs). The frequency bandwidth of the LDO regulator accounts for Δt_1. Finally, the output voltage reaches a stable state within 17 µs.

To obtain a better transient response, a higher bandwidth of the LDO regulator, higher values of output/bypass capacitors, and low ESR values are recommended, provided they meet the CSR requirements.

6 Line Regulation

Line regulation is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta V_i} \quad (5)$$

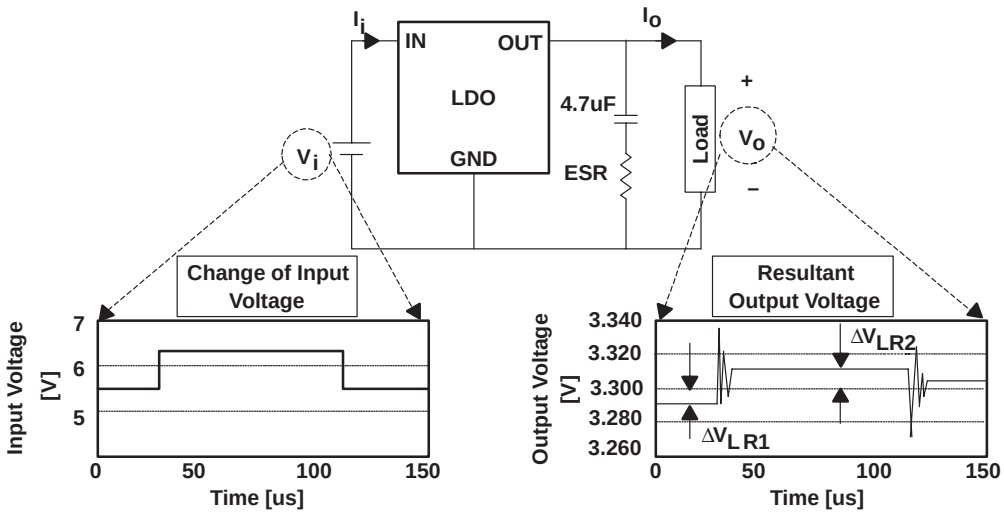

Figure 6. Line Transient Response of TPS76933

Figure 6 shows the input voltage transient response of the TPS76933 3.3-V LDO regulator. A step change of input voltage was applied to the regulator, which is shown at the lower left in the figure. The resultant output voltage has been changed due to the different input voltages as shown in the right side of the figure. The line regulation is determined by ΔV_{LR1} and ΔV_{LR2} since line regulation is a steady-state parameter (i.e., all frequency components are neglected). Figure 7 shows the circuit performance of the TPS76933 LDO regulator with respect to the input voltages. The broken line shows the range of the output voltage variation (ΔV_{LR}) resulting from the input voltage change. Increasing open loop gain improves the line regulation.

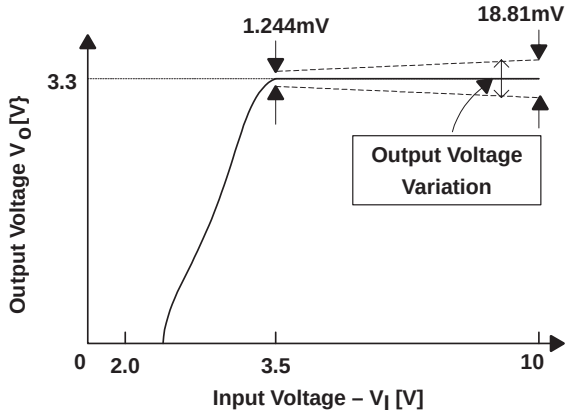

Figure 7. TPS76933 Output Voltage With Respect to the Input Voltages

7 Load Regulation

Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions. Load regulation is defined as

$$\text{Load regulation; } \frac{\Delta V_O}{\Delta I_O} \tag{6}$$

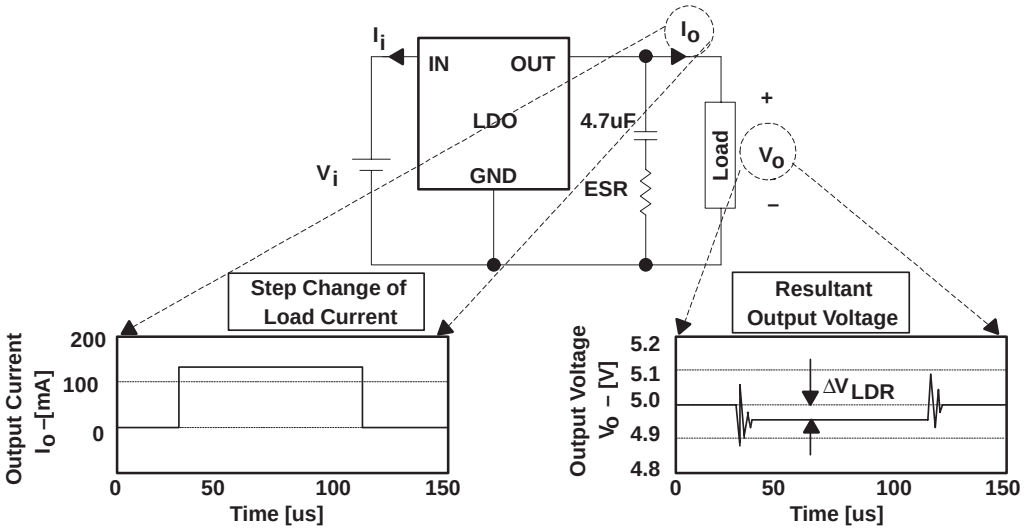

Figure 8. Load Transient Response of TPS76350

The worst case of the output voltage variations occurs as the load current transitions from zero to its maximum rated value or vice versa, which is illustrated in Figure 8. The load regulation is determined by the ΔV_{LDR} since load regulation is a steady-state parameter like the line regulation. Figure 9 shows the circuit performance of the TPS76350 5-V LDO regulator with respect to the output currents. Increasing open loop gain improves the load regulation.

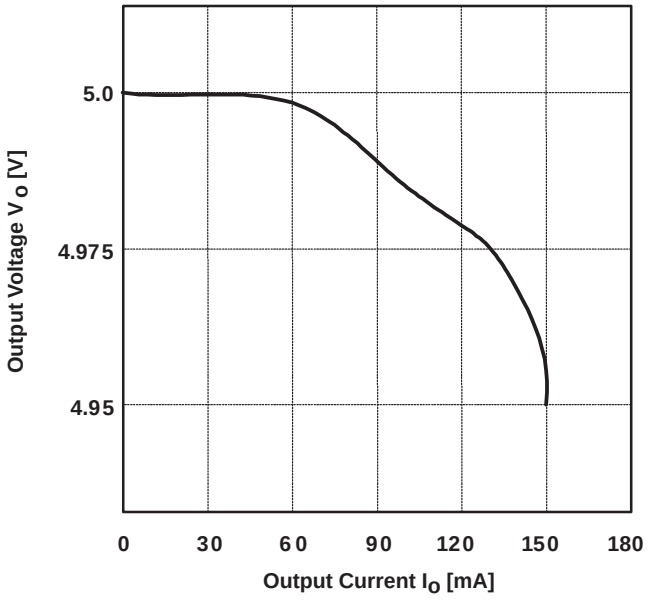

Figure 9. TPS76350 LDO Regulator Output Voltage With Respect to Output Currents

8 Power Supply Rejection

Power supply rejection ratio (PSRR), also known as ripple rejection, measures the LDO regulator's ability to prevent the regulated output voltage fluctuating caused by input voltage variations. The same relation for line regulation applies to PSRR except that the whole frequency spectrum is considered.

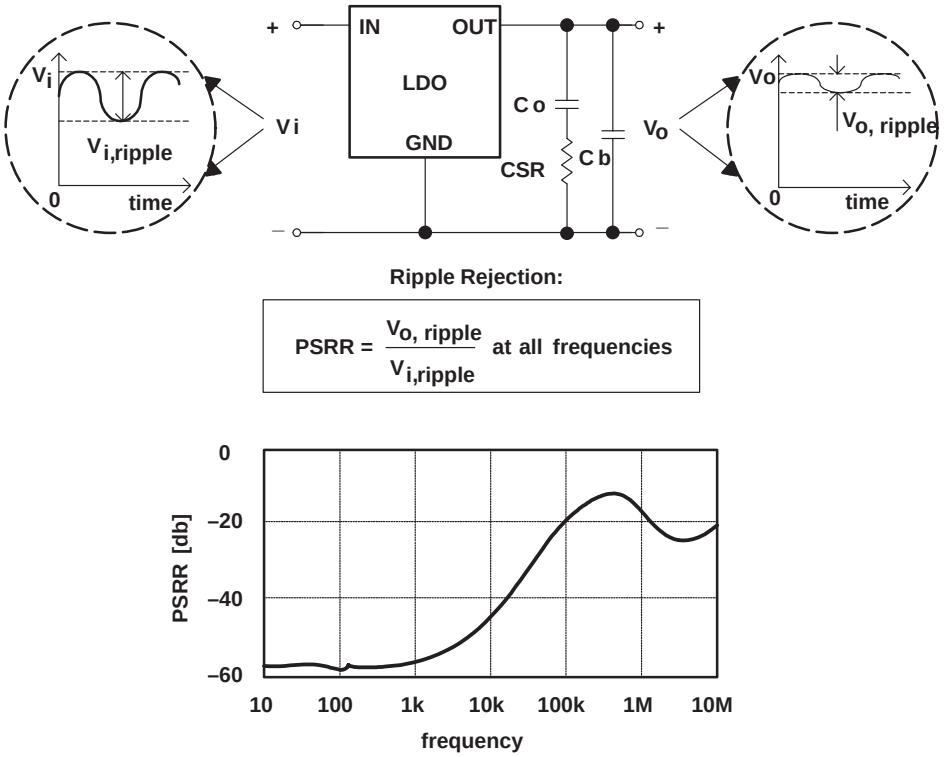

Figure 10. Power Supply Rejection

The ripple rejection is defined by

$$\text{PSRR} = \frac{V_{o,ripple}}{V_{i,ripple}} \text{ at all frequencies} \quad (7)$$

For example, supply rejection in the frequency band between 100 kHz and 1 MHz is especially important in applications where the output of a dc/dc switch mode power supply (SMPS) is used to power the linear regulator. The output ripple of the SMPS is typically in the aforementioned frequency span. Thus, the figure above does not seem to show a good PSRR performance for the SMPS applications over the frequency range (100 kHz to 1 MHz). The worst performance (maximum point in the graph) occurs when R_{ESR} is large and C_b is low.

The control loop tends to be the dominant contributor of supply rejection. Low ESR value, a large output capacitor, and added bypass capacitors improve the PSRR performance, provided they meet the CSR requirement.

9 Output Noise Voltage

Output noise voltage is the RMS output noise voltage over a given range of frequencies (10 Hz to 100 kHz) under the conditions of a constant output current and a ripple-free input voltage. The noise generated only by an LDO regulator becomes the output noise voltage.

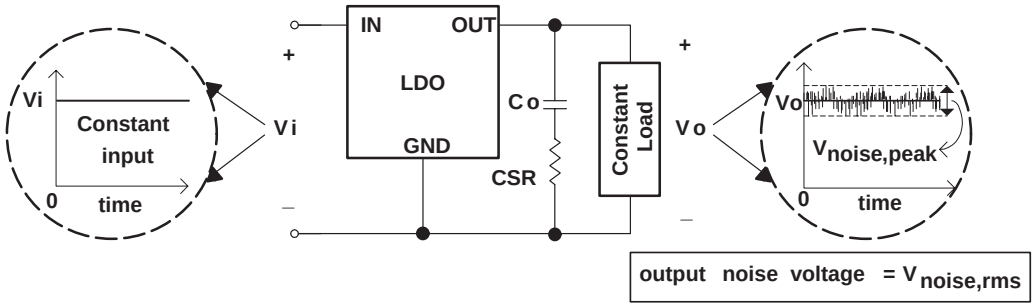

Figure 11. Output Noise Voltage

Most output noise is caused by the internal voltage reference. Typical specification of output noise voltage ranges from 100 to 500 μV. TI-TPS764xx devices have an external compensation pin to enable customers to connect a bypass capacitor to reduce the output noise. A bypass capacitor, in conjunction with an internal resistor, creates a low-pass filter to further reduce the noise. TI-TPS764xx exhibits only 50 μV of output voltage noise using 0.01 μF bypass and 4.7 μF output capacitors.

10 Instability of LDO Regulator

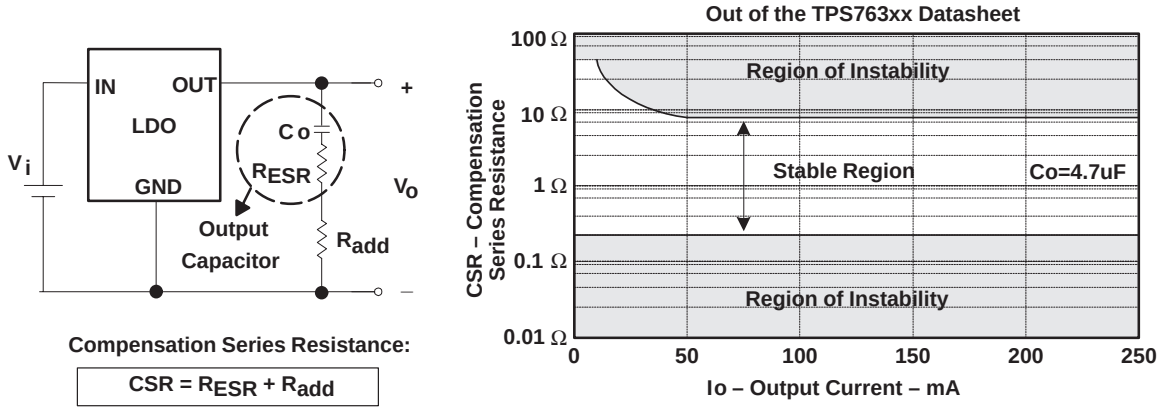

Figure 12. Stable Range of CSR

LDO manufacturers typically provide a graph showing the stable range of the compensation series resistance (CSR) values, since CSR can cause instability with respect to output currents. The CSR is the sum of the equivalent series resistance (R_{ESR}) of the output capacitance and the additional resistor (R_{add}).

$$CSR = R_{ESR} + R_{add} \tag{8}$$

An additional resistor can be used if the R_{ESR} is too small. An example of a typical stable range of CSR values is shown in Figure 12. This curve is called *tunnel of death*. The curve shows that CSR must be between 0.2 Ω and 9 Ω so that the LDO regulator is stable. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the CSR requirements.

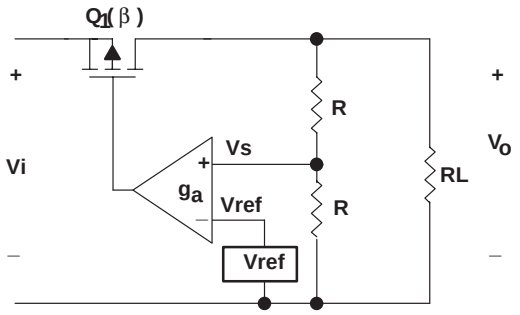

Figure 13. LDO Regulator

11 Accuracy

The overall accuracy considers the effects of line regulation (ΔV_{LR}), load regulation (ΔV_{LDR}), reference voltage drift ($\Delta V_{o,ref}$), error amplifier voltage drift ($\Delta V_{o,a}$), external sampling resistor tolerance ($\Delta V_{o,r}$), and temperature coefficient (ΔV_{TC}). It is defined by

$$\text{Accuracy} \approx \frac{|\Delta V_{LR}| + |\Delta V_{LDR}| + \sqrt{\Delta V_{o,ref}^2 + \Delta V_{o,a}^2 + \Delta V_{o,r}^2 + \Delta V_{TC}^2}}{V_o} \times 100 \qquad (9)$$

The output voltage variation in a regulated power supply is due primarily to temperature variation of the constant voltage reference source and temperature variation of the difference amplifier characteristics, as well as the sampling resistor tolerance. Load regulation, line regulation, gain error, and offsets normally account for 1 to 3% of the overall accuracy.

Example:

What is the total accuracy of the 3.3 V LDO regulator shown in Figure 13 over the temperature span from 0° to 125° with the following operating characteristics; temperature coefficient is 100 ppm/°C, sampling resistor tolerance is 0.25%, output voltage change resulting from load regulation and line regulation are ±5 mV, and ±10 mV, respectively. The accuracy of the reference is 1%.

The output voltage is given by

$$V_o = \frac{R + R}{R} V_{ref} = 2V_{ref}$$

Therefore, the reference voltage V_{ref} is half of the output voltage (i.e., V_{ref} = 3.3/2[V]), and

$$\Delta V_{TC} = \text{Temperature Coefficient} \cdot \left(T_{max} - T_{min}\right) \cdot V_o$$

$$= (100\text{ppm}/°\text{C})(125°\text{C})(3.3\text{ V}) = 41.2\text{ mV}$$

$$\Delta V_{o,r} = \left(0.25\%\text{ of } V_o + 0.25\%\text{ of } V_o\right)V_{ref}$$

$$= (0.005)(3.3)\left(\frac{3.3}{2}\right) = 27\text{ mV}$$

$$\Delta V_{o,ref} = \frac{2R}{R} V_d = 2\left(\frac{3.3}{2}\right)0.01 = 33\text{mV}, \text{ where } V_d = V_{ref} \times 0.01 = \left(\frac{3.3}{2}\right) \times 0.01$$

Therefore, the overall accuracy of the LDO is obtained as follows:

$$\text{Accuracy} \approx \frac{10\text{mV} + 5\text{mV} + \sqrt{(33\text{mV})^2 + (27\text{mV})^2 + (41.2\text{mV})^2}}{3.3\ \text{V}} \times 100 \approx 2.25\%$$

12 Power Dissipation and Junction Temperature

Most LDO regulators specify a junction temperature to assure their operations; the maximum junction temperature allowable without damaging the device is also specified. This restriction limits the power dissipation that the regulator can handle in any given application. To ensure that the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$. The maximum power dissipation limit is determined using the following equation;

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \tag{10}$$

Where

T_{Jmax} is the maximum allowable junction temperature.
$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 285°C/W for the 5-terminal SOT23.
T_A is the ambient temperature.

The regulator power dissipation is calculated using;

$$P_D = \left(V_i - V_o\right) \times I_o \tag{11}$$

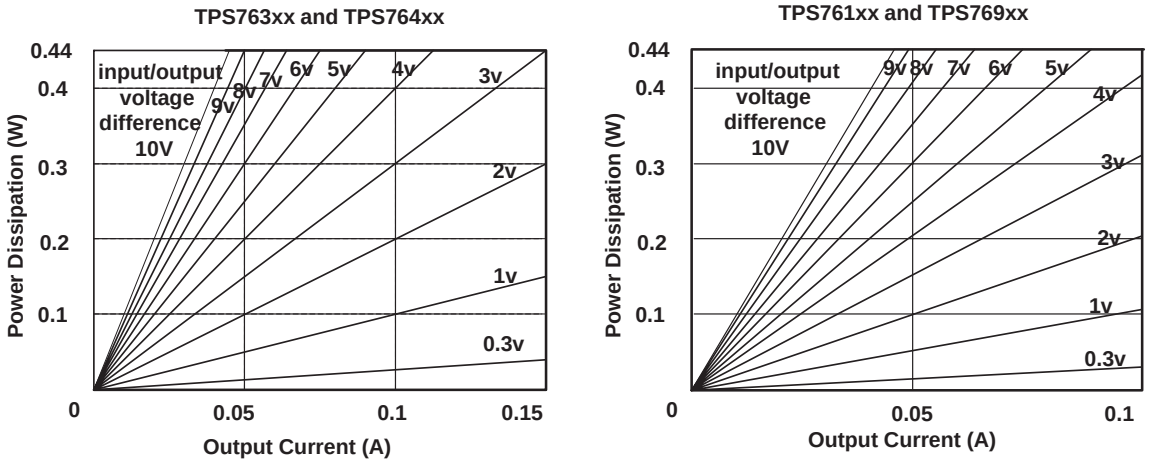

Figure 14. Power Dissipation vs Output Current

Figure 14 shows the safe operating area for several TI LDO regulators in terms of output current, input/output voltage difference, and dissipation power, which are calculated by using equation (11). Calculate maximum power dissipation $P_{D(max)}$ by using equation (10). The calculated $P_{D(max)}$ must not exceed the safe area shown in the figures. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately to 140°C, where regulator operation resumes.

13 Summary

This application report described the terms and definitions of low dropout (LDO) voltage regulators, and provided fundamental concepts.

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