

Power Supply Sequencing Solutions for Dual Supply Voltage DSPs

Mixed Signal Products

ABSTRACT

This application report describes power-supply sequencing recommendations and techniques applicable to dual supply voltage DSPs in TI's TMS320C2000, TMS320C5000 and TMS320C6000 families. These techniques take advantage of the reset, power good, enable and soft-start features available on TI Power Management Products, including low drop out regulators, switching power supply controllers, supply voltage supervisors, and power distribution switches.

Contents

1	Introduction	3
1.1	Core and I/O Sequencing Requirements	3
1.2	Completing the Power-Up and Power-Down Operations in a Timely Manner	4
1.3	Sequencing the Core and I/O to Avoid System-Level Bus Contention	5
2	Core and I/O Supply Sequencing Options	6
2.1	Sequencing Solutions With 3.3 V Only Available	6
2.1.1	P-Channel MOSFET and DC/DC Supply With Power Good	6
2.1.2	P-Channel MOSFET and Single SVS	7
2.1.3	Power Distribution Switch and Power Good	9
2.1.4	Power Distribution Switch and Single SVS	11
2.1.5	Power Distribution Switch and Dual SVS	12
2.1.6	P-Channel MOSFET and Dual SVS	14
2.2	Sequencing Solutions With Greater Than 3.3 V Available	14
2.2.1	LDO Voltage Regulator and Power Good	14
2.2.2	LDO Voltage Regulator and Single SVS	16
2.2.3	LDO Voltage Regulator and Dual SVS	17
2.2.4	Sequencing Solutions With 12 V Only Available	18
3	References	20

List of Figures

1	Dual Supplies With Bootstrap Schottky Diode	5
2	Bus Contention on Bidirectional Port Pins	5
3	Power Sequencing Using a P-Channel MOSFET and DC/DC With Power Good	7
4	Power Sequencing Using a P-Channel MOSFET and Single SVS With RESET	8
5	Power Sequencing Using the TPS2034 and Power Good Signal	10
6	Power Sequencing Using the TPS2024 and Single SVS With RESET	12
7	Power Sequencing Using the TPS2024 and Dual SVS With RESET	13
8	Power Sequencing Using a P-Channel MOSFET and Dual SVS With RESET	14
9	Power Sequencing Using the TPS76733 and Power-On-Reset Signal	15
10	Power Sequencing Using the TPS76733 and Single SVS With RESET	16
11	Power Sequencing Using the TPS76733 and Dual SVS With RESET	17
12	Power Sequencing Using a TPS5618 and TPS5633 Power Supply	19

1 Introduction

The use of dual power supply voltages is common in TI's high-performance DSPs. TI offers power management products to address these power supply requirements, and those of many other systems. This application report discusses sequencing requirements and recommendations for TI DSPs, and presents options for sequencing power supply voltages in typical DSP applications. The power supply solutions given in this report are intentionally left in general terms; details are given when they are critical to a particular sequencing solution. Additional details and application reports pertaining to components suggested can be found in the references listed at the end of the report. Since new products are continually being developed, the user is encouraged to check the TI web site at: <http://www.ti.com>, for new products and the latest application information. In particular the reader will find information on TI's newly released families of advanced dual supply regulators, **TPS563xx** and **TPS701xx** and plug-in power modules, **PT693x**, which specifically address sequencing of dual supply voltage systems.

The reader is reminded that when suggestions are made, they are made in the context of a general discussion and that the exact power supply requirements, e.g., maximum output current, output voltage tolerance, output voltage ripple, efficiency, etc., must be considered in the power supply selection or design process. It is also important to note that decoupling capacitors are not shown but should be included as needed.

Many power supply configurations are possible for powering TI's dual supply voltage DSPs, depending on the voltage(s) available from the system for use as input power, and the configuration of the DSP application (i.e., how many DSPs, how much other circuitry, etc.). This report addresses sequencing solutions for the following:

- 3.3 V only available input power
- Greater than 3.3 V available input power
- 12 V only available input power (a special case of > 3.3 V)

1.1 Core and I/O Sequencing Requirements

When designing with dual supply logic devices, consideration should be given to the relative voltage and timing of core and I/O voltage supplies during power-up and power-down operations. Internally, the core and I/O blocks are isolated by structures which may become forward biased if the supply voltages are not at specified levels. During the power-up and power-down operations, differences in the starting point and ramp rates of the two supplies may cause current to flow in the isolation structures which, when prolonged and excessive, can reduce the useable life of the semiconductor device. These currents can also trigger latch-up in devices designed with inadequate latch-up protection. TI DSPs tolerate a wide range of conditions during power up. However, some control of the power-up and power-down sequencing deserves consideration to enhance short and long term reliability of the entire system. The following note, which is included in the data sheets for dual supply voltage DSPs, presents TI's requirements with regard to power supply sequencing:

NOTE: TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to insure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long term reliability of the device.

System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers.

On C62x and C67x DSPs, during power up, it is possible for the core supply to see a high current draw (in excess of 2A) if the core supply is powered while the I/O supply is not. This high current is a result of uninitialized logic within the DSP. This high current state may damage the device if the condition exists for an extended period of time (several seconds). A normal current state will return once the I/O power supply is turned on. Decreasing the amount of time between the core supply power up and the I/O supply power up can minimize the effects of this current draw.

A dual power supply with simultaneous sequencing, such as available with TPS563xx controllers or PT693x plug-in power modules, can be used to eliminate the delay between core and I/O power up (see application note SLVA088, *Using the TPS56300 to Power DSPs*). A Schottky diode can also be used to tie the core rail to the I/O rail, effectively pulling up the I/O power supply to a level that can help initialize the logic within the DSP.

Core and I/O supply voltage regulators should be located close to the DSP or DSP array to minimize inductance and resistance in the power delivery path. Additionally, the PC board should include separate power planes for core, I/O, and ground bypassed with high-quality, low-ESL/ESR capacitors when designing for high performance applications, such as those with the C6x family of DSPs.

1.2 Completing the Power-Up and Power-Down Operations in a Timely Manner

When system power is applied, or when the DSP power supply system is enabled, both DSP supplies should power up to their respective regulation points quickly. The core and I/O supplies of a single DSP powered by a low drop-out (LDO) linear regulator will reach regulation in 100 μ s or less. A power supply capable of providing several amps to an array of DSPs typically controls the ramp-up rate to limit in-rush currents on start-up in order to reduce stress on transistors and filter capacitors. Slow-start or soft-start mechanisms ramp the supply in 10 ms to 100 ms nominally to preserve supply component reliability. Bringing the core and I/O supplies to their respective regulation levels in a maximum time frame of several hundred milliseconds, moderates the stresses placed on both the power supply and the DSP. Including a Schottky diode, connected in an anode-to-core and cathode-to-I/O fashion, further reduces potential stress on the C62x and C67x DSPs by bootstrapping the I/O supply and shortening the delay between supply ramps. The **TPS563xx** and **PT693x** products provide the most reduction by simultaneously sequencing the core and I/O supplies, typically within 20 mV of one another. This essentially eliminates the delay in power up of the two supplies. Figure 1 shows a simplified diagram of a bootstrap Schottky diode connected between the I/O and core voltage regulators and a DSP.

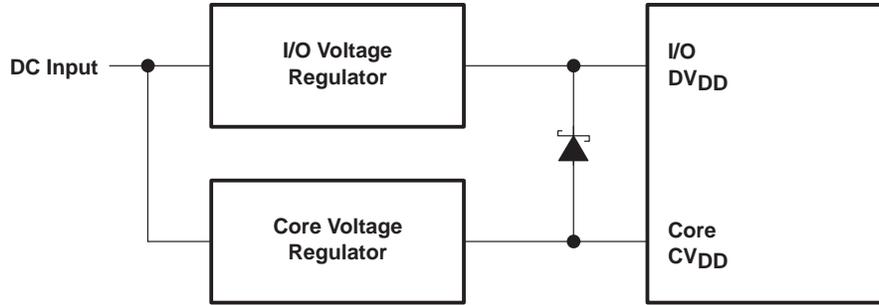


Figure 1. Dual Supplies With Bootstrap Schottky Diode

The voltage supply rails must also discharge in several hundred milliseconds upon removal of system power, or disabling of the DSP supply system. It is difficult to predict the power down rate of the core and I/O supplies, since unknown factors such as the load currents drawn from each supply during system shut down and the amount of capacitance present on each supply affect the rate of decay. Active loads enabled during the power-down operation more predictably discharge the core and I/O supply rails. The newest, DSP-specific, dual output LDO regulators and switching power supply controllers from TI activate internal loads to discharge the output rails during power down.

1.3 Sequencing the Core and I/O to Avoid System-Level Bus Contention

Of greater concern than timely power up and power down is system-level bus connection between the I/O pins of the DSP and external peripheral devices. Power supply sequencing between the core and I/O may be required to prevent bidirectional I/O pins of the DSP and a peripheral device from opposing each other. Since the bus control logic originates in the core section, powering the I/O prior to the core may result in both the DSP and peripheral pins simultaneously configured as outputs. If the data values on each side are opposing, then the output drivers contend for control. Figure 2 shows a simple representation of bidirectional ports. Excessive current will flow in one of the paths shown depending on the opposing data-out patterns. Following the recommendation to power the core at the same time or before powering the I/O prevents undefined logic states on the bus control signals.

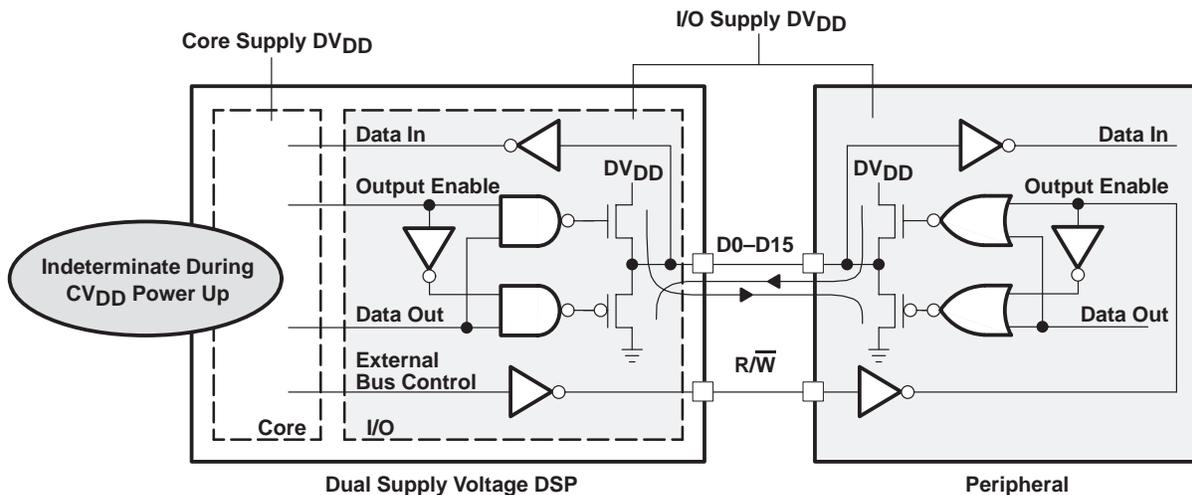


Figure 2. Bus Contention on Bidirectional Port Pins

Bus contention may also occur during power down. If the core is powered down before the I/O, the bus control signals may again become indeterminate which presents the possibility of excessive current flow through the DSP and peripheral output drivers, as with the case of power-up. Proper sequencing then, includes both core-up-first and core-down-last with respect to the I/O supply.

2 Core and I/O Supply Sequencing Options

2.1 Sequencing Solutions With 3.3 V Only Available

The solutions described in this section address systems that have 3.3 V only available as input power for the DSP application. It is assumed that 3.3 V input power supply meets the DSP's I/O supply requirements (all DSPs considered in this report require 3.3 V for the I/O supply). Several methods for powering up the DSP core supply before the I/O supply are presented that can be used to avoid system-level bus contention. These methods use either a discrete p-channel MOSFET or a TI power distribution switch to isolate the 3.3 V input supply from the DSP I/O pins while the DSP core is powering up.

2.1.1 P-Channel MOSFET and DC/DC Supply With Power Good

This approach is the simplest of those given. It does not have the features available in other approaches (discussed later) but it has the minimum number of additional components. This approach uses a p-channel power MOSFET as a power distribution switch and a dc/dc power supply with a power good (\overline{PG}) (logic low indicates that power is good) output signal.

For power-up sequencing, the I/O supply voltage is derived from the external 3.3-V input voltage through a power MOSFET switch. The core supply voltage is generated by a dc/dc power supply using the external 3.3-V as its input voltage. The dc/dc power supply is selected/selected to provide the current and voltage required for the DSP core (or multiple DSPs) and system circuitry. This dc/dc power supply could be an LDO or a switching regulator depending on the output current requirements.

For this approach, it is assumed that the dc/dc power supply has a \overline{PG} signal, i.e., it is high (or open collector) until the core supply is within its operating tolerance range. An open collector output is preferred because of MOSFET gate drive considerations. The \overline{PG} signal drives the gate of the power MOSFET switch low turning on the MOSFET to apply the external 3.3-V input to the DSP I/O input. This configuration prevents the external 3.3-V input voltage from being applied to the DSP I/O until after the core supply is within regulation, thus satisfying the power-up sequencing requirement.

For power-down sequencing, it is assumed that the external 3.3-V input voltage is removed. In this case, due to many variables, it is impossible to predict the exact power-down sequence. Unknown factors such as the load currents drawn from the core and the I/O supplies, the amount of capacitive storage present on the core and I/O supplies affect the power down sequencing. One possible power down scenario is the following: after the external 3.3-V input voltage is removed, the 3.3 V falls to approximately the level of the dc/dc power supply output voltage. Then the output of the dc/dc power supply goes out of regulation. Its \overline{PG} output will go high (or high impedance if open collector) and turn off the power MOSFET switch to remove power from the DSP I/O. For a particular system using this approach, actual power-down performance should be tested to insure proper system operation.

Figure 3 shows a simplified schematic/block diagram illustrating this approach.

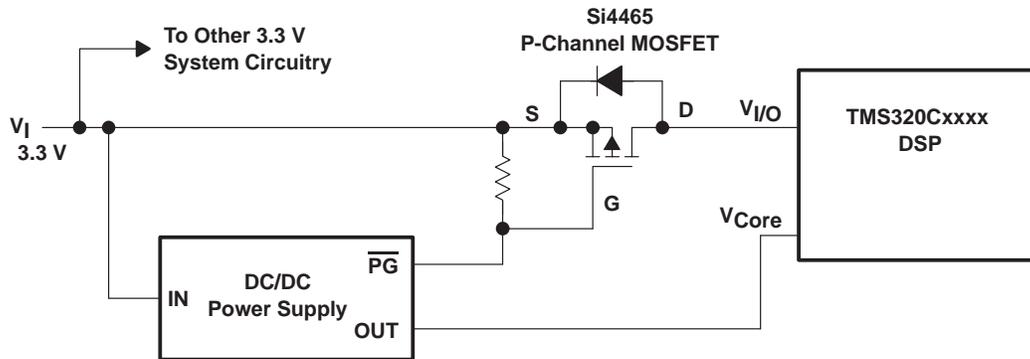


Figure 3. Power Sequencing Using a P-Channel MOSFET and DC/DC With Power Good

This approach specifies a p-channel power MOSFET used as a power distribution switch. The specific device referenced here as an example, an Si4465, has a static drain-to-source on-resistance of approximately 9 m Ω , at a gate-to-source voltage of 2.5 V in an SO-8 package. With an on-resistance this low, this transistor is capable of delivering several amps of current. Other devices with higher on-resistance are available and in different packages. It is left to the designer to choose the appropriate power MOSFET for a given application.

The guideline for choosing an on-resistance value is to ensure that no more than 1-2% of the switched voltage is dropped across the power MOSFET. The user should also verify that the power dissipation and temperature rise of the MOSFET are within the manufacturer's recommendations. In addition, the available gate-to-source drive voltage should be sufficient to fully turn on the power MOSFET for the expected load current. Since the \overline{PG} pin is often an open drain output, a resistor is shown to insure that the MOSFET turns off when the \overline{PG} pin goes to a high impedance state.

2.1.2 P-Channel MOSFET and Single SVS

If the dc/dc power supply used to supply DSP core power does not have a \overline{PG} output signal, this approach can be implemented. It uses a microprocessor supervisory circuit (supply voltage supervisor or SVS) to perform the function of a \overline{PG} signal and uses a p-channel power MOSFET as a power distribution switch to provide well-controlled power-up and power-down sequencing. Compared to the approach in Section 3.1, power-down sequencing is better controlled in this approach.

For power-up sequencing, the I/O supply voltage is derived from the external 3.3-V input voltage via a power MOSFET switch. The core supply voltage is generated by a dc/dc power supply using the external 3.3 V as its input voltage. The dc/dc power supply is selected/designed to provide the current and voltage required for the DSP core (or multiple DSPs) and system circuitry. This dc/dc power supply could be an LDO or a switching regulator depending on the output current requirements.

For this approach, the microprocessor supervisor circuit monitors the external 3.3-V input voltage. The SVS asserts a logic low RESET signal 200 ms (typ.) after the 3.3-V input supply voltage is above its undervoltage threshold. The SVS RESET signal drives the gate of the power MOSFET switch to apply the external 3.3-V input to the DSP I/O input. This configuration prevents the external 3.3-V input voltage from being applied to the DSP I/O until 200 ms after the 3.3-V input supply is up. This approach assumes that the dc/dc power supply comes up in less than 200 ms (normally a reasonable assumption). This satisfies the power-supply sequencing requirement for power-up.

For power-down sequencing, it is assumed that the external 3.3-V input voltage is removed. In this case, the SVS detects a loss of the external input voltage and asserts a logic high RESET signal thus turning off the MOSFET switch. This removes I/O power from the DSP before the core power is removed. This approach assumes that while the 3.3-V input supply voltage is decaying, the dc/dc power supply continues to supply core power to the DSP (again, a reasonable assumption). This satisfies the power-supply sequencing requirement for power-down.

Alternatively, the SVS could be connected to sense the DSP core voltage. This approach does not depend on the dc/dc power supply starting up in less than the SVS delay time of 200 ms. The I/O voltage is provided to the DSP 200 ms after the core voltage is in regulation. For power-down sequencing, the I/O supply is not removed from the DSP until the core voltage has already fallen below the SVS undervoltage sense threshold. If the dc/dc power supply for the core is out of regulation on the low side, it is likely that the input voltage is already below 3.3 V. This means that the I/O supply to the DSP is out of regulation before the power MOSFET is turned off. This condition may or may not cause system problems. For a particular system using this approach, actual power-down performance should be tested to insure proper system operation.

Figure 4 shows a simplified schematic/block diagram illustrating this approach for sensing the external 3.3-V input voltage.

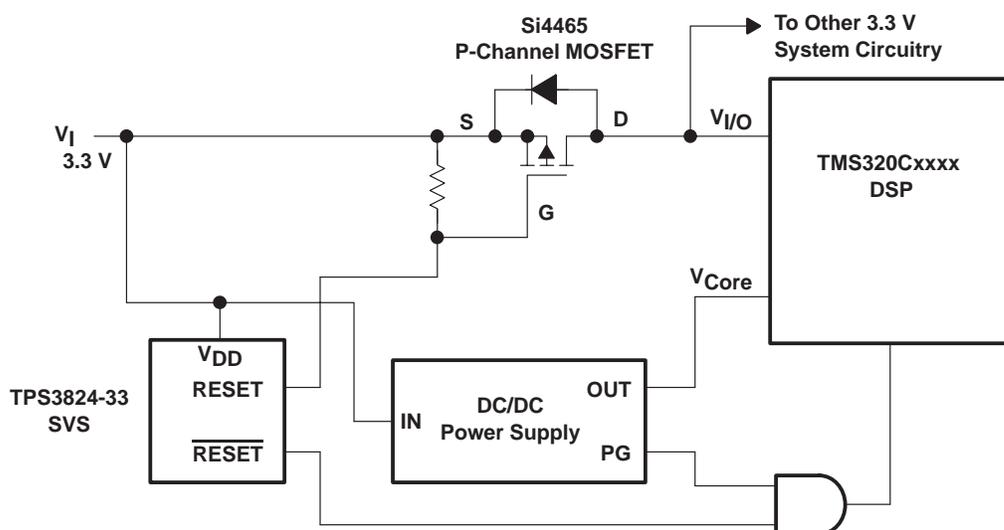


Figure 4. Power Sequencing Using a P-Channel MOSFET and Single SVS With RESET

This approach specifies a TPS3824-33 microprocessor supervisory circuit. This device, designed to monitor 3.3 V, is one of a family of micropower supply-voltage supervisors with an input supply voltage range of 1.1 V to 6 V providing circuit initialization and timing supervision. Other SVSs in this family are designed to monitor 2.5 V, 3 V, or 5 V. The SVS has a watchdog input, WDI, available for use by the designer. This input is not used in this application and can be disabled by leaving the WDI terminal open.

If the dc/dc power supply has a PG output, a single AND gate can be used to generate a signal for the RESET input of the DSP as shown in the figure. For more information on providing a power-on-reset signal to the DSP, refer to *TMS320C6x Reset Circuit Application Report*, TI literature number SPRA431.

2.1.3 Power Distribution Switch and Power Good

This approach uses a power distribution (PD) switch with an ENABLE input and a dc/dc power supply with a Power Good (PG) output signal. This option is similar to the one described in Section 3.1 with the power MOSFET being replaced by a PD switch. The PD switch has internal short circuit and thermal protection, a logic level enable input, a logic level overcurrent output signal and several other features that are not available when using a power MOSFET to switch the 3.3-V I/O voltage. This approach is recommended when the functionality of a PD switch is required.

For power-up sequencing, the I/O supply voltage is derived from the external 3.3-V input voltage via a power distribution (PD) switch with an ENABLE input. The core supply voltage is generated by a dc/dc power supply using the external 3.3-V input voltage. The dc/dc power supply is selected/selected to provide the current and voltage required for the DSP core(s) and system circuitry. This dc/dc power supply could be an LDO or a switching regulator depending on the output current requirements.

For this approach, the dc/dc power supply is assumed to have a logic high (or positive logic) PG signal, i.e., it is low until the core supply is within its operating tolerance range. The PG signal drives the ENABLE input of the PD switch. This configuration prevents the external 3.3-V input voltage from being applied to the DSP I/O until after the core supply is up satisfying the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external 3.3-V input voltage is removed. In this case, due to many variables, it is impossible to predict the exact power-down sequence. Unknown factors such as the load currents drawn from the core and the I/O supplies, the amount of capacitive storage present on the core and I/O supplies affect the power down sequencing. One possible power down scenario is the following: after the external 3.3-V input voltage is removed, the 3.3-V falls to approximately the level of the dc/dc power supply output voltage. Then the output of the dc/dc power supply goes out of regulation. Its PG output will go low and turn off the PD switch to remove power from the DSP I/O. For a particular system using this approach, actual power-down performance should be tested to insure proper system operation.

Figure 5 shows a simplified schematic/block diagram illustrating this approach. If needed, add a pull up resistor as shown connected to the EN input of the TPS2034.

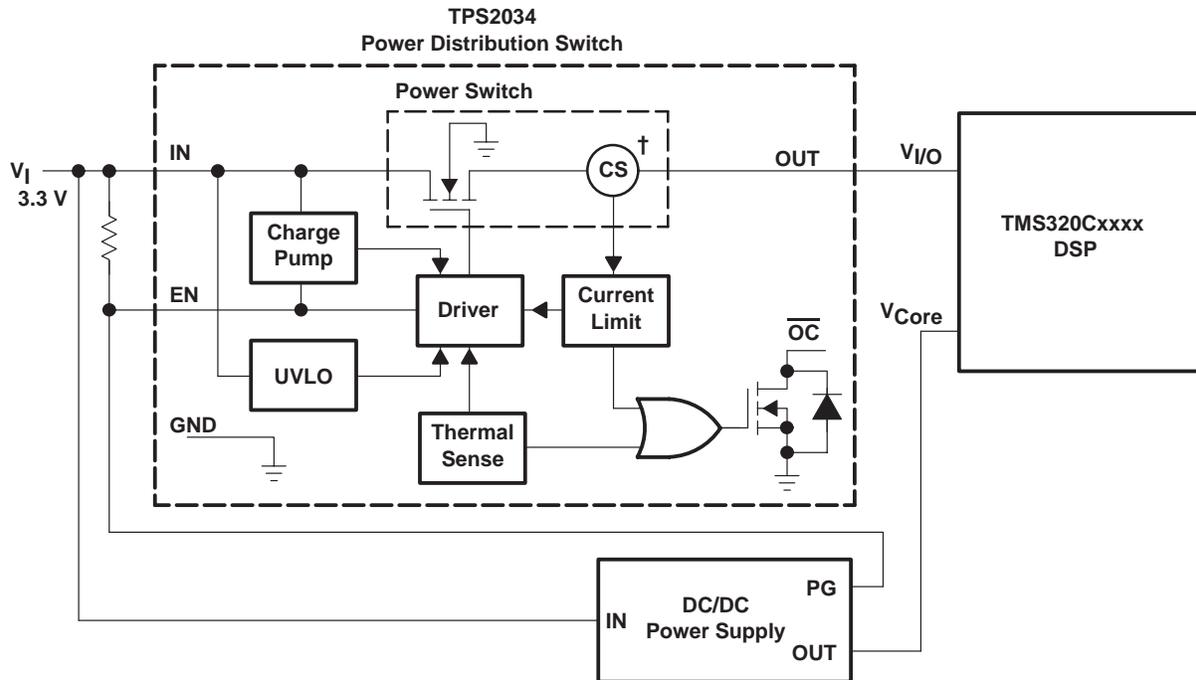


Figure 5. Power Sequencing Using the TPS2034 and Power Good Signal

This approach uses a TPS2034 power distribution switch. The TPS2034 is one of a family of devices, TPS203x devices, with an operating input voltage range of 2.7 V to 5.5 V. They differ only in short-circuit current threshold. The device specified here, the TPS2034, limits at a 3-A load. All of the devices in the TPS203x family use a power MOSFET as the switch and have the same static drain-source on-state resistance. This resistance, $r_{DS(on)}$, is specified as 37 m Ω typical at $V_I = 3.3$ V, $I_O = 1.8$ A, 25 $^{\circ}$ C. This resistance is given at a specific operating condition because it varies with temperature and current as all power MOSFET drain-source on-state resistances do. The logic-high ENABLE input requires a minimum of 2 V to turn on the switch.

With the on-state resistance of the PD switch known, one can calculate the maximum load for an acceptable error introduced on the 3.3 V supply voltage to the I/O. For example, with an on-resistance of 50 m Ω corresponding to a junction temperature of 85 $^{\circ}$ C (accounting for the increase in on-state resistance at elevated temperatures), we can calculate the maximum load current while keeping the 3.3-V error less than 2%.

$$I_{O(Max)} = \frac{V_{DS(on)}}{r_{DS(on)}} = \frac{3.3 \times 0.02}{0.05} = 1.32 \text{ A} \quad (1)$$

The above calculation shows that the current available for I/O power is enough for several DSPs.

This approach specifies a dc/dc power supply with a PG signal, which needs to be positive logic, i.e. the signal should be low until the dc/dc power supply output voltage is within its operating tolerance range.

A variation of this approach is to use a dc/dc power supply with a $\overline{\text{PG}}$ signal (a negative logic signal) and a PD switch with an ENABLE input. TI offers a family of PD switches with an ENABLE input. These devices are TPS202x family of PD switches.

2.1.4 Power Distribution Switch and Single SVS

If the dc/dc power supply used to supply DSP core power does not have a PG output signal and the functionality of a PD switch is required, this approach should be implemented. It uses a microprocessor supervisory circuit (SVS) to perform the function of a PG signal and uses a power distribution (PD) switch with an $\overline{\text{ENABLE}}$ input to provide well-controlled power-up and power-down sequencing. This option is similar to the one described in Section 3.2 with the power MOSFET being replaced by a PD switch.

For power-up sequencing, the I/O supply voltage is derived from the external 3.3-V input voltage via a PD switch. The core supply voltage is generated by a dc/dc power supply using the external 3.3 V as its input voltage. The dc/dc power supply is selected/selected to provide the current and voltage required for the DSP core (or multiple DSPs) and system circuitry. This dc/dc power supply could be an LDO or a switching regulator depending on the output current requirements.

For this approach, the SVS monitors the external 3.3-V input voltage. The SVS asserts a logic low RESET signal 200 ms (typ.) after the 3.3-V input supply voltage is above its undervoltage threshold. The SVS RESET signal drives the $\overline{\text{ENABLE}}$ input of the PD switch to apply the external 3.3-V input to the DSP I/O input. This configuration prevents the external 3.3-V input voltage from being applied to the DSP I/O until 200 ms after the 3.3-V input supply is up. This approach assumes that the dc/dc power supply comes up in less than 200 ms (normally a reasonable assumption). This satisfies the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external 3.3-V input voltage is removed. In this case, the SVS detects a loss of the external input voltage and asserts a logic high RESET signal thus turning off the PD switch. This removes I/O power from the DSP before the core power is removed. This approach assumes that while the 3.3-v input supply voltage is decaying, the dc/dc power supply continues to supply core power to the DSP (again, a reasonable assumption). This satisfies the power-supply sequencing requirement for power down.

Alternatively, the SVS could be connected to sense the DSP core voltage as described in Section 3.2.

A variation of this approach is to use an SVS with a $\overline{\text{RESET}}$ signal and a PD switch with an ENABLE input. This is essentially the same as above but with opposite logic polarity.

Figure 6 shows a simplified schematic/block diagram illustrating this approach using RESET and ENABLE.

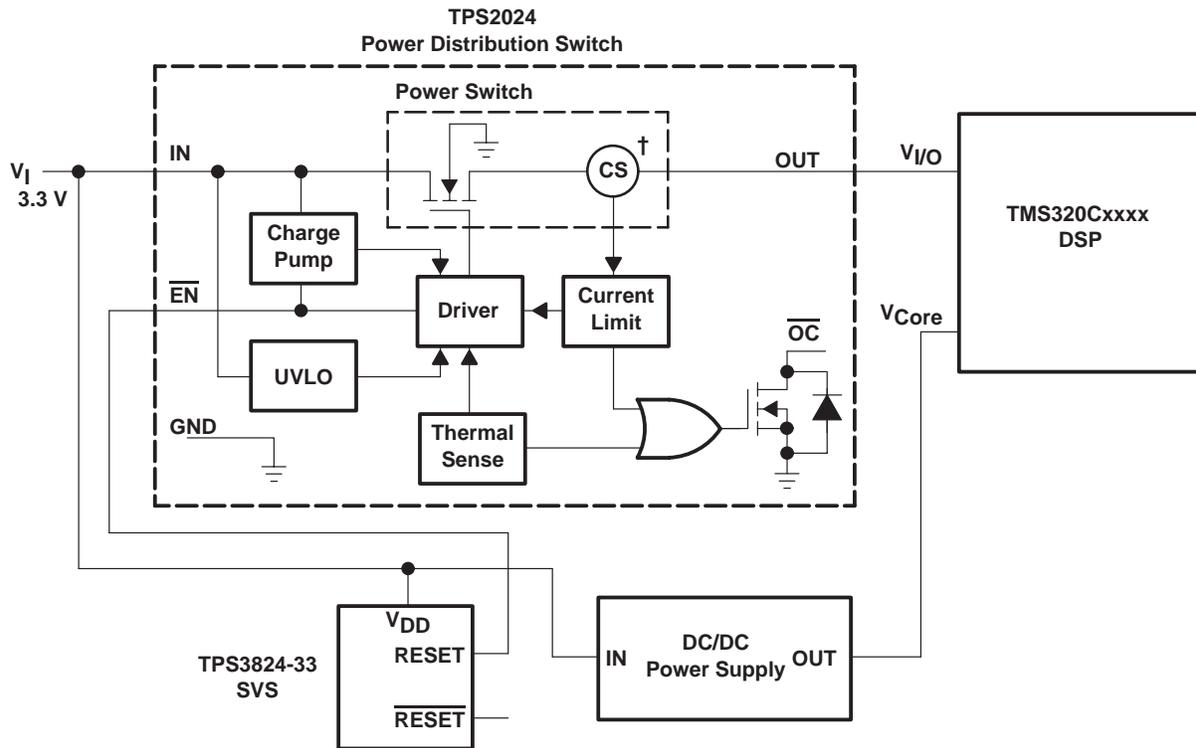


Figure 6. Power Sequencing Using the TPS2024 and Single SVS With RESET

The components suggested for this approach were discussed previously.

2.1.5 Power Distribution Switch and Dual SVS

This approach uses a power distribution switch with an $\overline{\text{ENABLE}}$ input and a dual supply voltage supervisor (SVS) circuit to provide well-controlled power-up and power-down sequencing. The dual SVS senses the external 3.3-V input voltage and the output of the dc/dc power supply. By sensing both voltages, any ambiguity is removed from power-up or power-down sequencing. On power up, the core voltage is applied before (as opposed to possibly simultaneously) and the I/O voltage and on power down, the I/O voltage is removed before (again, as opposed to possibly simultaneously) the core voltage goes down. This approach should be used if any of the previously described approaches are unsatisfactory.

For power-up sequencing, the I/O supply voltage is derived from the external 3.3-V input voltage via a power distribution (PD) switch with an $\overline{\text{ENABLE}}$ input. The core supply voltage is generated by a dc/dc power supply using the external 3.3-V as its input voltage. The dc/dc power supply is selected/selected to provide the current and voltage required for the DSP core (or multiple DSPs) and system circuitry. This dc/dc power supply could be an LDO or a switching regulator depending on the output current requirements.

For this approach, the dual-processor supervisor circuit monitors the external 3.3-V input voltage and the dc/dc power-supply output voltage. The SVS asserts a logic low RESET signal 200 ms (typ.) after both monitored supply voltages are above their respective undervoltage thresholds. The SVS RESET signal drives the $\overline{\text{ENABLE}}$ input of the PD switch. This configuration prevents the external 3.3-V input voltage from being applied to the DSP I/O until after the core supply is up satisfying the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external 3.3-V input voltage is removed. In this case, the SVS detects a loss of the external input voltage and asserts a logic high RESET signal thus turning off the PD switch. This removes I/O power from the DSP before the core power is removed fully satisfying the power-supply sequencing requirement for power down.

Figure 7 shows a simplified schematic/block diagram illustrating this approach.

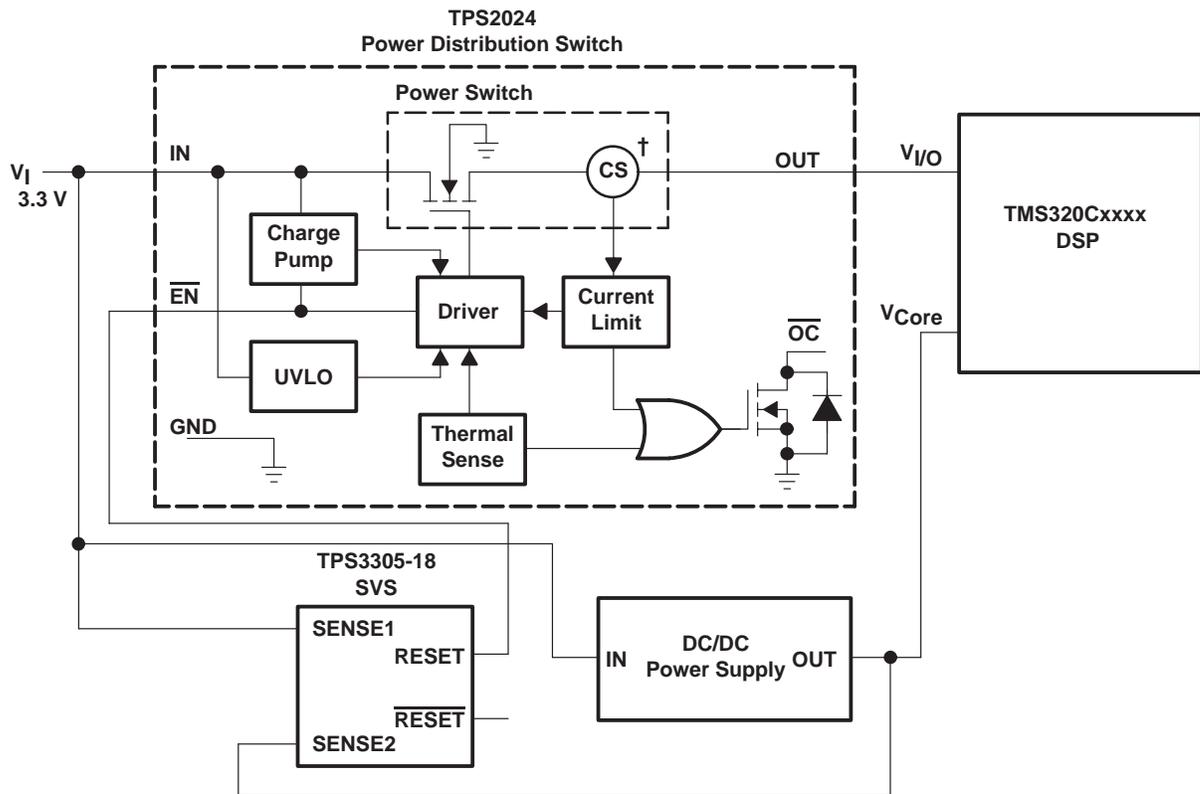


Figure 7. Power Sequencing Using the TPS2024 and Dual SVS With RESET

This approach specifies a TPS3305-18 dual processor supervisor. This device, designed to monitor 3.3 V and 1.8 V, is one of a family of devices including the TPS3305-25 (monitoring 3.3 V and 2.5 V) and the TPS3305-33 (monitoring 5 V and 3.3 V), with an input supply voltage range of 2.7 V to 6 V. However, the RESET output is defined for input supply voltages ≥ 1.1 V producing a stable RESET output during power up. The SVS has a watchdog input, WDI. This input is not used in this application and can be disabled by leaving the input open. The SVS has a manual reset input for the system designer to use if necessary. This input is not used in this application and can be left open.

As with previous approaches, variations are possible using different logic configurations. The dual SVS has both polarities of RESET available and PD switches with both polarities of ENABLE input are available.

2.1.6 P-Channel MOSFET and Dual SVS

This approach uses a p-channel power MOSFET as a power distribution switch and a dual processor supervisor supply voltage supervisor (SVS) circuit to provide well-controlled power-up and power-down sequencing. This approach is very similar to the one discussed in the previous section except that a power MOSFET is used as a power distribution switch. This approach should be used if the features in a PD switch are not required.

Figure 8 shows a simplified schematic/block diagram illustrating this approach.

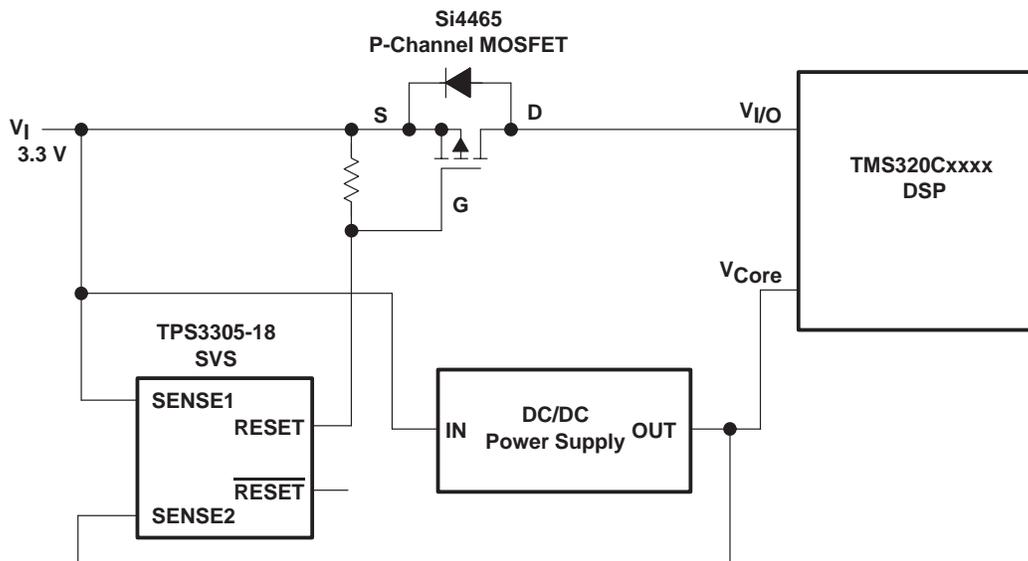


Figure 8. Power Sequencing Using a P-Channel MOSFET and Dual SVS With RESET

2.2 Sequencing Solutions With Greater Than 3.3 V Available

The solutions in this section are for systems that where the input voltage is greater than 3.3 V for input power for the DSP application. With an input voltage greater than 3.3 V, the input voltage must be regulated down to the required 3.3 V for I/O power. This section gives approaches for providing proper power-supply sequencing to DSPs.

The approaches shown below use low-dropout voltage regulators to derive the 3.3-V I/O power from the external input voltage. The main idea illustrated in the following approaches is using PG, ENABLE, and RESET signals to accomplish the desired power supply sequencing.

The total I/O current required must be estimated to insure that the LDO output current ratings are not exceeded. If more current is required, other power supply options must be considered. For a list of TI recommended power supply products for 'C5000 DSPs, see the web site <http://www.ti.com/sc/docs/msp/c5000.htm>. For TI recommended power supply products for 'C6000 DSPs, see the web site <http://www.ti.com/sc/docs/msp/c6000.htm>. The amount of power dissipated in the LDO must be calculated to insure that the LDO thermal ratings are not exceeded. In addition to the above considerations, the particular LDOs and SVSs must have input voltage ratings sufficient to withstand the expected maximum input voltage.

2.2.1 LDO Voltage Regulator and Power Good

This approach uses a low-dropout (LDO) voltage regulator with an $\overline{\text{ENABLE}}$ input and a dc/dc power supply with a power good (PG) output signal. This approach is the simplest and should be used when the control signals are already available.

For power-up sequencing, the 3.3-V I/O supply voltage is derived from the external input voltage via an LDO voltage regulator with an $\overline{\text{ENABLE}}$ input. The core supply voltage is generated by a dc/dc power supply using the external input voltage. The dc/dc power supply is selected/ designed to provide the current and voltage required for the DSP core (or multiple DSPs) and system circuitry. This dc/dc power supply could be an LDO or a switching regulator depending on the output current requirements.

For this approach, the dc/dc power supply is assumed to have a logic low (or negative logic) or $\overline{\text{PG}}$ signal, i.e., it is high until the core supply is within its operating tolerance range. The $\overline{\text{PG}}$ signal drives the $\overline{\text{ENABLE}}$ input of the voltage regulator. This configuration prevents the 3.3-V output of the voltage regulator from being applied to the DSP I/O until after the core supply is within regulation satisfying the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external input voltage is removed. In this case, due to many variables, it is impossible to predict the exact power-down sequence. Unknown factors such as the load currents drawn from the core and the I/O supplies, the amount of capacitive storage present on the core and I/O supplies affect the power down sequencing. One possible power down scenario is the following: after the external input voltage is removed, this voltage falls to approximately the level of the dc/dc power supply output voltage. Then the output of the dc/dc power supply goes out of regulation. Its $\overline{\text{PG}}$ output will go high (or high impedance if open collector) and turn off the LDO voltage regulator to remove power from the DSP I/O. For a particular system using this approach, actual power-down performance should be tested to insure proper system operation.

The TPS76733 has a power-on-reset output (POR) signal. This signal can be used as the $\overline{\text{RESET}}$ input to the DSP.

Figure 9 shows a simplified schematic/block diagram illustrating this approach.

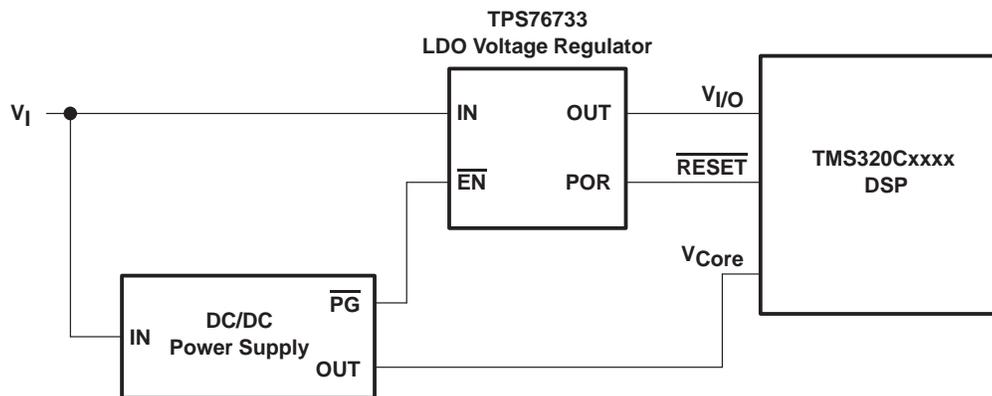


Figure 9. Power Sequencing Using the TPS76733 and Power-On-Reset Signal

This approach is shown with a TPS76733 low-dropout voltage regulator. This is given as an example to illustrate a concept. Actual current requirements for the 3.3-V output may dictate the use of a switching power supply or a lower current LDO.

The TPS76733 is one of a family of devices including the TPS76748 (4.8 V output) and the TPS76750 (5 V output) with an operating input voltage range up to 10 V and capable of delivering output current of 1 A depending on ambient thermal conditions. The logic-low $\overline{\text{ENABLE}}$ input requires a maximum voltage of 0.5 V to turn on the voltage regulator.

2.2.2 LDO Voltage Regulator and Single SVS

If the dc/dc power supply used to supply the DSP core does not have a $\overline{\text{PG}}$ output signal, the following approach should be considered. A supply voltage supervisor (SVS) IC is used to delay the power-up of the I/O supply regulator, in this case a low-dropout (LDO) voltage regulator.

For power-up sequencing, the 3.3-V I/O supply voltage is derived from the external input voltage via an LDO voltage regulator with an $\overline{\text{ENABLE}}$ input. The core supply voltage is generated by a dc/dc power supply using the external input voltage.

For this approach, the SVS circuit monitors the external input voltage. The SVS asserts a logic low RESET signal 200 ms (typ.) after the input supply voltage is above its undervoltage threshold. The SVS RESET signal drives the $\overline{\text{ENABLE}}$ input of the LDO voltage regulator. This configuration prevents the 3.3-V LDO output voltage from being applied to the DSP I/O until 200 ms after the input supply is up. This approach assumes that the dc/dc power supply comes up in less than 200 ms after application of the input voltage (normally a reasonable assumption). This satisfies the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external input voltage is removed. In this case, the SVS detects a loss of the external input voltage and asserts a logic high RESET signal to turn off the LDO voltage regulator. This removes I/O power from the DSP before the core power is removed. This approach assumes that while the input supply voltage is decaying, the dc/dc power supply continues to supply core power to the DSP (again, a reasonable assumption). This satisfies the power-supply sequencing requirement for power down.

The TPS76733 power-on-reset output (POR) signal is shown connected to the DSP $\overline{\text{RESET}}$ input.

Figure 10 shows a simplified schematic/block diagram illustrating this approach. As an example, if the input voltage is 5-V, the TPS3824-50 SVS is an appropriate choice.

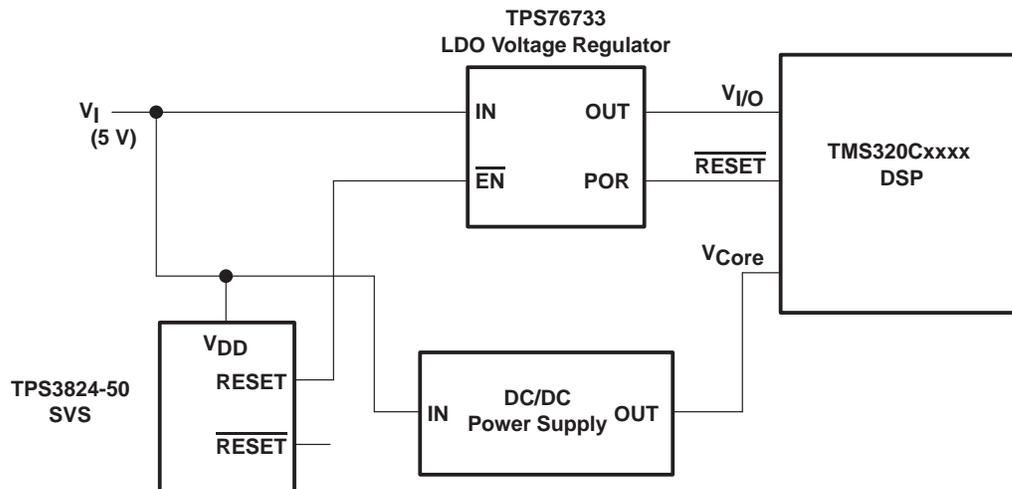


Figure 10. Power Sequencing Using the TPS76733 and Single SVS With RESET

2.2.3 LDO Voltage Regulator and Dual SVS

This approach uses a low-dropout (LDO) voltage regulator with an $\overline{\text{ENABLE}}$ input and a dual supply voltage supervisor (SVS) circuit to provide well-controlled power-up and power-down sequencing. The dual SVS senses the external input voltage and the output of the dc/dc power supply. By sensing both voltages, any ambiguity is removed from power-up or power-down sequencing. On power up, the core voltage is applied before (as opposed to possibly simultaneously) and the I/O voltage and on power down, the I/O voltage is removed before (again, as opposed to possibly simultaneously) the core voltage goes down. This approach should be used if any of the previously described approaches are unsatisfactory.

For power-up sequencing, the 3.3-V I/O supply voltage is derived from the external input voltage via an LDO voltage regulator with an $\overline{\text{ENABLE}}$ input. The core supply voltage is generated by a dc/dc power supply using the external input voltage.

For this approach, the dual-processor SVS monitors the external input voltage and the dc/dc power-supply output voltage. The SVS asserts a logic low RESET signal 200 ms (typ.) after both monitored supply voltages are above their respective undervoltage thresholds. The SVS RESET signal drives the $\overline{\text{ENABLE}}$ input of the LDO voltage regulator. This configuration prevents the 3.3-V LDO output voltage from being applied to the DSP I/O until 200 ms after both the input supply and the core supply are up. This satisfies the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external input voltage is removed. In this case, the SVS detects a loss of the external input voltage and asserts a logic high RESET signal thus turning off the LDO voltage regulator. This removes I/O power from the DSP before the core power is removed. This approach assumes that while the input supply voltage is decaying, the dc/dc power supply continues to supply core power to the DSP (a reasonable assumption). This satisfies the power-supply sequencing requirement for power-down.

The TPS76733 power-on-reset (POR) output signal is shown connected to the DSP $\overline{\text{RESET}}$ input.

Figure 11 shows a simplified schematic/block diagram illustrating this approach. This circuit is also an example showing an external input voltage of 5 V.

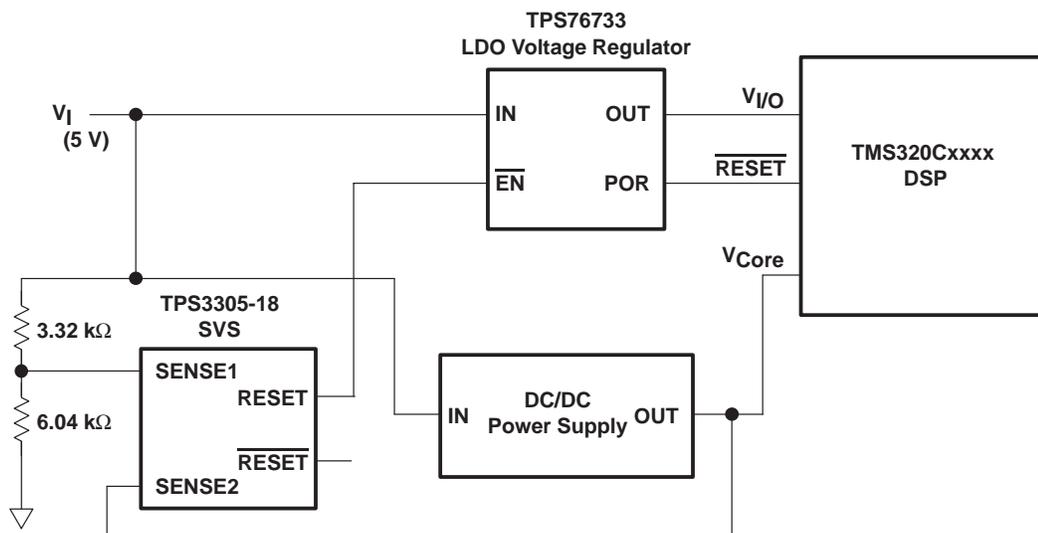


Figure 11. Power Sequencing Using the TPS76733 and Dual SVS With RESET

This approach, shown here with an external input voltage of 5-V, specifies a TPS3305-18 dual processor supervisor that was discussed in a previous section. This device is designed to monitor 3.3 V and 1.8 V. Although the TPS3305 is a dual input supervisor, there is currently no option available designed to monitor 5 V and 1.8 V. However, with an external resistive voltage divider, the 3.3 V sense input of the SVS is configured to monitor the external 5-V input voltage. The resistor values shown are selected to interface with the internal divider resistors of the TPS3305-18. The internal divider resistors for a 3.3-V input are both greater than 500 k Ω (see Table 3 of TI Literature Number SLVA056)

2.2.4 Sequencing Solutions With 12 V Only Available

The solutions in this section are for systems that only have 12 V available for input power for the DSP application. The approaches for this 12-V only configuration are essentially the same as for the 5-V only configuration. If an SVS is used, choose an SVS with a voltage rating compatible with the 12-V input voltage and its expected variations. The selection/design of the power supply for the 3.3-V DSP I/O supply should also be revisited. Even with a single DSP, the I/O current requirement of 150 mA may preclude the use of an LDO voltage regulator due to power dissipation considerations. Texas Instruments offers several power supply solutions for an input voltage of 12 V.

One specific approach is presented here that does not use an SVS.

2.2.4.1 TPS5618 Power Supply and TPS5633 Power Supply

This approach uses two independent power supplies, each controlled by one of the TPS56xx family of controllers. The controllers have a built in PG output and an INHIBIT input. These two signals can be configured to provide proper power-supply sequencing with no need for any additional circuits.

For power-up sequencing, the 3.3-V I/O supply voltage is derived from the external 12-V input voltage via a switching dc/dc power supply controlled by a TPS5633 with a PG output and INHIBIT input. The core supply voltage is generated by a switching dc/dc power supply controlled by a TPS5618 with a PG output and INHIBIT input.

For this approach, the 1.8-V dc/dc power supply has a logic high (or positive logic) PG, signal, i.e., it is low until the core supply is above 93% of its nominal output voltage of 1.8 V. The PG signal drives the INHIBIT input of the 3.3-V dc/dc power supply. This configuration prevents the 3.3-V output of the dc/dc power supply from being applied to the DSP I/O until after the core dc/dc power supply is up satisfying the power-supply sequencing requirement for power up.

For power-down sequencing, it is assumed that the external 12-V input voltage is removed. In this case, the input undervoltage lockout circuits of the TPS5618 and TPS5633 controllers activate and both outputs are turned off simultaneously. This satisfies the power-supply sequencing requirement for power down.

Figure 12 shows a simplified schematic/block diagram illustrating this approach. A single SVS, the TPS3824-33, is used to provide a $\overline{\text{RESET}}$ signal to the DSP.

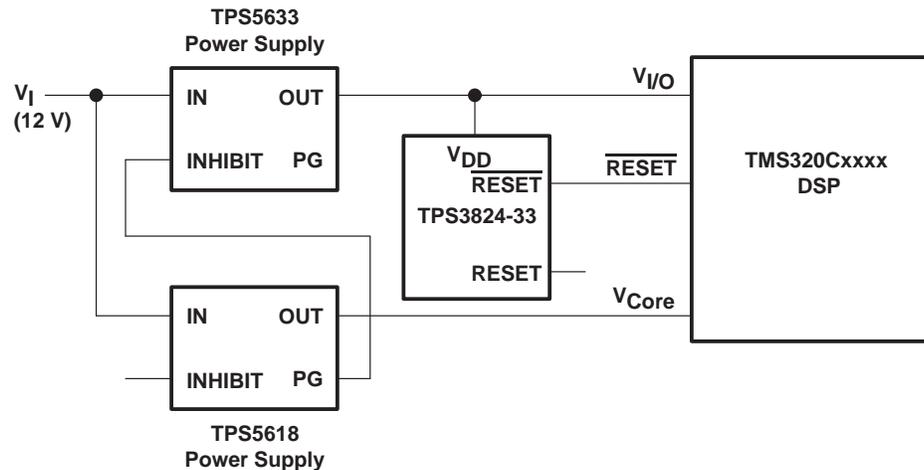


Figure 12. Power Sequencing Using a TPS5618 and TPS5633 Power Supply

This approach uses power supplies controlled by the TPS5633 and TPS5618 controllers. Texas Instruments offers the TPS56xx family of synchronous-buck hysteretic regulator controllers capable of operating on a single input voltage of 12 V. A PG output signal (open-drain, requiring a pullup resistor) and an INHIBIT input along with several other features make these controllers well suited for the 12-V to 3.3-V and 12-V to 1.8-V power supplies for this approach. The PG output signal goes high whenever the output voltage is above 93% of its nominal value. For complete details, refer to the *TPS5615, TPS5618, TPS5625, TPS5633 Synchronous-Buck Hysteretic Regulator Controller* datasheet, Texas Instruments literature number SLVS177A.

3 References

1. TPS2030, TPS2031, TPS2032, TPS2033, TPS2034 Power-Distribution Switches Datasheet, Texas Instruments Literature Number SLVS190
2. TPS2020, TPS2021, TPS2022, TPS2023, TPS2024 Power-Distribution Switches Datasheet, Texas Instruments Literature Number SLVS175
3. *TPS202x/3x and TPS204x/5x USB Power Distribution*, Application Report, Texas Instruments Literature Number SLVA049
4. TPS3823-25, TPS3823-30, TPS2823-33, TPS3823-50, TPS3824-25, TPS3824-30, TPS3824-33, TPS3824-50 Microprocessor Supervisory Circuits Datasheet, Texas Instruments Literature Number SLVS165A
5. *TPS382x Microprocessor Supervisory Circuits With Watchdog Function in SOT-23 Package*, Application Report, Texas Instruments Literature Number SLVA039
6. TPS3305-18, TPS3305-25, TPS3305-33 Dual Processor Supervisors Datasheet, Texas Instruments Literature Number SLVS198
7. *TPS3305 and TPS3307 Supervising DSP and Processor Applications* Application Report, Texas Instruments Literature Number SLVA056
8. TPS7101Q, ... TPS7150Y Low-Dropout Voltage Regulators Datasheet, Texas Instruments Literature Number SLVS092F
9. *TMS320C62x/67x Power Supply Solutions for 1-2 DSPs: Using the TL5001A and TPS7133* Application Report, Texas Instruments Literature Number SLVA066
10. TPS5615, TPS5618, TPS5625, TPS5633 Synchronous-Buck Hysteretic Regulator Controller Datasheet, Texas Instruments Literature Number SLVS177A
11. *Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs* User's Guide, Texas Instruments Literature Number SLVU007
12. *Designing Fast Response Synchronous Buck Converters Using the TPS5210* Application Report, Literature Number SLVA044
13. TPS5210 Programmable Synchronous-buck Regulator Controller data sheet, Literature Number SLVS171.
14. *Dual Power Supply Management for the TMS320VC549 Digital Signal Processor* Application Report, Literature Number SPRA280A

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.