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Technical Review of Low Dropout Voltage Regulator Operation and Performance

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Contents

List of Figures

List of Tables

Technical Review of Low Dropout Voltage Regulator Operation and Performance

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ABSTRACT

This application report provides a technical review of low dropout (LDO) voltage regulators, and describes fundamental concepts including dropout voltage, quiescent current, and topologies. The report also includes detailed discussions of load/line regulation, efficiency, frequency response, range of stable ESR, and accuracy of LDO voltage regulators.

1 Dropout Voltage

Dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage. Figure 1 shows an example of a simple NMOS low dropout (LDO) voltage regulator.

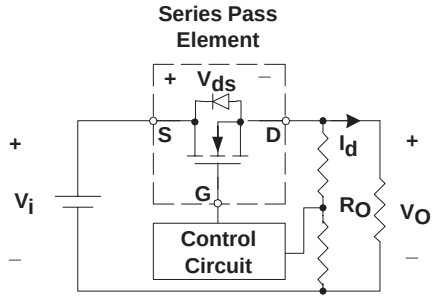
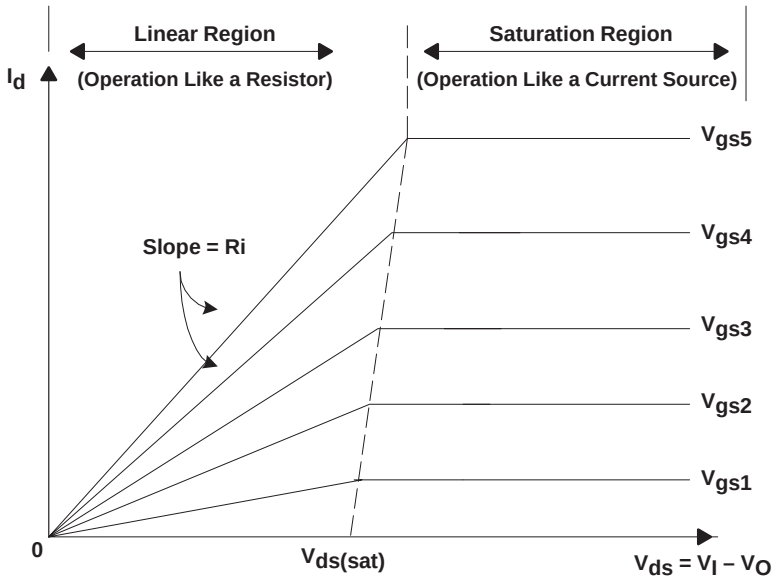
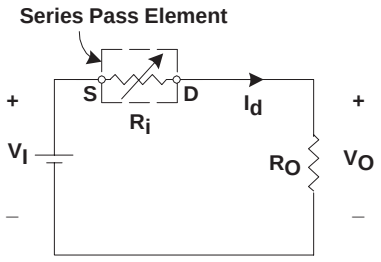


Figure 1. LDO Voltage Regulator

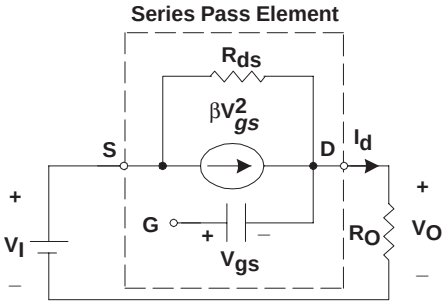
LDO operation can be explained using the NMOS series pass element I-V characteristics shown in Figure 2. NMOS devices are not widely used in LDO designs, but they simplify the explanation of LDO performance. Figure 2 (a) shows the two regions of operation—linear and saturation. In the linear region, the series pass element acts like a series resistor. In the saturation region, the device becomes a voltage-controlled current source. Voltage regulators usually operate in the saturation region.



(a) I-V Characteristic of n-channel MOSFET



(b) LDO Equivalent Circuit in The Linear Region



(c) LDO Equivalent Circuit in The Saturation Region

Figure 2. Series Pass Element I-V Characteristic and LDO Equivalent Circuits

Figures 2 (b) and (c) show the LDO equivalent circuits for the two operating regions. The control circuit is not shown. Figure 2 (c) shows the LDO equivalent circuit in the saturation region (assume threshold voltage is zero). There is a constant current source between the drain and source, which is a function of gate-to-source voltage, V_{gs}. The drain current (load current) is given by

$$I_d = \beta V_{gs}^2 \tag{1}$$

Where β is a current gain.

From equation (1), the series pass element acts like a constant current source in the saturation region in terms of gate-to-source voltage. Under varying load conditions, V_{gs} controls the LDO regulator to supply the demand output load. Figure 3 illustrates the LDO operation in the saturation region. When load current increases from Id_2 to Id_3, the operating point moves from P_0 to P_2, and the input-to-output voltage differential, V_{ds}, is given by

$$V_{ds} = V_I - V_O \tag{2}$$

From equation (2) and Figure 3, as the input voltage decreases, the voltage regulator pushes the operating point toward P_1 (toward the dropout region). As the input voltage nears the output voltage, a critical point exists at which the voltage regulator can not maintain a regulated output. The point at which the LDO circuit begins to lose loop control is called the dropout voltage. Below the dropout voltage, the LDO regulator can no longer regulate the output.

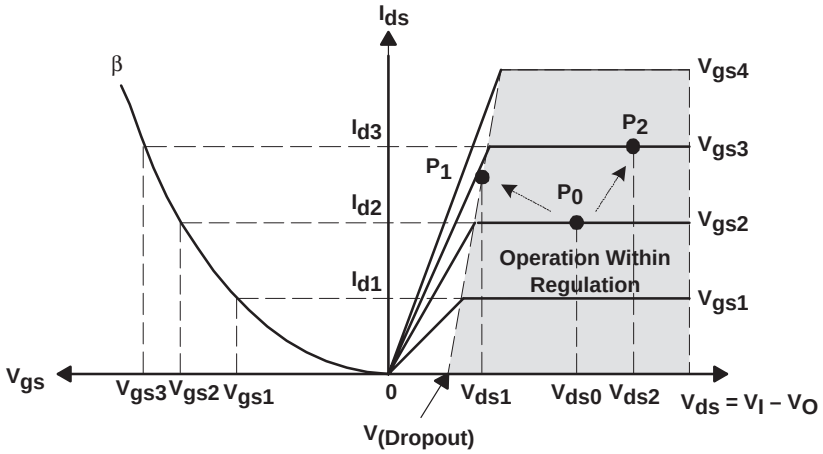


Figure 3. NMOS Operation With LDO in Saturation Region

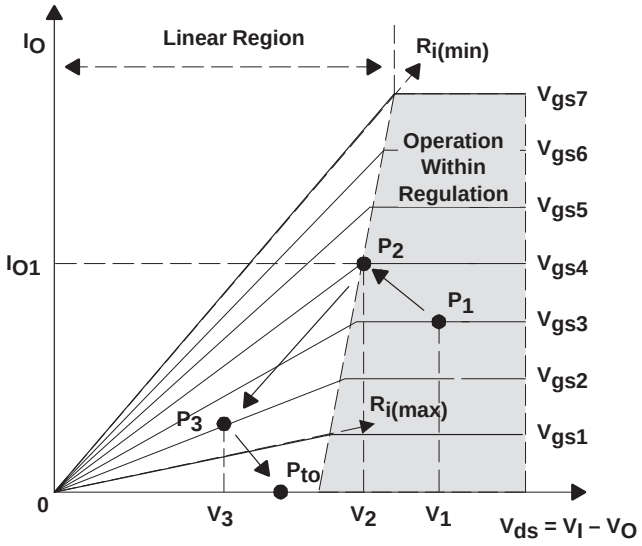


Figure 4. NMOS Operation With LDO in Dropout Region

In the dropout region, the series pass element limits the load current like a resistor—as shown in Figure 2 (b). Figure 4 shows NMOS operation with the LDO regulator in the dropout region and decreasing input voltage. The equivalent resistors $R_{i(max)}$ and $R_{i(min)}$ are the maximum and minimum values respectively of the series pass element in the linear region. When the input voltage decreases to near the output voltage, the operating point P_1 moves to the operating point P_2 that is the minimum regulating point at the specific load condition (I_{O1}) (i.e., dropout voltage). Within the dropout region, V_{gs} is not a function of the control loop, but of the input voltage. In other words, the regulator control loop cut off and V_{gs} begins to depend on the decreasing input voltage. Thus when the input

voltage decreases further, the control voltage (V_{gs}) also decreases in proportion to the decreasing input voltage. The operating point moves down to P_3 from P_2. Finally, the regulator reaches the turnoff point, P_{to}.

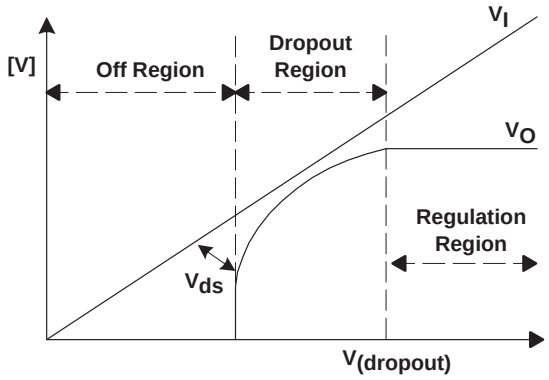


Figure 5. Typical Input/Output Voltage Characteristics of a Linear Regulator

Figure 5 shows the dropout region in relation to the off and regulation regions. Below $V_{(dropout)}$, the output voltage drops with decreasing input voltage.

1.1 Application Implications

In dropout region, the magnitude of the dropout voltage depends on the load current and the on resistance (R_{on}) of the series pass element. It is given by

$$V_{do} = I_{Load} R_{on} \tag{3}$$

Throughout the dropout region, the output voltage is not maintained any more by the control loop since the control loop is electrically disconnected at the output of the controller (Figure 1) and then the pass device acts like a resistor. Therefore, the output voltage can be pulled down to ground by the load.

Figure 6 shows the input-output characteristics of the TPS76333 3.3-V LDO regulator. The dropout voltage of the TPS76333 is typically 300 mV at 150 mA. The LDO regulator begins dropping out at 3.6-V input voltage; the range of the dropout region is between 3.6 V and 2.0 V input voltage.

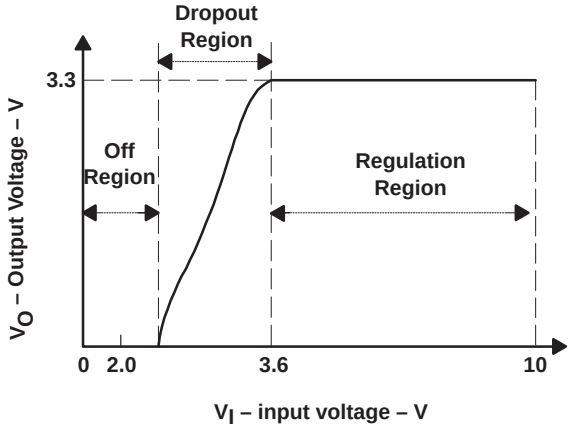


Figure 6. Dropout Region of TI TPS76333 (3.3-V LDO)

2 Quiescent Current or Ground Current

Quiescent current, or ground current, is the difference between input and output currents. Minimum quiescent current is necessary for maximum current efficiency. Quiescent current is defined by

$$I_q = I_I - I_O \tag{4}$$

Quiescent current consists of bias current (such as band-gap reference, sampling resistor and error amplifier) and drive current of the series pass element, which do not contribute to output power. The value of quiescent current is mostly determined by the series pass element, topologies, ambient temperature, etc.

Linear voltage regulators usually employ bipolar or MOS transistors as the series pass element. The collector current of bipolar transistors is given by

$$I_c = \beta I_b \tag{5}$$

where β is forward current gain and typically ranges from 20-500, I_c is the collector current, and I_b is the base current. Figure 7 shows the I-V characteristic of bipolar transistors.

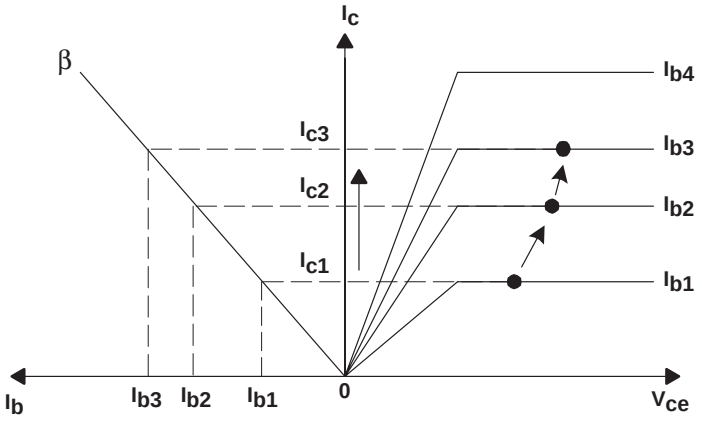


Figure 7. I-V Characteristic of Bipolar Transistors

Equation (5) and Figure 7 show that the base current of bipolar transistors is proportional to the collector current. As load current increases, base current also increases. Since base current contributes to quiescent current, bipolar transistors intrinsically have high quiescent currents. In addiiton, during the drop out region the quiescent current can increase due to the addiitional parasitic current path between the emitter and the base of the bipolar transistor, which is caused by a lower base voltage than that of the output voltage.

The drain-source current of MOS transistors is given by

$$I_{ds} = \beta_1 \left(V_{gs} - V_t \right)^2 \tag{6}$$

where β_1 is a MOS transistor gain factor, V_{gs} is the gate-to-source voltage, and V_t is the device threshold. Figure 8 shows the I-V characteristic of MOS transistors.

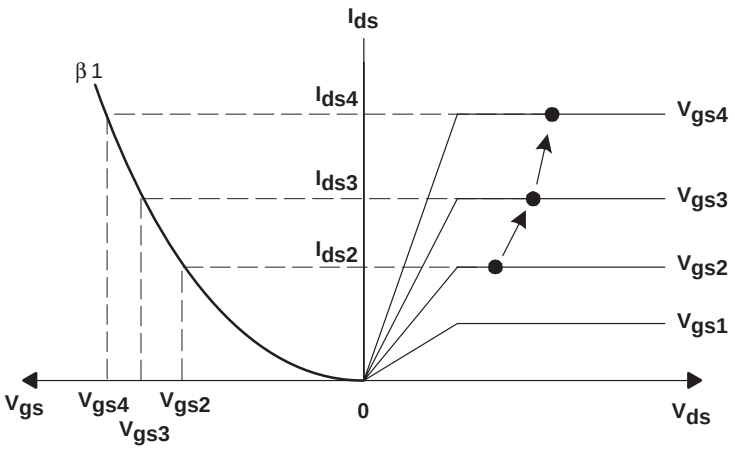


Figure 8. I-V Characteristic of MOS Transistors

The drain-to-source current is a function of the gate-to-source voltage, not the gate current. Thus, MOS transistors maintain a near constant gate current regardless of the load condition.

2.1 Application Implications

Figure 9 shows the quiescent current of both transistors with respect to the load current.

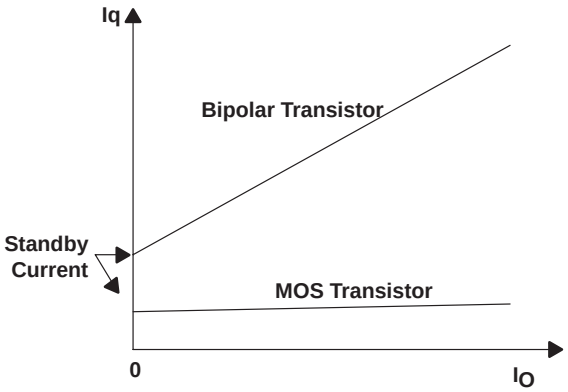


Figure 9. Quiescent Current and Output Current

For bipolar transistors, the quiescent current increases proportionally with the output current because the series pass element is a current-driven device. For MOS transistors, the quiescent current has a near constant value with respect to the load current since the device is voltage-driven. The only things that contribute to the quiescent current for MOS transistors are the biasing currents of band-gap, sampling resistor, and error amplifier. In applications where power consumption is critical or where small bias current is needed in comparison with the output current, an LDO voltage regulator employing MOS transistors is essential.

3 LDO Topologies

The regulator circuit can be partitioned into four functional blocks: the reference, the pass element, the sampling resistor, and the error amplifier as shown in Figure 10.

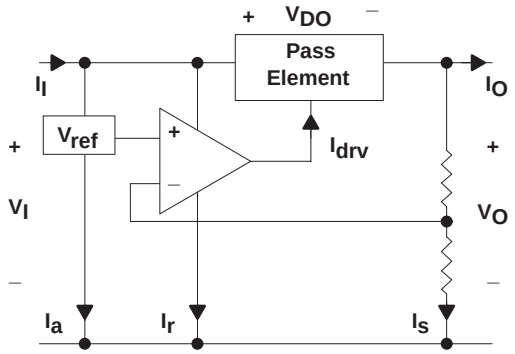


Figure 10. Linear Regulator

Figure 11 shows that linear voltage regulators can be classified based on pass element structures: NPN-Darlington, NPN, PNP, PMOS, and NMOS regulators. The bipolar devices can deliver the highest output currents for a given supply voltage. The MOS-based circuits offer limited drive performance with a strong dependence on aspect ratio (width to length ratio) and to voltage-gate drive. On the positive side, however, the voltage-driven MOS devices minimize quiescent current flow.

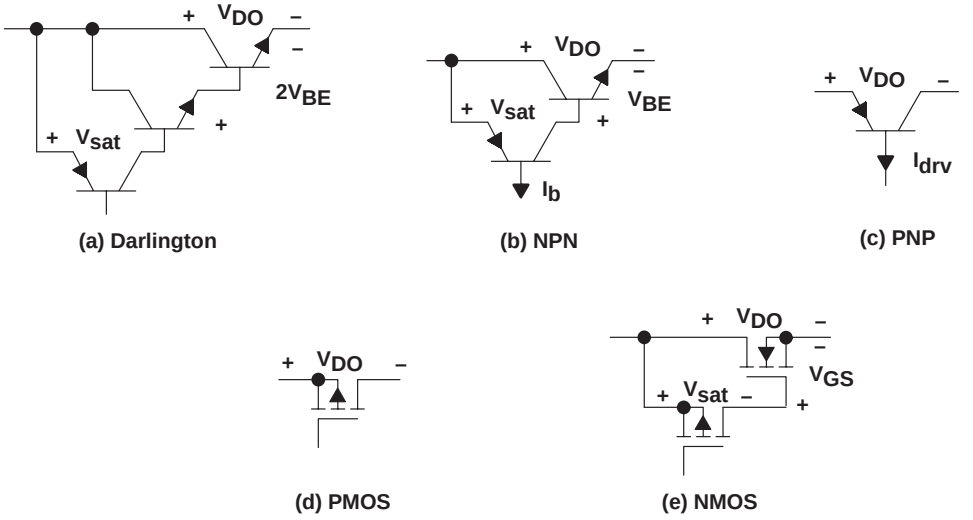


Figure 11. Pass Element Structures

The Darlington requires at least 1.6 V of dropout voltage to regulate, while the LDO will typically work with less than 500 mV of input-to-output voltage differential. The dropout voltage of NPN-Darlington is given by

$$V_{(dropout)} = V_{CE}(sat) + 2V_{BE} \cong 1.6 \sim 2.5\ V \qquad \text{for Darlington} \tag{7}$$

The NPN regulator is comprised of an NPN and a PNP transistor. The base potential of the NPN transistor should always be higher than the emitter potential to ensure proper operation of the pass element. When the input-output differential voltage is high, there is no problem. When the input voltage approaches the output voltage, the control circuit pushes the pass element toward saturation to ensure proper operation of the regulator, and the value of the transistor equivalent variable resistor decreases. However, the equivalent variable resistor can not decrease to zero because the transistor NPN needs to maintain a necessary V_{be} level. Below a certain level of input voltage, the regulator cannot maintain the regulation.

The minimum voltage difference between the input and output required to maintain regulation (dropout voltage) is given by

$$V_{(dropout)} = V_{CE}(sat) + V_{BE} \geq 0.9\ V \qquad \text{for NPN regulator} \tag{8}$$

The NPN transistor receives its drive current from the input rail through the PNP transistor. The base drive circuit contributes its emitter current (I_{drv}) to output current (I_O). Therefore, the quiescent current of the NPN regulator is small. The quiescent current for the NPN regulator is defined as follows:

$$I_q = I_{bias} \qquad \text{for NPN regulator} \tag{9}$$

Where:

I_q = quiescent current
I_{bias} = total bias current ($I_{bias} = I_a + I_r + I_s$)

The PNP regulator shown in Figure 11 (c) operates the same as the NPN with the exception that the NPN pass transistor has been replaced by a single PNP transistor. The big advantage of the PNP regulator is that the PNP pass transistor can maintain output regulation with very little voltage drop across it.

$$V_{(dropout)} = V_{CE}(sat) \cong 0.15 \sim 0.4\ V \qquad \text{for PNP regulator} \tag{10}$$

By selecting a high-gain series transistor, dropout voltages as low as 150 mV at 100 mA are possible. However, the base drive current flows to ground and no longer contributes to the output current. The value of this ground current directly depends on the pass element transistor's gain. Thus, the quiescent current of the PNP regulator is higher than the NPN regulator. The quiescent current is defined as follows:

$$I_q = I_{drv} + I_{bias} \cong 0.8 \sim 2.6\ mA \qquad \text{for PNP regulator} \tag{11}$$

Where:

I_{drv} = base drive current of PNP

Figures 11(d) and 11(e) show the P-MOS and N-MOS voltage regulators respectively, which employ MOSFETs as the pass element. The PMOS devices have very low dropout voltages. The NMOS can have a low dropout voltage with a charge pump. The dropout voltage is determined by saturation voltage across the pass element, and the dropout voltage is proportional to the current flowing through the pass element.

$$V_{(dropout)} = I_o R_{on} \cong 35 \sim 350\ mV \qquad \text{for PMOS regulator} \tag{12}$$

where R_{on} is the on-resistance of the pass element

At light load, the dropout voltage is only a few millivolts. At full load, the typical dropout voltage is 300 mV for most of the families. The MOSFET pass element is a voltage controlled device and, unlike a PNP transistor, does not require increased drive current as output current increases. Thus, very low quiescent current is obtained (less than 1 mA).

3.1 Application Implications

Table 1 summarizes the differences of these pass element devices.[2]

Table 1. Comparison of Pass Element Structures

PARAMETER	DARLINGTON	NPN	PNP	NMOS	PMOS
$I_{o,max}$	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{dropout}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	$V_{ce(sat)}$	$V_{sat}+V_{gs}$	$V_{SD(sat)}$
Speed	Fast	Fast	Slow	Medium	Medium

Traditionally, the PNP bipolar transistor has been applied to low dropout applications, primarily because it easily enables a low drop out voltage. However, it has a high quiescent current and low efficiency, which are not ideal in applications where maximizing efficiency is a priority. The NMOS pass element is most advantageous due to its low on resistance. Unfortunately, the gate drive difficulties make it less than ideal in applicaitons and as a result there are few NMOS LDOs available. PMOS devices have been highly developed and now have performance levels exceeding most bipolar devices.

4 Efficiency

The efficiency of a LDO regulator is limited by the quiescent current and input/output voltage as follows:

$$Efficiency = \frac{I_o V_o}{\left(I_o + I_q\right) V_I} \times 100 \tag{13}$$

To have a high efficiency LDO regulator, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized since the power dissipation of LDO regulators accounts for the efficiency$\left(Power\ Dissipation = \left(V_I - V_O\right) I_O\right)$. The input/output voltage difference is an intrinsic factor in determining the efficiency regardless of the load condition.

4.1 Application Implications—An Example

What is the efficiency of the TPS76333 3.3-V LDO regulator with the following operating conditions?

- Input voltage range is 3.8 V to 4.5 V.
- Output current range is 100 mA to 150 mA.
- Maximum quiescent current is 140 μA.

$$Efficiency = \frac{150\ mA \times 3.3}{(150\ mA + 140\ \mu A)4.5\ V} \times 100 = 73.2\% \quad (14)$$

5 Load Regulation

Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions. Load regulation is defined as

$$\text{Load regulation; } \frac{\Delta V_o}{\Delta I_o} \quad (15)$$

Figure 12 shows a PMOS voltage regulator. The output voltage change for a given load change ($\Delta V_O/\Delta I_O$) under constant input voltage V_I can be calculated as follows:

Q_1 is the series pass element, and β is the current gain of Q_1. g_a is the transconductance of the error amplifier at its operating point.

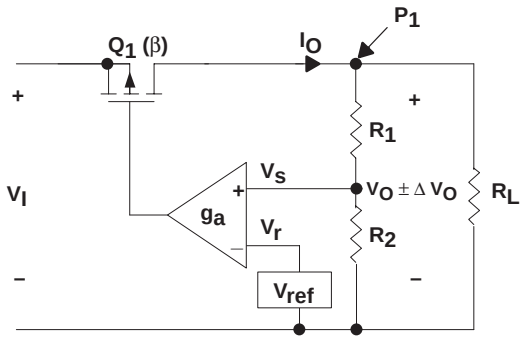


Figure 12. PMOS Voltage Regulator

Assume that there is a small output current change (ΔI_O). The change of output current causes the output voltage change. Thus,

$$\Delta V_o = \Delta I_o R_{eq} \quad (16)$$

Where R_{eq} is the equivalent output resistor at P_1 ($R_{eq} = (R_1 + R_2) \| R_L \approx R_L$).

The change of sensed voltage multiplied by g_a of the error amplifier input difference and β of the PMOS current gain (Figure 12) must be enough to achieve the specified change of output current. Thus,

$$\Delta I_o = \beta\ g_a \Delta V_s = \beta\ g_a \left(\frac{R_2}{R_1 + R_2} \right) \Delta V_o \quad (17)$$

Then, the load regulation is obtained from equation (17).

$$\frac{\Delta V_o}{\Delta I_o} = \frac{1}{\beta g_a} \left(\frac{R_1 + R_2}{R_2} \right) \quad (18)$$

Since load regulation is a steady-state parameter, all frequency components are neglected. The load regulation is limited by the open loop current gain of the system. As noted from the above equation, increasing dc open-loop current gain improves load regulation.

5.1 Application Implications

The worst case of the output voltage variations occurs as the load current transitions from zero to its maximum rated value or vice versa. Figure 13 shows that the load regulation is determined by the ΔV_{LDR}. Figure 14 shows the output voltage variation with respect to the output current with the TPS76350 5-V LDO regulator.

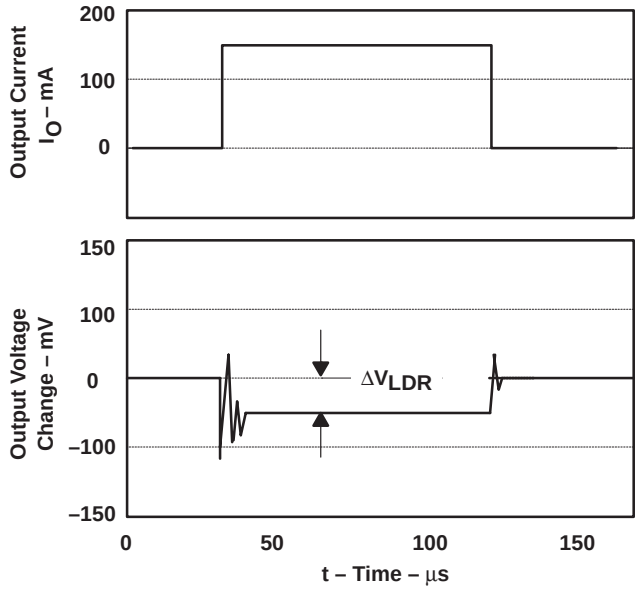


Figure 13. Load Transient Response of TPS76350

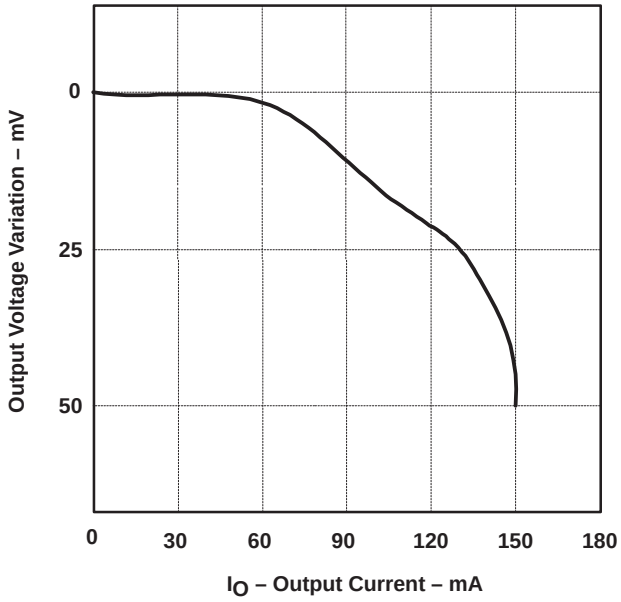


Figure 14. TPS76350 Output Voltage With Respect to Output Current

6 Line Regulation

Line regulation is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as

$$\text{Line regulation; } \frac{\Delta V_o}{\Delta V_I} \tag{19}$$

The output voltage change for a given input voltage change (ΔV_o / ΔV_I) can be calculated from Figure 12 as follows;

$$\begin{aligned} V_o &= \frac{V_I R_{eq}}{R_{ds} + R_{eq}} - \Delta V_o = \frac{V_I R_{eq}}{R_{ds} + R_{eq}} - \Delta I_o R_{eq} \\ &= \frac{V_I R_{eq}}{R_{ds} + R_{eq}} - G(V_s - V_r) R_{eq} \end{aligned} \tag{20}$$

where the open loop current gain $G = \beta \times g_a$, and R_{ds} is the equivalent resistor between drain and source of the series pass element. R_{eq} is the equivalent output resistor at the point P_1 ($R_{eq} = (R_1 + R_2) \| R_L \approx R_L$). The sensed voltage V_s is given by

$$V_s = \frac{R_2}{R_1 + R_2} V_o \tag{21}$$

Substituting (21) into equation (20),

$$V_o = \frac{\frac{R_{eq}(R_1 + R_2)}{R_{ds} + R_{eq}} V_I + (R_1 + R_2) G V_r R_{eq}}{R_1 + R_2 + G R_2 R_{eq}} \tag{22}$$

Now in the usual case,

$$G V_s \gg 1 \tag{23}$$

From equations (22) and (23), the output voltage is

$$V_o = \frac{(R_1 + R_2)}{G R_2 (R_{ds} + R_{eq})} V_I + \frac{(R_1 + R_2)}{R_2} V_r \tag{24}$$

Now, the right hand side of the equation can be split into two parts. One is the steady state average output voltage and the another is the function of input voltage. The average steady state output voltage is then given by

$$V_o = \frac{(R_1 + R_2)}{R_2} V_r \tag{25}$$

Thus, the line regulation is obtained from equation (24).

$$\frac{\Delta V_o}{\Delta V_I} = \frac{1}{(R_{ds} + R_L)} \frac{(R_1 + R_2)}{G R_2} \tag{26}$$

Or substituting the open loop current gain G into equation (26), the line regulation can be

$$\frac{\Delta V_O}{\Delta V_I} = \left[\frac{1}{\left(R_{ds} + R_L\right)\beta g_a}\right]\left(\frac{R_1 + R_2}{R_2}\right) \quad (27)$$

Like load regulation, line regulation is a steady state parameter—all frequency components are neglected. Increasing dc open loop current gain improves the line regulation.

6.1 Application Implications

Figure 15 shows the input voltage transient response; the line regulation is determined by ΔV_{LR}.

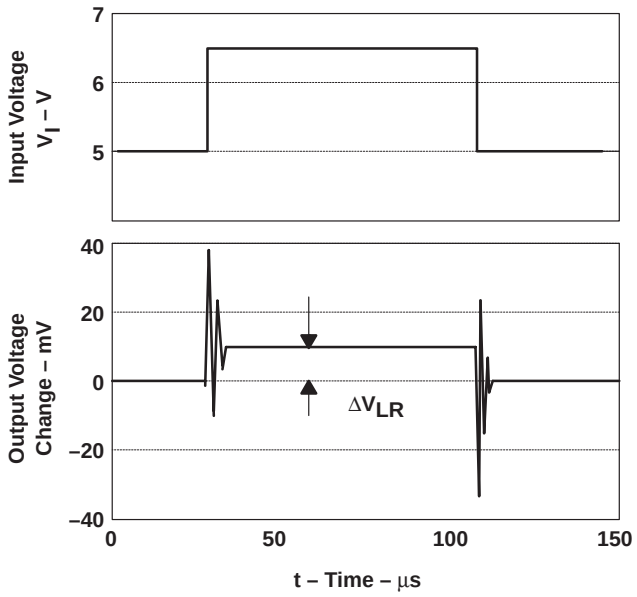


Figure 15. Line Transient Response of TPS76333

Figure 16 shows the circuit performance of the TPS76333 3.3-V LDO regulator with respect to the input voltages. The broken line shows the range of output voltage variation resulting from the input voltage change (1.244 mV to 18.81 mV).

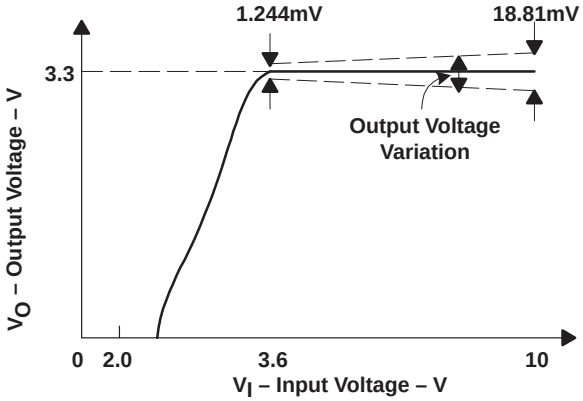


Figure 16. TPS76333 Output Voltage With Respect to Input Voltage

7 Transient Response

The transient response is an important specification, which is the maximum allowable output voltage variation for a load current step change. The transient response is a function of the output capacitor value (C_o), the equivalent series resistance (ESR) of the output capacitor, the buypass capacitor (C_b), and the maximum load-current ($I_{o,max}$). The application determines how low this value should be. The maximum transient voltage varitation is defined as follows[2].

$$\Delta V_{tr,\,max} = \frac{I_{o,max}}{C_o + C_b}\,\Delta t_1 + \Delta V_{ESR} \tag{28}$$

Where Δt_1 corresponds to the closed loop bandwidth. ΔV_{ESR} is the voltage variation resulting from the presence of the ESR (R_{ESR}) of the output capacitor. ΔV_{ESR} is proportional to R_{ESR}.

7.1 Application Implications

A LDO voltage regulator with output capacitor of 4.7 μF is shown in Figure 17.

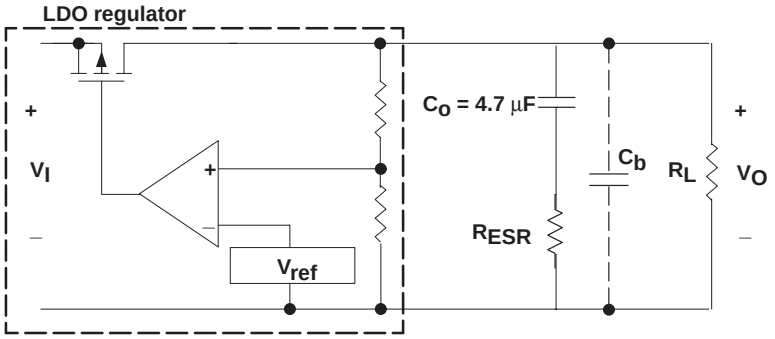


Figure 17. 1.2-V, 100-mA LDO Voltage Regulator With Output Capacitor of 4.7 μF

Figure 18 illustrates the transient response of a 1.2 V, 100 mA LDO regulator with an output capacitor of 4.7 μF shown in Figure 17. A step change of load current (near 90 mA) was applied to the regulator which is shown in the upper trace of the figure. It is noted that in the lower trace the output voltage drops approximately 120 mV and then the voltage control loop begins to respond to the step load change in 1 μs (Δt_1 = 1 μs). Finally, the output voltage reaches to a stble state within 17 μs. From equation 28, the calculated maximum voltage variation is given by:

$$\Delta V_{tr,\,max} = \frac{90\ mA}{4.7\ \mu F + 0} \times 1\ \mu s + \Delta V_{ESR} = 19\ mV + \Delta V_{ESR} = 120\ mV \tag{29}$$

Therefore, the output voltage variation of 101 mV is caused by the ΔV_{ESR}. The effects of ΔV_{ESR} can be reduced by adding bypass capacitors shown in Figure 17, which normally exhibit low ESR value.

To decrease the voltage variation resulting from the load transient, a big value of output capacitor and the low ESR of the capacitor are recommended. However, the *Tunnel of Death* (discussed in section 9) limits the values of output capacitor and its ESR value.

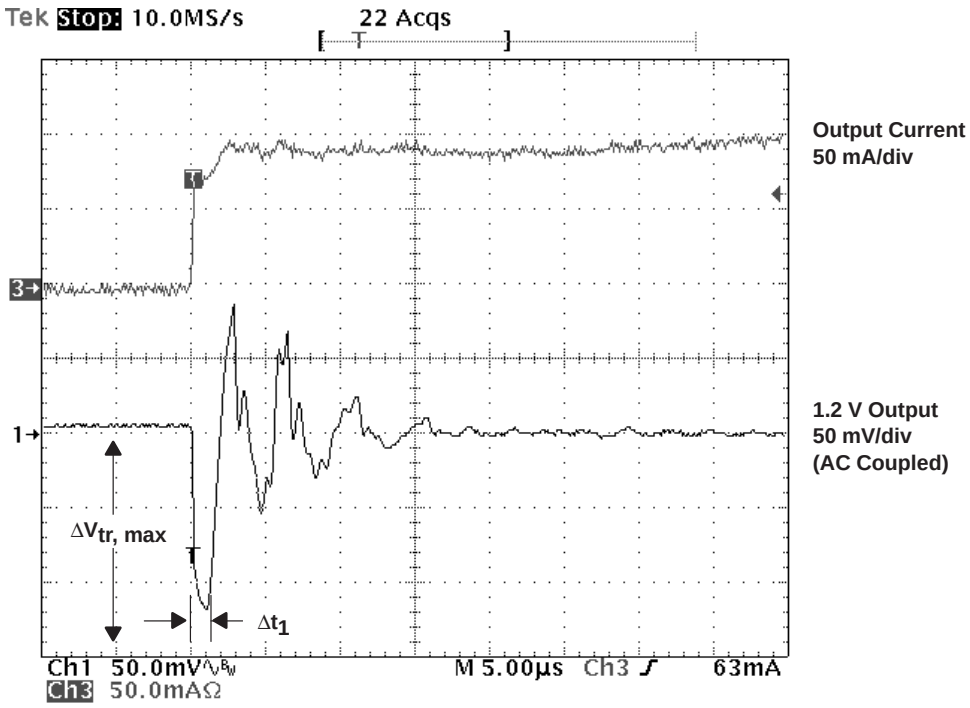


Figure 18. Transient Response of Step Load Change of 1.2-V, 100-mA LDO Voltage Regulator With an Output Capacitor C_O=4.7 µF

8 Frequency Response

Figure 19 shows the essential elements of a linear regulator.[2] The error amplifier is modeled by a transconductor (g_a) with a load comprised of capacitor C_{par} and resistor R_{par}. The series pass element (MOS transistor) is modeled by a small signal model with transconductance g_p. An output capacitor C_o with an equivalent series resistor (R_{ESR}) and a bypass capacitor C_b is added.

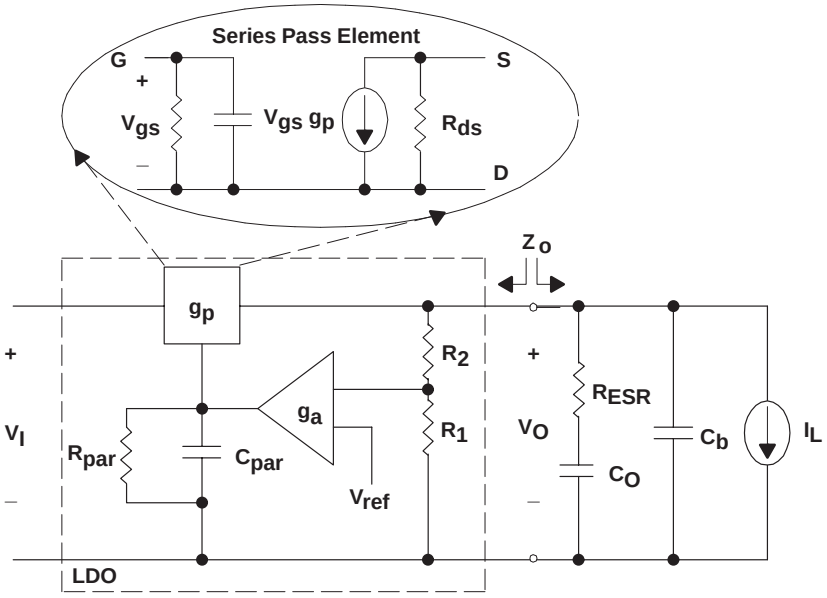


Figure 19. AC Model of a Linear Regulator

From Figure 19, the output impedance is given by

$$Z_o = R_{12p} \left\| \left(R_{ESR} + \frac{1}{SC_o} \right) \right\| \frac{1}{SC_b} \tag{30}$$

$$= \frac{R_{12p}\left(1 + SR_{ESR}C_o\right)}{S^2 R_{12p} R_{ESR} C_o C_b + S\left[\left(R_{12p} + R_{ESR}\right)C_o + R_{12p}C_b\right] + 1}$$

Where $R_{12p} = R_{ds} \| \left(R_1 + R_2\right) \approx R_{ds}$ (31)

Typically, the output capacitor value C_o is considerably larger than the bypass capacitor C_b. Thus, the output impedance Z_o approximates to

$$Z_o \approx \frac{R_{ds}\left(1 + SR_{ESR}C_o\right)}{\left[1 + S\left(R_{ds} + R_{ESR}\right)C_o\right] \times \left[1 + S\left(R_{ds} \| R_{ESR}\right)C_b\right]} \tag{32}$$

From equation (32), a part of the overall open-loop transfer function for the regulator is obtained, and the zero and poles can be found. The first pole is

$$P_o; \quad S\left(R_{ds} + R_{ESR}\right)C_o = -1$$

$$\textit{Therefore}, \; f_{po} = \frac{-1}{2\pi\left(R_{ds} + R_{ESR}\right)C_o} \simeq \frac{-1}{2\pi R_{ds} C_o} \left(\textit{Because } R_{ds} \gg R_{ESR}\right) \tag{33}$$

The second pole is obtained from equation (32) again,

$$P_b; \quad S\left(R_{ds} \parallel R_{ESR}\right)C_b = -1 \tag{34}$$

$$\textit{Therefore}, \; f_{pb} = \frac{-1}{2\pi\left(R_{ds} \parallel R_{ESR}\right)C_b} \approx \frac{-1}{2\pi R_{ESR}C_b} \tag{35}$$

The zero is

$$Z_{ESR}; \quad SR_{ESR}C_o = -1 \tag{36}$$

$$\textit{Therefore}, \; f_{Z(ESR)} = \frac{-1}{2\pi R_{ESR}C_o} \tag{37}$$

In addition, another pole exists from the input impedance of the pass element (i.e. the output impedance of the amplifier, R_{par}, C_{par}). The approximated poles and the zero are then given by

$$P_o \approx \frac{1}{2\pi R_{ds}C_o} \approx \frac{I_L}{2\pi V_A C_o} \tag{38}$$

$$P_b \approx \frac{1}{2\pi R_{ESR}C_b} \tag{39}$$

$$P_a \approx \frac{1}{2\pi R_{par}C_{par}} \tag{40}$$

$$\text{and} \quad Z_{ESR} \approx \frac{1}{2\pi R_{ESR}C_o} \tag{41}$$

Where $R_{ds} \approx \frac{V_A}{I_L}$, $V_A = \frac{1}{\lambda}$ for MOS device, λ is the channel-length modulation parameter. Pole P_a is the only one introduced at the input of the pass device, not at the output of the device. Figure 20 illustrates the typical frequency response of the LDO voltage regulator.

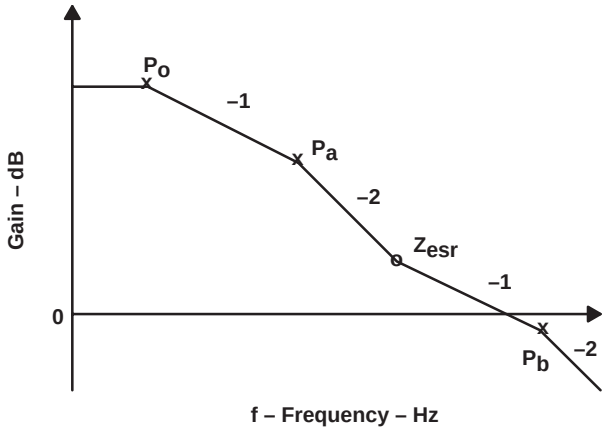


Figure 20. Frequency Response of the LDO Voltage Regulator

9 Range of Stable ESR (Tunnel of Death)

An LDO regulator would require an output capacitor with an output equivalent series resistor (ESR) to stabilize the control loop. An LDO has two poles that can cause oscillations as shown in Figure 21 if it is not compensated. It is obvious that the linear regulator is unstable because the phase shift at unity gain frequency (UGF) is –180° due to the effects of two poles (P_o, P_a) at low frequencies. To make the regulator stable, a zero must be added, which will cancel out the phase effect of one of two poles.

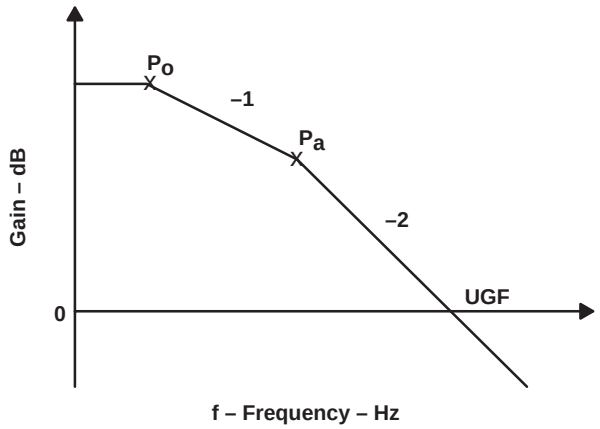


Figure 21. LDO Frequency Response Without Compensation

The equivalent series resistance of the output capacitor (ESR) or a compensated series resistor (CSR) is used for the zero. Figure 22 shows how the ESR (or CSR) zero stabilizes the control loop. The zero produced by the ESR locates before the UGF so that the phase shift at UGF_1 will be around –90° (i.e., two poles –zero = -180°+90° = -90°). Thus, the linear regulator becomes stable. The phase shift of the control loop at UGF should always be less than –180° for system stability.

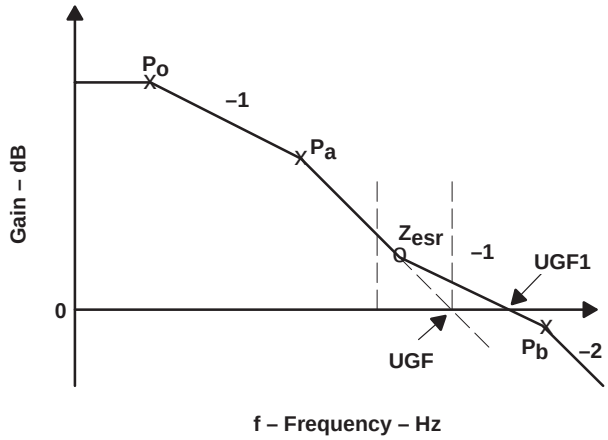


Figure 22. LDO Frequency Response With External Compensation

The ESR value should be maintained in the range that determines the loop stability. For most LDO regulators, minimum and maximum ESR values exist. Figures 23 and 24 show the unstable loop responses of an LDO regulator even though a zero is added. From equation (39) and (41), the zero Z_{esr} and the pole P_b are determined by the equivalent series resistor (ESR). When the ESR changes, Z_{esr} and P_b are shifted upward/downward and the loop stability is affected.

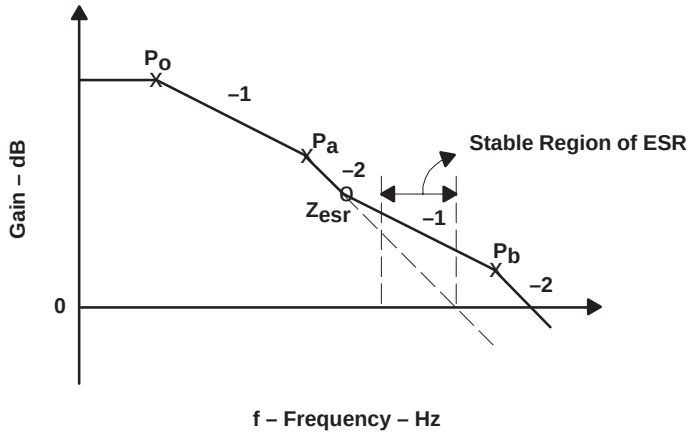


Figure 23. Unstable Frequency Response of LDO With too High ESR

Figure 23 illustrates the unstable frequency response of an LDO when too high an ESR is added, and Figure 24 illustrates the LDO frequency response when too low an ESR is used. For both cases, the total phase shift at unity gain frequency is –180°, resulting in system instability. The broken line in Figures 23 and 24 shows the stable range of Z_{esr}.

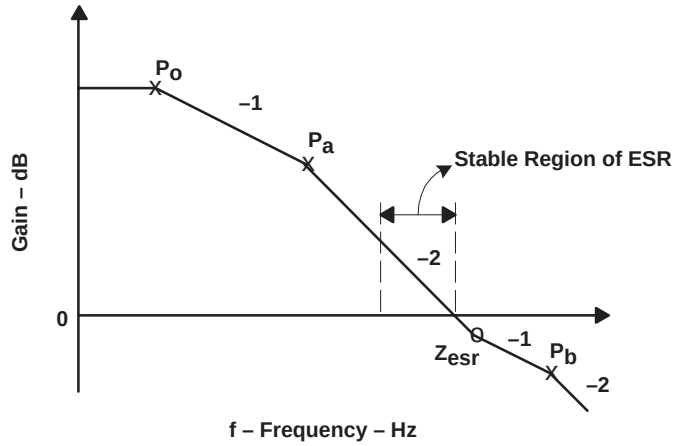


Figure 24. Unstable Frequency Response of LDO With too Low ESR

9.1 Application Implications

Since ESR can cause instability, LDO manufacturers typically provide a graph showing the stable range of ESR values. Figure 25 shows a typical range of ESR values with respect to the output currents. This curve is called tunnel of death. The curve shows that the ESR must be between 0.2 Ω and 9 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the ESR requirements.

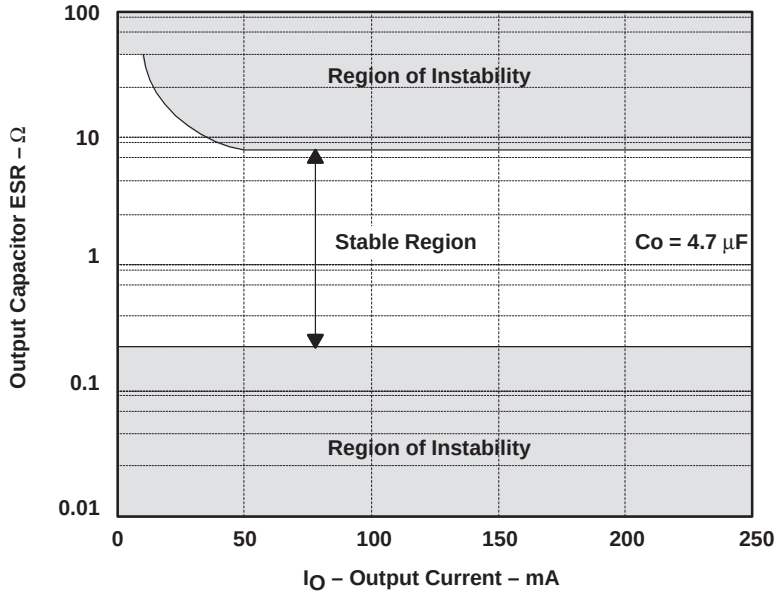


Figure 25. Range of Stable ESR Values

10 Accuracy

Accuracy specifies all effects of line regulation (ΔV_{LR}), load regulation (ΔV_{LDR}),reference voltage drift ($\Delta V_{o,ref}$), error amplifier voltage drift ($\Delta V_{o,a}$), external sampling resistor tolerance ($\Delta V_{o,r}$), and temperature coefficient (ΔV_{TC}). It can be defined by

$$Accuracy \approx \frac{|\Delta V_{LR}| + |\Delta V_{LDR}| + \sqrt{\Delta V_{o,ref}^2 + \Delta V_{o,a}^2 + \Delta V_{o,r}^2 + \Delta V_{TC}^2}}{V_o} \times 100 \quad (42)$$

Output voltage variation in a regulated power supply is due primarily to temperature variation of the constant voltage reference source and temperature variation of the difference amplifier characteristics as well as the sampling resistor tolerance. Load regulation, line regulation, gain error, and offsets normally account for 1% to 3% of the overall accuracy.

Output voltage variations resulting from the reference voltage drift, error amplifier voltage drift, and sampling resistor tolerance that are due to inter-lot and process variations are detailed in this section.

10.1 Reference Voltage Drift

Assume the LDO regulator exhibits the reference voltage drift (V_d) as shown in Figure 26. The reference voltage drift directly causes the output voltage change ($\Delta V_{o,ref}$).

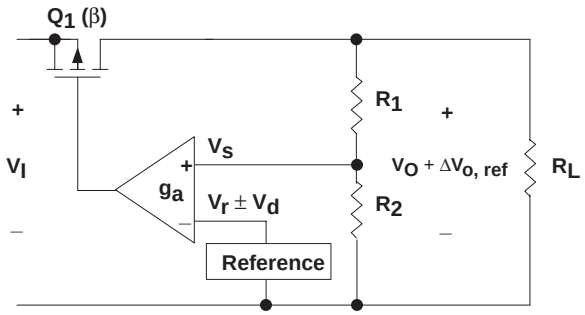


Figure 26. LDO With Reference Voltage Drift

Thus, the resultant output voltage is

$$V_o + \Delta V_{o,ref} = \left[V_s - \left(V_r \pm V_d\right)\right] g_a \beta R_L \tag{43}$$

The sensed voltage V_S is given by

$$V_s = \frac{R_2}{R_1 + R_2}\left(V_o + \Delta V_{o,ref}\right) \tag{44}$$

Substituting equation (44) into equation (43),

$$\begin{aligned} V_o + \Delta V_{o,ref} &= \left[\frac{R_2}{R_1 + R_2}\left(V_o + \Delta V_{o,ref}\right) - \left(V_r \pm V_d\right)\right] g_a \beta R_L \\ &= \frac{\left(R_1 + R_2\right)\left(-V_r \mp V_d\right) g_a \beta R_L}{R_1 + R_2 - R_2 g_a \beta R_L} \end{aligned} \tag{45}$$

Now in the usual case,

$$g_a \beta V_s \gg 1 \tag{46}$$

From equation (45) and (46), the output voltage is obtained.

$$V_o + \Delta V_{o,ref} = \frac{R_1 + R_2}{R_2}\left(V_r \pm V_d\right) \tag{47}$$

Now, the right hand side of the equation can be split into two parts. One is the average output voltage and the other is the function of the reference voltage drift. The average output voltage is then given by

$$V_o = \frac{\left(R_1 + R_2\right)}{R_2} V_r \tag{48}$$

Thus, the output voltage variation resulting from reference voltage drift is obtained from equation (47).

$$\Delta V_{o,ref} = \frac{R_1 + R_2}{R_2}\left(\pm V_d\right) \tag{49}$$

From equations (48) and (49), the following equation is obtained.

$$\frac{\Delta V_{o,ref}}{V_O} = \pm \frac{V_d}{V_r} \tag{50}$$

Equation (50) shows that the output voltage variation is directly affected by the accuracy of the reference voltage. If the reference voltage accuracy is 1%, then the output voltage of the regulator will exhibit the same percentage of variation.

10.2 Error Amplifier Voltage Drift

The error amplifiers exhibit drift characteristics with temperature. Assume that an error (or drift) voltage V_d appears at the output of the amplifier as shown in Figure 27.

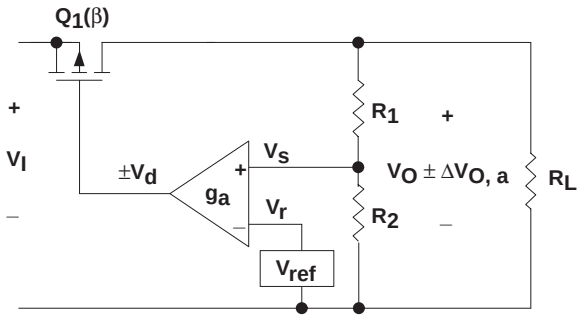


Figure 27. LDO With Error Amplifier Voltage Drift

The output change $\Delta V_{o,a}$ resulting from the drift voltage V_d is obtained from Figure 27.

$$\Delta V_{o,a} = \beta V_d R_L \pm g_a \beta \Delta V_s R_L \tag{51}$$

The sensed voltage ΔV_S is given by

$$\Delta V_s = \frac{R_2}{R_1 + R_2} \Delta V_{o,a} \tag{52}$$

Substituting equation (52) into equation (51)

$$\Delta V_{o,a} = \frac{\beta V_d (R_1 + R_2) R_L}{R_1 + R_2 \pm g_a \beta R_2 R_L} \tag{53}$$

By equation (46), the output voltage variation resulting from the error amplifier voltage drift is obtained as follows.

$$\Delta V_{o,a} = \pm \frac{V_d (R_1 + R_2)}{g_a R_2} \tag{54}$$

10.3 Tolerance of External Sampling Resistors

For adjustable regulators, the output depends on the accuracy of two sampling resistors. Suppose that the sampling resistors of an LDO regulator have tolerances such as $\pm\Delta R_1$ and $\pm\Delta R_2$ as shown in Figure 28.

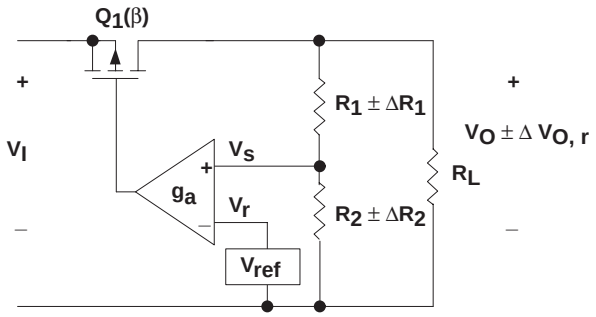


Figure 28. LDO With Sampling Resistors

The output voltage change resulting from the sampling resistor tolerance is

$$V_o + \Delta V_{o,r} = g_a \beta (V_s - V_r) R_L \tag{55}$$

The sensed voltage V_S is given by

$$V_s = \frac{\left(R_2 \pm \Delta R_2\right)}{\left(R_1 \pm \Delta R_1\right) + \left(R_2 \pm \Delta R_2\right)} \left(V_o + \Delta V_{o,r}\right) \tag{56}$$

Substituting V_S into equation (55)

$$V_o + \Delta V_{o,r} = \frac{-g_a \beta V_r \left[\left(R_1 \pm \Delta R_1\right) + \left(R_2 \pm \Delta R_2\right)\right] R_L}{\left(R_1 \pm \Delta R_1\right) + \left(R_2 \pm \Delta R_2\right) - g_a \beta \left(R_2 \pm \Delta R_2\right) R_L} \tag{57}$$

By equation (46), the output voltage resulting from the tolerance of the sampling resistors is obtained as follows.

$$V_o + \Delta V_{o,r} = \frac{\left(R_1 \pm \Delta R_1\right) + \left(R_2 \pm \Delta R_2\right)}{\left(R_2 \pm \Delta R_2\right)} V_r \tag{58}$$

Thus, the average output voltage is given by

$$V_o = \frac{R_1 + R_2}{R_2 \pm \Delta R_2} V_r \tag{59}$$

The average output voltage is a function of the resistor accuracy. Specifically, the bottom side of the resistor dominates the overall LDO accuracy. The output voltage variation due to the resistor tolerance is given by.

$$\Delta V_{o,r} = \pm \frac{\Delta R_1 + \Delta R_2}{R_2 \pm \Delta R_2} V_r \tag{60}$$

10.4 Application Implications—an Example

What is the total accuracy of the 3.3-V LDO regulator shown in Figure 29 over the temperature span from 0° to 125° with the following operating characteristics?

- Temperature coefficient is 100 ppm/°C.
- Sampling resistor tolerance is 0.25%.
- Output voltage change resulting from load regulation, and line regulation are ±5 mV, and ±10 mV, respectively.

- Accuracy of the reference is 1%.

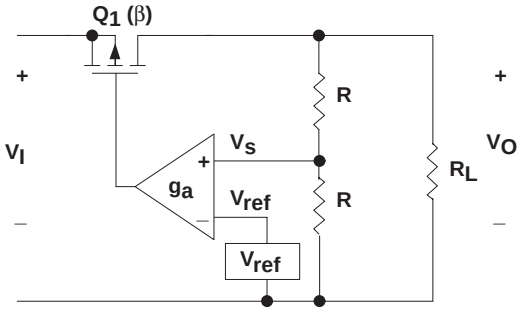


Figure 29. LDO Regulator

The output voltage is given by

$$V_o = \frac{R + R}{R}\ V_{ref} = 2\ V_{ref} \tag{61}$$

Therefore, the reference voltage V_{ref} is half of the output voltage (i.e. V_{ref} = 3.3/2[V]), and

$$\begin{aligned} \Delta V_{TC} &= Temperature\ Coefficient \times \left(T_{max} - T_{min}\right) \times V_o \\ &= (100\ ppm/^{\circ}C)\ (125^{\circ}C)\ (3.3\ V)\ =\ 41.2\ mV \\ \Delta V_{o,r} &= (0.25\%\ of\ V_o + 0.25\%\ of\ V_o)\ V_{ref} \\ &= (0.005)\ (3.3)\ \frac{3.3}{2} = 27\ mV \end{aligned} \tag{62}$$

From equation (49), the output voltage variation resulting from the reference voltage is obtained as follows.

$$\Delta V_{o,ref} = 2\left(\frac{3.3}{2}\right)0.01 = 33\ mV \tag{63}$$

Where

$$V_d = V_{ref} \times 0.01 = \left(\frac{3.3}{2}\right) \times 0.01$$

Therefore, the overall accuracy of the LDO is obtained as follows,

$$Accuracy \approx \frac{10\ mV + 5\ mV + \sqrt{(33\ mV)^2 + (27\ mV)^2 + (41.2\ mV)^2}}{3.3\ V} \times 100 \approx 2.25\% \tag{64}$$

11 References

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