User's Guide

TPS546A24A SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS546A24AEVM-1PH evaluation module (EVM). The user's guide includes test information, descriptions, and results. A complete schematic diagram, printed-circuit board layouts, and bill of materials are also included in this document. Throughout this user's guide, the abbreviations EVM, TPS546A24AEVM-1PH, and the term evaluation module are synonymous with the TPS546A24AEVM-1PH, unless otherwise noted.

Trademarks

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1 Description

The TPS546A24AEVM-1PH evaluation module uses the TPS546A24A device in a buck design. It designed for a nominal 12-V bus and to produce a regulated 1.2-V output at up to 10 A of load current. The TPS546A24AEVM-1PH provides a number of test points to evaluate the performance of the devices.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS546A24AEVM-1PH. Observe all safety precautions.

Warning The TPS546A24AEVM-1PH circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces, or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the battery- potential of the EVM.

1.2 Typical Applications

The TPS546A24A device is designed for the following applications:

- High-density power solutions
- Wireless infrastructure
- Switcher
- Router network
- Server
- Storage
- Smart power systems

1.3 Features

This EVM has the following features:

- Regulated 1.2-V output up to 10-A_{DC} steady-state output current
- The output voltage is marginable and trimmable using the PMBus interface
  - Programmable UVLO, soft-start, and enable via the PMBus interface
  - Programmable overcurrent warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable overvoltage and undervoltage warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable turn-on and turn-off delays
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 2-1 lists the electrical performance specifications in room temperature (20 to 25°C). Characteristics are given for an input voltage of VIN = 12 V, unless otherwise specified.

Table 2-1. TPS546A24AEVM-1PH Electrical Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input Characteristics					
Input voltage range, V_{IN}		5	12	18	V
Full load input current	I_{OUT} = 10 A		1.13		A
Full load input current	V_{IN} = 5 V, I_{OUT} = 10 A		2.6		A
No load input current	I_{OUT} = 0 A, switching enabled		65		mA
Enable switching threshold	Set by default resistor divider, JP4 pins 3 and 4 shorted		4.7		V
Disable switching threshold	Set by default resistor divider, JP4 pins 3 and 4 shorted		4.22		V
Output Characteristics					
Output voltage, V_{OUT}			1.2		V
Output load current, I_{OUT}		0		10	A
Output voltage regulation	Line Regulation: V_{IN} = 5 V to 18 V		0.1%		
	Load Regulation: I_{OUT} = 0 A to 10 A		0.1%		
Output voltage ripple	I_{OUT} = 10 A		7		mVpp
Output voltage undershoot	I_{OUT} = 2.5-A to 7.5-A step at 10 A/µs		90		mV
Output voltage overshoot	I_{OUT} = 7.5-A to 2.5-A step at 10 A/µs		90		mV
Output overcurrent fault threshold	Phase current limit programmed by MSEL2		14		A
Systems Characteristics					
Switching frequency	Programmed by MSEL1		650		kHz
Full load efficiency, V_{OUT} (1)	I_{OUT} = 10 A		89.2%		
Operating case temperature	I_{OUT} = 10 A, 10 minute soak		37		°C
Loop bandwidth	I_{OUT} = 10 A		37		kHz
Phase margin			61		°
PMBus Interface and Pin-Strapping					
PMBus address	Programmed by NVM and ADRSEL		36		Decimal
Voltage reference	Default setting of VOUT_COMMAND programmed by VSEL		1.2		V
Soft-start time (TON_RISE)	Default setting of TON_RISE programmed by MSEL2		3		ms

(1) The efficiency is measured using the test points listed in Table 6-1 to minimize the effect of DC drops caused by onboard copper traces.

3 Schematic

Figure 3-1 through Figure 3-2 illustrate the TPS546A24AEVM-1PH schematics.

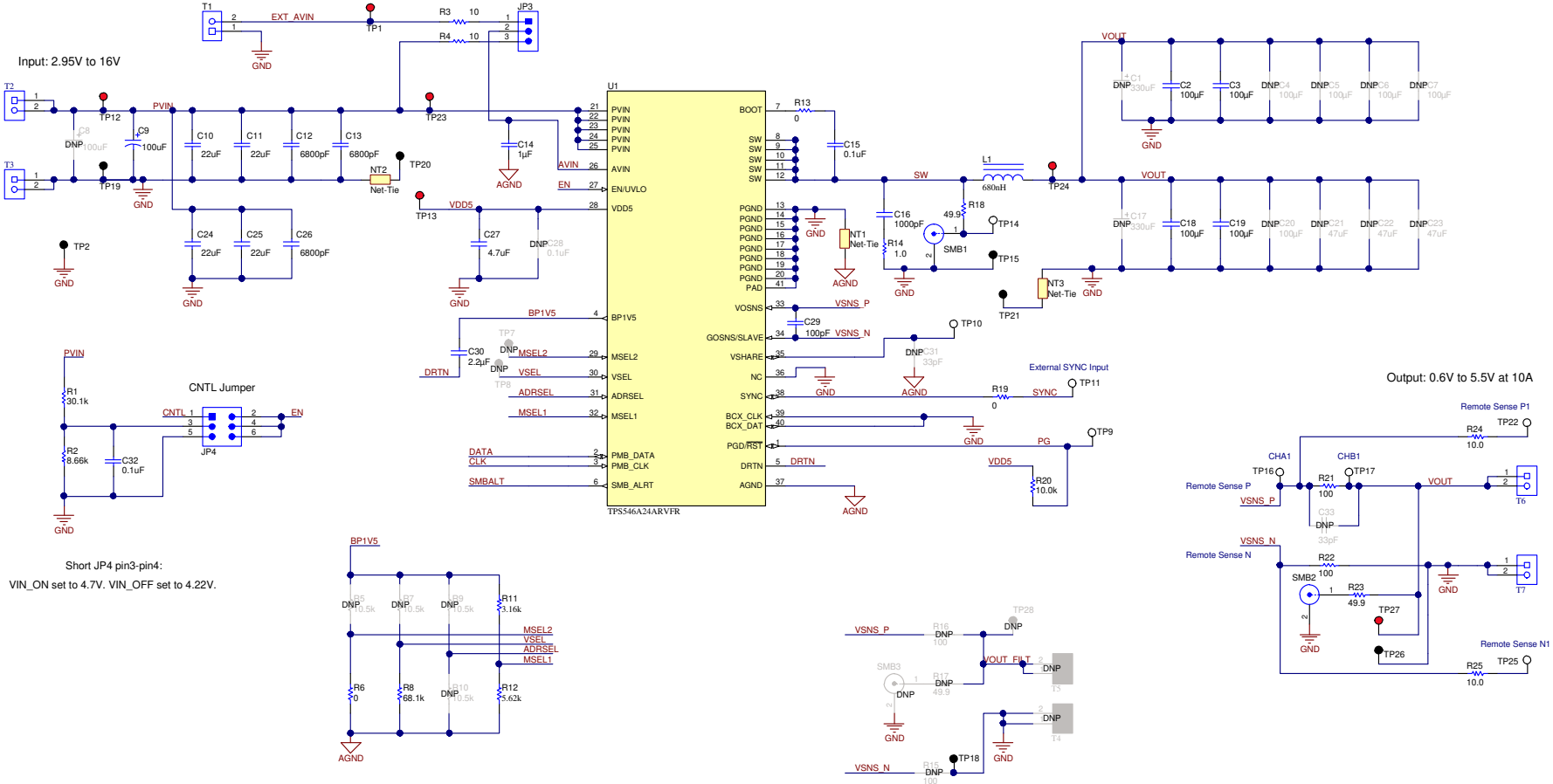


Figure 3-1. TPS546A24AEVM-1PH Schematic - Main Circuit

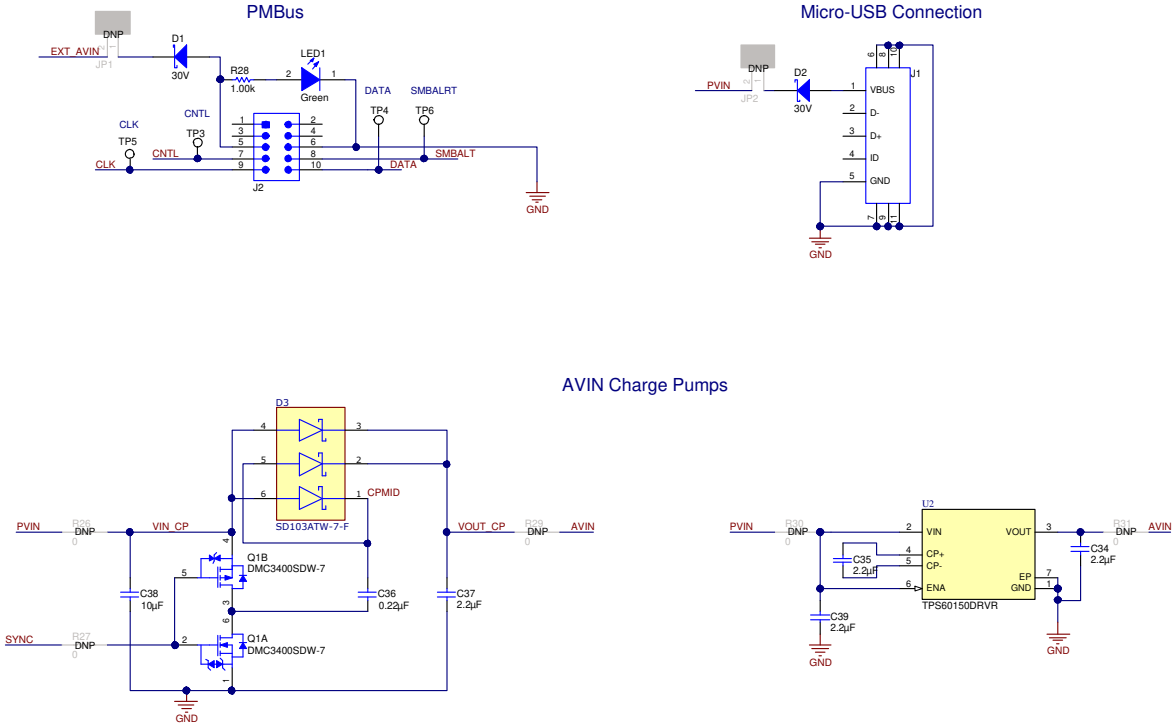


Figure 3-2. TPS546A24AEVM-1PH Schematic - Connectors and Charge Pumps

4 Test Setup

4.1 Test and Configuration Software

To change any of the default configuration parameters on the EVM through PMBus, obtain the *TI Fusion Digital Power Designer* software.

4.1.1 Description

The *TI Fusion Digital Power Designer* is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPS546A24A power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter described in Section 4.2.6.

4.1.2 Features

Some of the tasks you can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data. Items such as input voltage, output voltage, output current, die temperature, and warnings and faults that are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as V_{OUT} trim and margin, UVLO, soft-start time, warning and fault thresholds, fault response, and On/Off modes.

4.2 Test Equipment

4.2.1 Voltage Source

The input voltage source V_{IN} should be a 0-V to 20-V variable DC source capable of supplying a minimum of 3 A_{DC} to support 10-A load with 5-V input. Connect input VIN and GND to T2 and T3. If the output voltage of the EVM is increased, the power supply may need to be capable of supplying more current.

4.2.2 Multimeters

TI recommends using two separate multimeters: one meter to measure V_{IN} and the other to measure V_{OUT}.

4.2.3 Output Load

A variable electronic load is recommended for the test setup. To test the full load current this EVM supports, the load should be capable of sinking at least 10 A.

4.2.4 Oscilloscope

When using an oscilloscope to measure the switching node voltage or voltage ripple, measure using a *Tip-and-Barrel* method as Figure 4-1 shows, or better.

4.2.5 Fan

During prolonged operation at high loads, it may be necessary to provide forced air cooling with a small fan aimed at the EVM. Maintain the surface temperature of the devices on the EVM below their rated temperature.

4.2.6 USB-to-GPIO Interface Adapter

A communications adapter is required between the EVM and the host computer. This EVM is designed to use TI's USB-to-GPIO Adapter. Purchase this adapter at http://www.ti.com/tool/usb-to-gpio.

4.2.7 Recommended Wire Gauge

- Input VIN and GND to T2 and T3 (GND) (12-V input) – The recommended wire size is AWG #18 or better, with the total length of wire less than 2 feet (1 foot input, 1 foot return).
- Output T6 and GND T7 (1.2-V output) – The recommended wire size is AWG #16 or better, with the total length of wire less than 2 feet (1 foot output, 1 foot return). A thicker wire gauge may be required to minimize the voltage drop in the wires.

4.3 Tip and Barrel Measurement

Figure 4-1 illustrates the tip and barrel measurement for switching node waveform on TP14 with TP15.

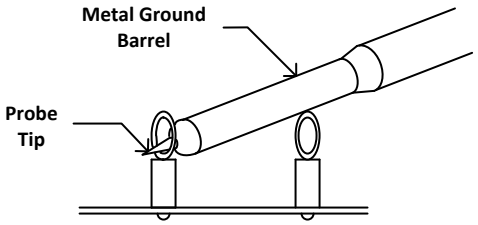


Figure 4-1. Tip and Barrel Measurement

4.4 List of Test Points, Jumpers, and Connectors

Table 4-1 lists the test point functions.

Table 4-1. Test Point Functions

Test Point	Type	Name	Description
TP1	T-H Loop	EXT_AVIN	AVIN measurement point
TP2	T-H Loop	GND	GND reference
TP3	T-H Loop	CNTL	CNTL signal on J2 header
TP4	T-H Loop	DATA	DATA signal on J2 header
TP5	T-H Loop	CLK	CLK signal on J2 header
TP6	T-H Loop	SMBALRT	SMBALERT signal on J2 header
TP7	T-H Loop	MSEL2	MSEL2 measurement point for U1
TP8	T-H Loop	VSEL	VSEL measurement point for U1
TP9	T-H Loop	PG	PGOOD signal of U1
TP10	T-H Loop	VSHARE	VSHARE measurement point. Sensitive signal
TP11	T-H Loop	SYNC	External SYNC input
TP12	T-H Loop	PVIN	VIN+ measurement point
TP13	T-H Loop	VDD5	VDD5 measurement point or external VDD5 input
TP14	T-H Loop	SW	Switching node, reference to TP15
TP15	T-H Loop	GND	GND reference for switch node measurement
TP16	T-H Loop	CH_A	INPUT for small signal loop gain measurements (B/A setup)
TP17	T-H Loop	CH_B	OUTPUT for small signal loop gain measurements (B/A setup)
TP18	T-H Loop	GND	GND reference
TP19	T-H Loop	GND	VIN- measurement point
TP20	T-H Loop	GND	GND reference for U1 PVIN for efficiency measurement
TP21	T-H Loop	GND	GND reference for VOUT for efficiency measurement
TP22	T-H Loop	Remote SNS+	OUTPUT remote sense + voltage point
TP23	T-H Loop	PVIN_EFF	PVIN pin voltage of U1 measurement point for efficiency, reference to TP20
TP24	T-H Loop	VOUT_EFF	VOUT measurement point for efficiency, reference to TP21
TP25	T-H Loop	Remote SNS-	OUTPUT remote sense - voltage point
TP26	T-H Loop	GND	VOUT - measurement point
TP27	T-H Loop	VOUT	VOUT + measurement point
TP28	T-H Loop	VOUT_FILT	VOUT_FILT measurement point when using second stage filter

Table 4-2 lists the EVM jumpers.

Table 4-2. Jumpers

Jumper	Type	Name	Description
JP1	Header, 100 mil, 2 × 1	Micro_USB-PVIN	Short to connect PVIN to Micro USB connector
JP2	Header, 100 mil, 2 × 1	PMBus3.3V-AVIN	Short to connect USB-to-GPIO 3.3V to AVIN
JP3	Header, 100 mil, 3 × 1	AVIN Select	AVIN input source selections

Table 4-2. Jumpers (continued)

Jumper	Type	Name	Description
JP4	Header, 100 mil, 3 × 2	EN Select	EN/UVLO pin selections

Table 4-3 lists the options for the EN/UVLO pin selection.

Table 4-3. JP4 Selections

Shunt Position	Selection
pin 1 to 2 shorted	PMBus adaptor control signal
pin 3 to 4 shorted	Resistor divider to PVIN
pin 5 to 6 shorted	EN/UVLO short to ground

Table 4-4 lists the options for the AVIN selection.

Table 4-4. JP3 Selections

Shunt Position	Selection
pin 1 to 2 shorted	AVIN pin connected to AVIN input through 10-Ω resistor. Use this selection when testing with a split rail input.
pin 2 to 3 shorted	AVIN pin connected to PVIN through 10-Ω resistor

Table 4-5 lists the EVM connector functions.

Table 4-5. Connector Functions

Connector	Type	Name	Description
J1	Micro USB	Micro USB	Micro USB connector to power EVM from a 5 V USB source
J2	Header, 100 mil, 5 × 2	PMBus connector	PMBus socket for TI FUSION adaptor
T1	Terminal block, 2 × 1	Ext_AVIN	External AVIN connector
T2	Terminal block, 2 × 1	PVIN	VIN+ connector
T3	Terminal block, 2 × 1	GND	VIN– connector
T4	Terminal block, 2 × 1	GND	VOUT_FILT- connector
T5	Terminal block, 2 × 1	VOUT_FILT	VOUT_FILT+ connector
T6	Terminal block, 2 × 1	VOUT	VOUT+ connector
T7	Terminal block, 2 × 1	GND	VOUT– connector

4.5 Evaluating Split Rail Input

The default configuration of the EVM is for single rail input. Split rail input enables operation with 3.3V PVIN. For split rail operation, configure the jumpers on the EVM as follows:

1. Move the jumper JP3 to position 1-2 to disconnect the AVIN pin from the PVIN pin.
2. Apply the AVIN input to T1. 4-V or greater AVIN is required to bring the VDD5 voltage high enough to enable conversion.
3. If operation with 3.3-V PVIN is needed and the EN Select jumper (JP4) is in position 3-4, the resistor divider at the EN/UVLO will need to be changed. Alternately move the EN Select jumper to position 1-2 and use the control signal to enable conversion or use the *On/Off Config* and *OPERATION* commands to enable conversion.

4.6 Configuring EVM to Overdrive VDD5

The EVM has a testpoint TP13 that can be used to overdrive VDD5. Externally applying VDD5 is useful to minimize the power dissipation in the TPS546A24A IC when using a single rail input by moving the loss from the internal LDO of the TPS546A24A to the external supply connected to TP13.

To overdrive the internal LDO, ensure the VDD5 output of the TPS546A24A is set below the external supply voltage connected from TP13 to ground (e.g. TP2).

4.7 Powering from a Single 3.3-V Input Power Supply

The EVM includes two charge pump options to enable powering the TPS546A24A from a single 3.3-V input supply. The operation of these charge pumps is discussed in the application note Powering the TPS546D24A Device Family from a Single 3.3-V Input Power Supply.

Before following the instructions below to use one of the charge pump circuits, it is first necessary to modify the conditions that enable power conversion. By default, the EVM is configured to start switching when PVIN goes above 4.7 V based on the R1 and R2 voltage divider to the EN pin. Increasing R2 from 8.66 kΩ to 16.2 kΩ sets the enable threshold to approximately 3.0 V. An alternative method is to use the Fusion GUI to change the *On/Off Config* setting to *Always Converting* such that the device is enabled whenever power is present, regardless of the state of the EN pin or the *OPERATION* command. The configuration screen is shown in Figure 10-3. Be sure to *Store Config to NVM* after writing the change to hardware such that the setting persists after power is removed and reapplied.

To use the discrete charge pump, modify the EVM as follows:

1. Modify the enable threshold or *On/Off Config* of the device as described previously.
2. Set SYNC pin as an output. This can be accomplished by doing *either* of the following:
   a. Populate ADRSEL pin-strap resistor divider with R9 = 2.05 kΩ and R10 = 10 kΩ.
   b. Use Fusion GUI to set the *SYNC_DIR* bits of the *SYNC_CONFIG* register to *01b: Enable SYNC OUT*. This register can be set from the *All Config* tab in Fusion GUI, shown in Figure 10-8. Be sure to *Store Config to NVM* after writing the change to hardware.
3. Remove the jumper JP3 to disconnect AVIN from both the external AVIN header (T1) and from PVIN.
4. Populate the resistors R26, R27, and R29 with 0-Ω resistors.
5. Apply PVIN input voltage. Note that the output voltage of the discrete charge pump will be approximately 2 x PVIN (minus two diode drops). Pay careful attention that the applied PVIN remains below 9 V such that the generated AVIN does not exceed the 18-V rating of the converter IC.

To use the charge pump IC TPS60150, modify the EVM as follows:

1. Modify the enable threshold or *On/Off Config* of the device as described previously.
2. Remove the jumper JP3 to disconnect AVIN from both the external AVIN header (T1) and from PVIN.
3. Populate the resistors R30 and R31 with 0-Ω resistors.
4. Apply PVIN input voltage. Pay careful attention that the applied PVIN remains below the 5.5-V input rating of the TPS60150 charge pump IC.

Note

Only one charge pump circuit should be connected and used at a time. Remove the 0-Ω resistors that connect the charge pump to PVIN and AVIN (and SYNC for the discrete charge pump) before connecting the other charge pump, or before testing other conditions with higher input voltages that do not require the charge pump.

5 EVM Configuration Using the Fusion GUI

The TPS546A24A IC leaves the factory pre-configured. The factory default settings for the parameters can be found in the datasheet. If configuring the EVM to settings other than the factory defaults, use the software described in Section 4.1. It is necessary to have the input voltage applied to the EVM prior to launching the software so that the TPS546A24A may respond to the GUI and the GUI can recognize the device. The default configuration for the EVM to stop converting is set by the EN/UVLO resistor divider to a nominal input voltage of 4.22 V; therefore, an input voltage less than 4.22 V should be applied to avoid any converter activity during configuration. TI recommends an input voltage of 3.3 V.

5.1 Configuration Procedure

1. Adjust the input supply to provide 3.3 VDC, current limited to 1 A.
2. Apply the input voltage to the EVM. See Section 4.2 for connections and test setup.
3. Launch the Fusion GUI software. See the screen shots in Section 10 for more information.
4. Configure the EVM operating parameters as desired.

6 Test Procedure

6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as Section 4.2 and Section 6.2 describe.
2. Set the electronic load to draw 0 A_{DC}.
3. Increase V_{IN} from 0 V to 12 V using voltage meter to measure input voltage.
4. Use the other voltage meter to measure output voltage V_{OUT}.
5. Vary the load from 0 to 10 A_{DC}. V_{OUT} should remain in regulation as defined in Table 2-1.
6. Vary V_{IN} from 5 V to 18 V. V_{OUT} should remain in regulation as defined in Table 2-1.
7. Decrease the load to 0 A.
8. Decrease V_{IN} to 0 V.

6.2 Efficiency Measurement Test Points

To evaluate the efficiency of the power train (device and inductor), it is important to measure the voltages at the correct location. This is necessary because otherwise the measurements will include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which should not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

Table 6-1 shows the measurement points for input voltage and output voltage. VIN and VOUT are measured to calculate the efficiency. Using these measurement points will result in efficiency measurements that excludes losses due to the wires and connectors as well as PCB voltage drops.

Table 6-1. Test Points for Efficiency Measurements

Test Point	Node Name	Description	Comment
TP23	PVIN	Input voltage measurement point for VIN+	This pair of test points are connected to PVIN and PGND near the pins of U1. The voltage drop between input terminal to the device pins is not included for efficiency measurement.
TP20	PGND	Input voltage measurement point for VIN– (GND)	
TP24	VOUT	Output voltage measurement point for VOUT+	This pair of test points are connected to VOUT and GND near the output inductor. The voltage drop from the output point of the inductor to the output terminals is not included for efficiency measurement.
TP21	GND	Output voltage measurement point for VOUT– (GND)	

6.3 Control Loop Gain and Phase Measurement Procedure

The TPS546A24AEVM-1PH includes a 100.0-Ω series resistor in the feedback loop for V_{OUT}. The resistor is accessible at the test points TP16 and TP17 for loop response analysis. These test points should be used during loop response measurements as the perturbation injecting points for the loop . See the description in Table 6-2.

Table 6-2. List of Test Points for Loop Response Measurements

Test Point	Node Name	Description	Comment
TP16	CH_A	Input to feedback divider of V_{OUT}	The amplitude of the perturbation at this node should be limited to less than 30 mV
TP17	CH_B	Resulting output of V_{OUT}	Bode can be measured by a network analyzer with a CH_B/CH_A configuration

Measure the loop response with the following procedure:

1. Set up the EVM as described in Section 4.2.
2. For V_{OUT}, connect the isolation transformer of the network analyzer from TP16 to TP17.
3. Connect the input signal measurement probe to TP16. Connect the output signal measurement probe to TP17.
4. Connect the ground leads of both probe channels to TP18.
5. On the network analyzer, measure the Bode as TP17/TP16 (Out/In).

7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-3 present typical performance curves for the TPS546A24AEVM-1PH. The input voltage is 12 V and the oscilloscope measurements use 20 MHz bandwidth limiting unless otherwise noted.

7.1 Efficiency

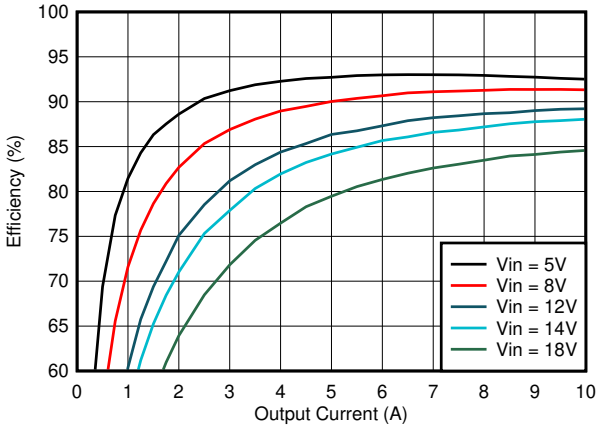


Figure 7-1. Efficiency

7.2 Load and Line Regulation (Measured Between TP27 and TP26)

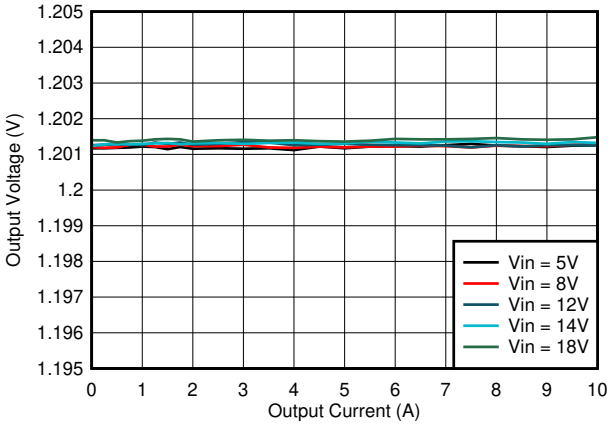


Figure 7-2. Load Regulation

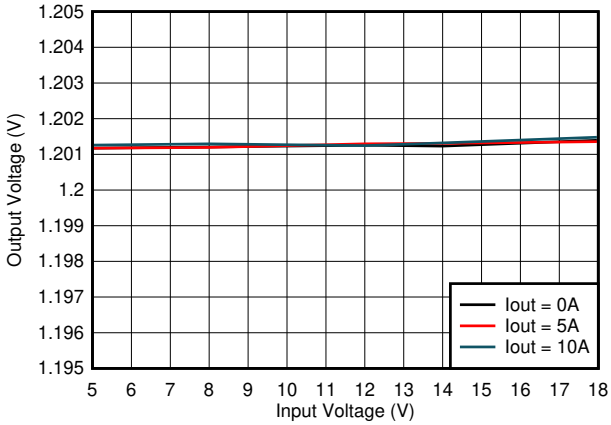


Figure 7-3. Line Regulation

7.3 Transient Response

Figure 7-4 shows the transient response waveform with a 2.5 A to 7.5 A transient at 10 A/µs

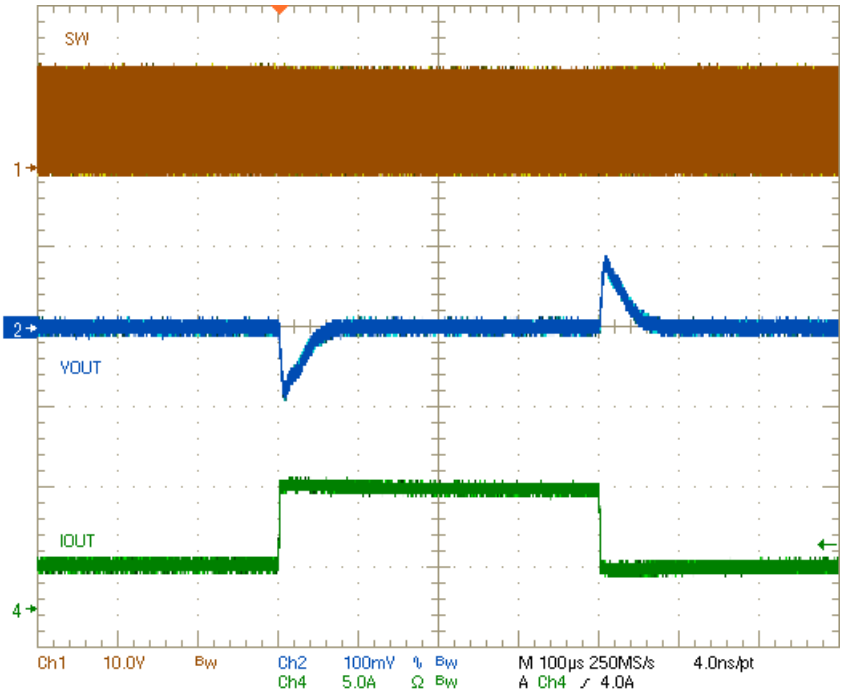


Figure 7-4. Transient Response

7.4 Control Loop Bode Plot

Figure 7-5 is the control loop bode plot.

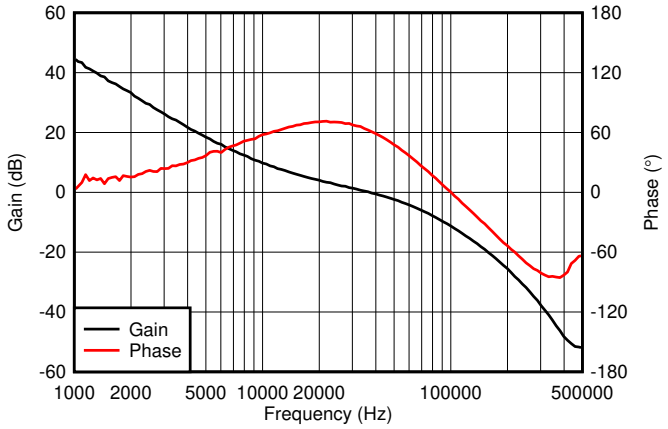


Figure 7-5. Bode Plot at 1.2-V Output at 12 V_{IN}, 10-A Load

7.5 Output Ripple

Figure 7-6 and Figure 7-7 show the output ripple waveforms at 0-A and 10-A load.

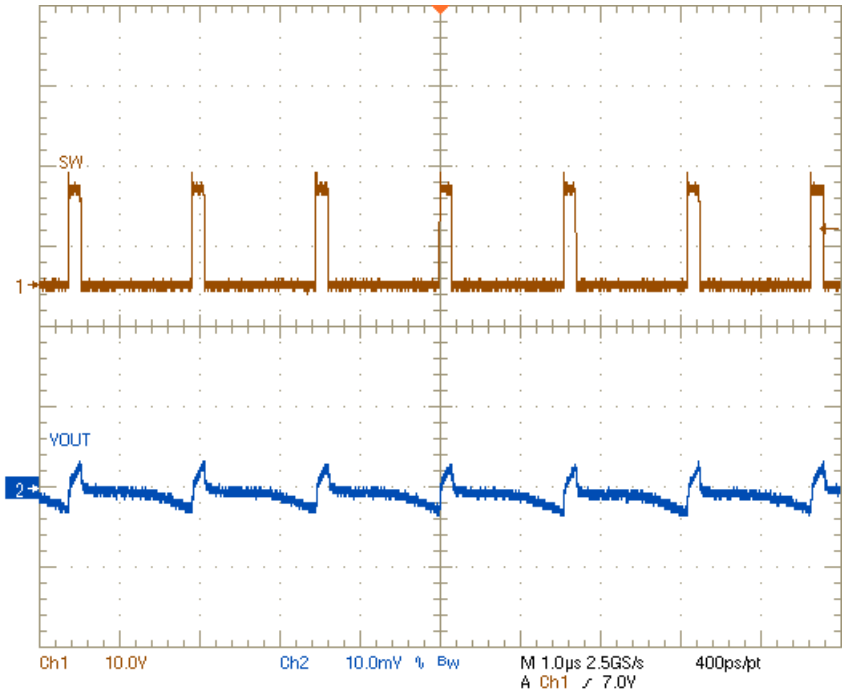


Figure 7-6. Output Ripple With 0-A Load

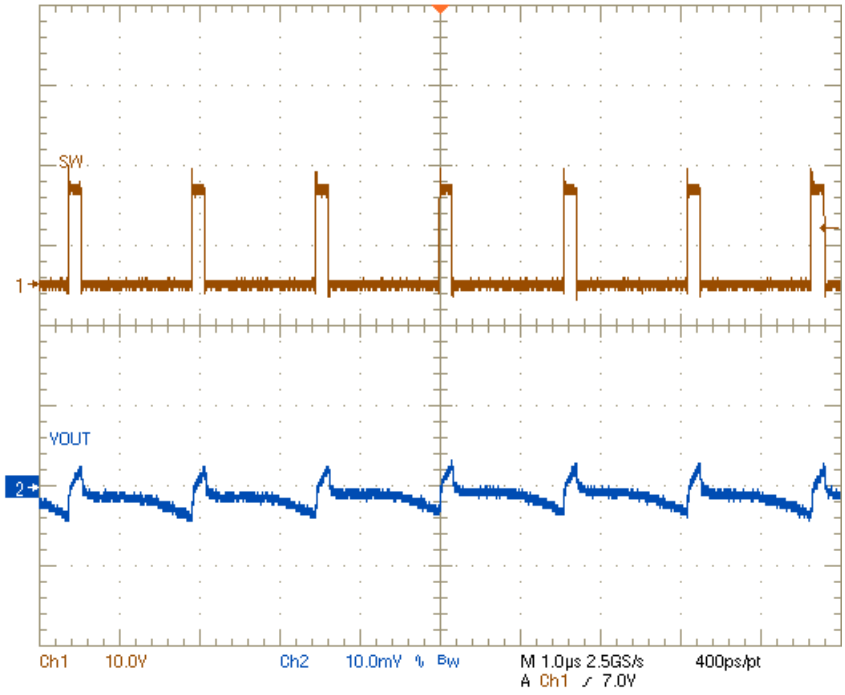


Figure 7-7. Output Ripple With 10-A Load

7.6 Power MOSFET Drain-Source Voltage

Figure 7-8 and Figure 7-9 show the low-side and high-side MOSFET drain-source voltage (V_{DS}) at 10-A load. The voltage is measured with 1-GHz bandwidth and at the solder mask openings near the U1 IC using a 1-GHz differential probe.

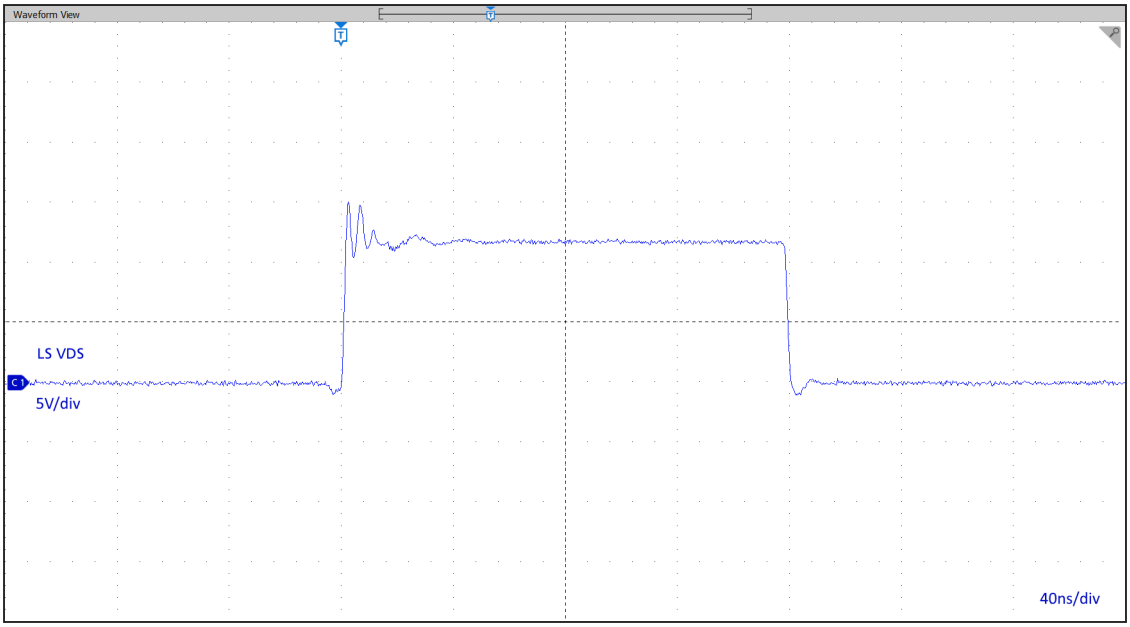


Figure 7-8. Low-side MOSFET V_{DS}

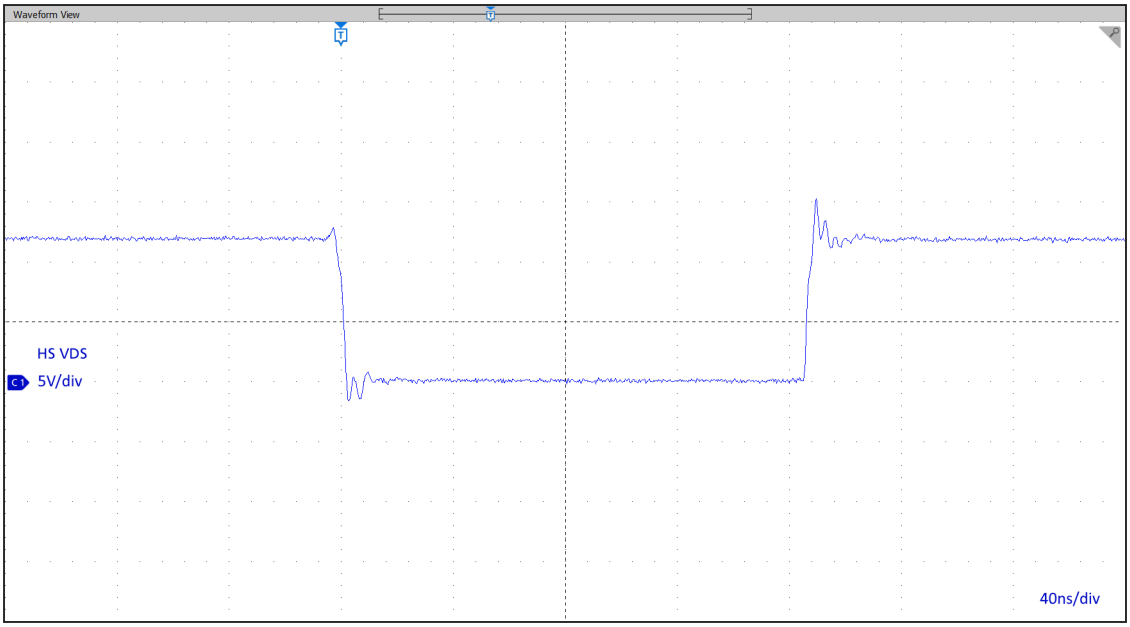


Figure 7-9. High-side MOSFET V_{DS}

7.7 Control On

Figure 7-10 illustrates the start-up from control on waveforms at 10-A output.

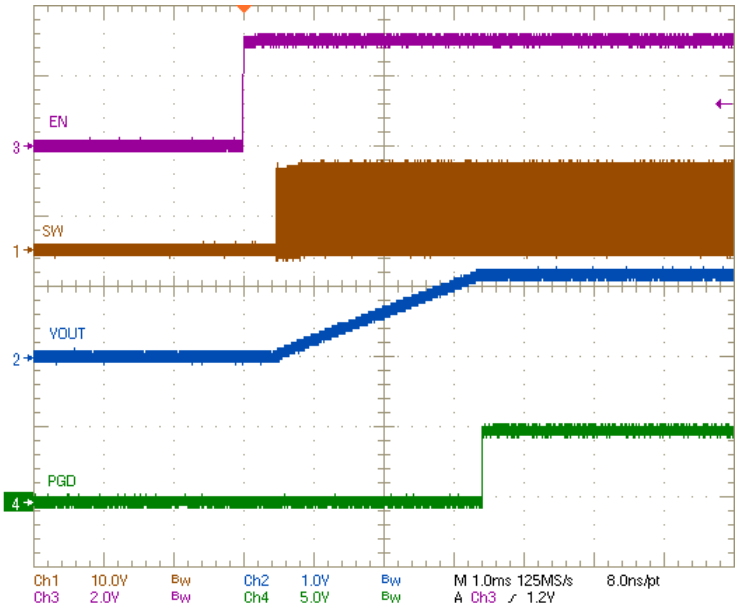


Figure 7-10. Start-Up From Control, 10-A CC Load

7.8 Control Off

Figure 7-11 illustrate the control off waveforms at 10-A output.

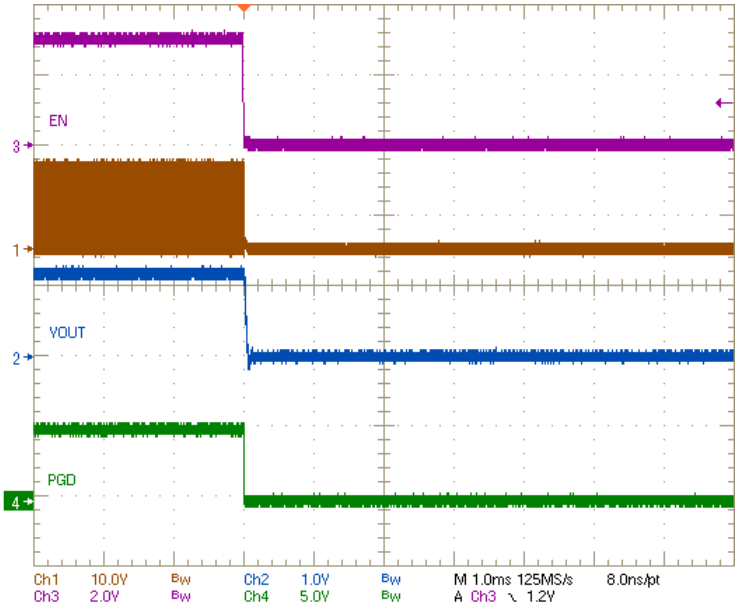


Figure 7-11. Shutdown From Control, 10-A CC Load

7.9 Control On With Pre-biased Output

Figure 7-12 illustrates the control on waveforms with a pre-biased output voltage.

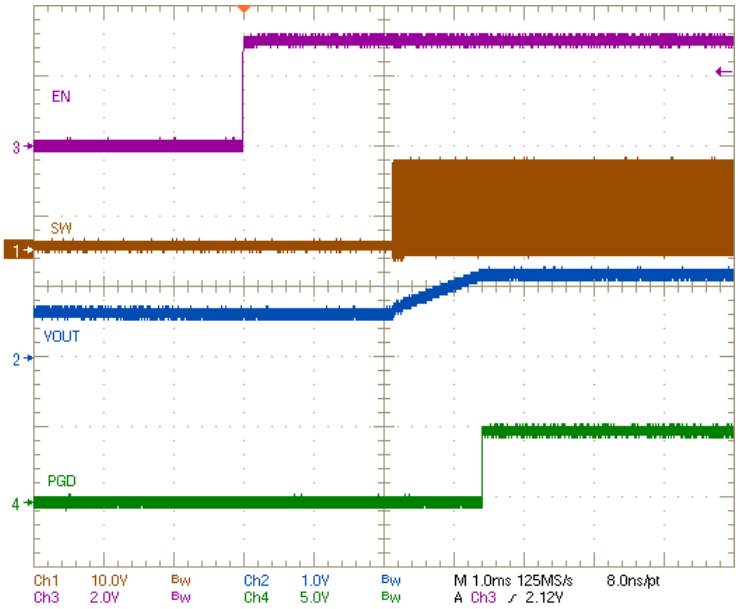
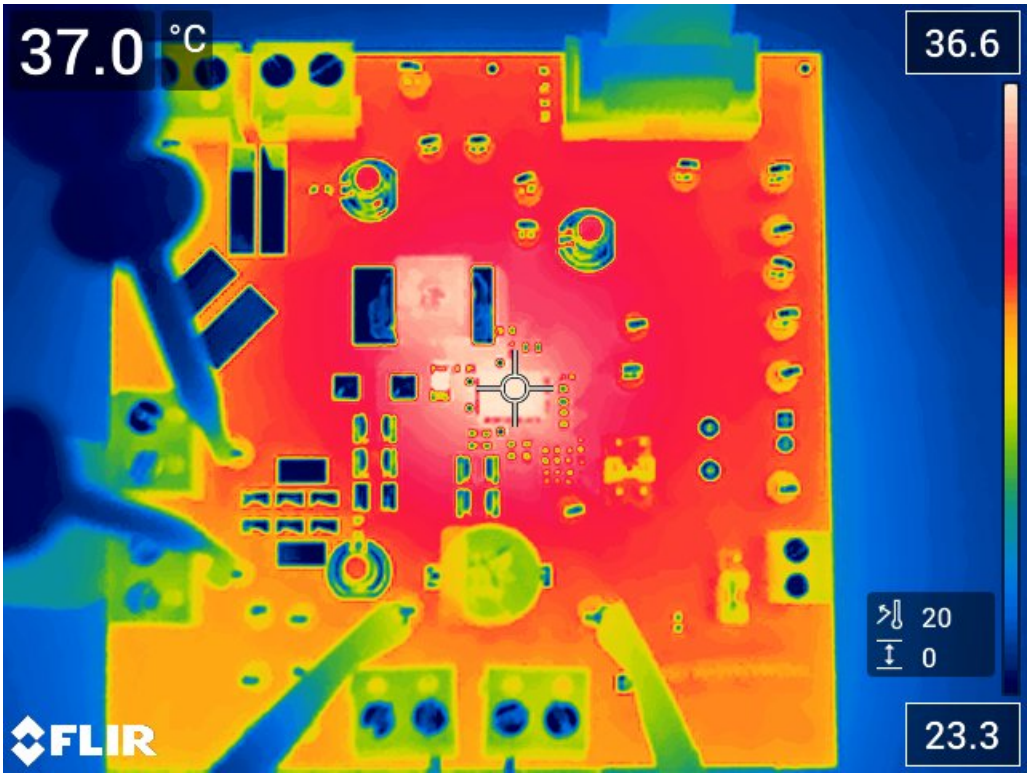


Figure 7-12. Start-Up From Control With Pre-biased Output

7.10 Thermal Image

Figure 7-13 shows the TPS546A24AEVM-1PH thermal image.



V_{IN} = 12 V, I_{OUT} = 10 A

Figure 7-13. Thermal Image

8 EVM Assembly Drawing and PCB Layout

Figure 8-1 through Figure 8-12 show the design of the TPS546A24AEVM-1PH printed circuit board.

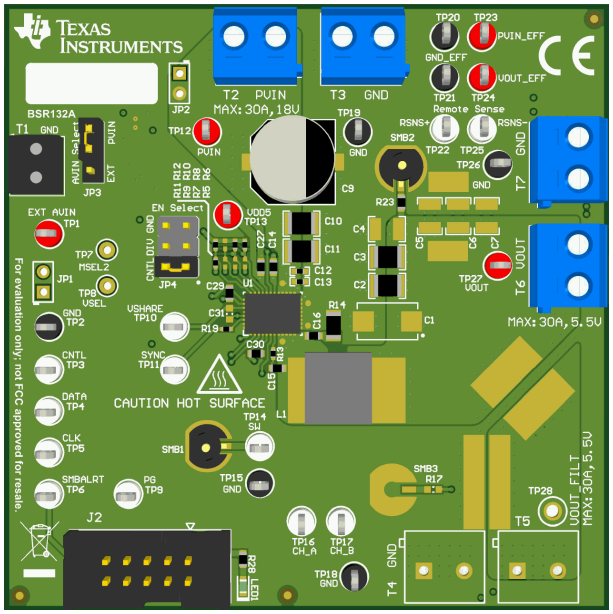


Figure 8-1. TPS546A24AEVM-1PH 3D Top View

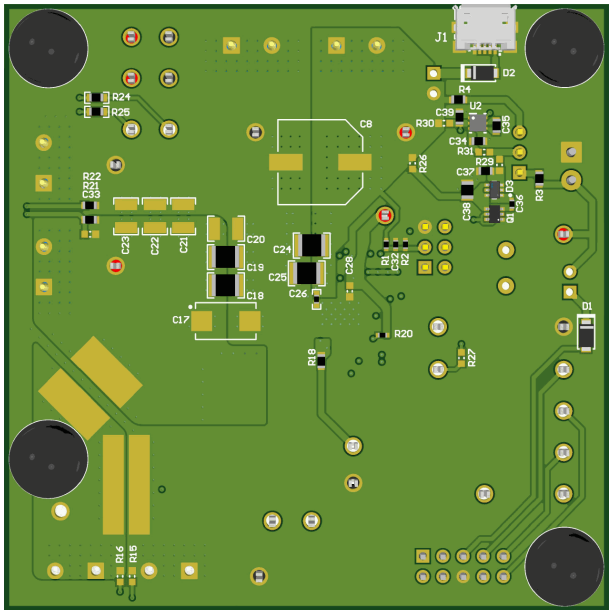


Figure 8-2. TPS546A24AEVM-1PH 3D Bottom View

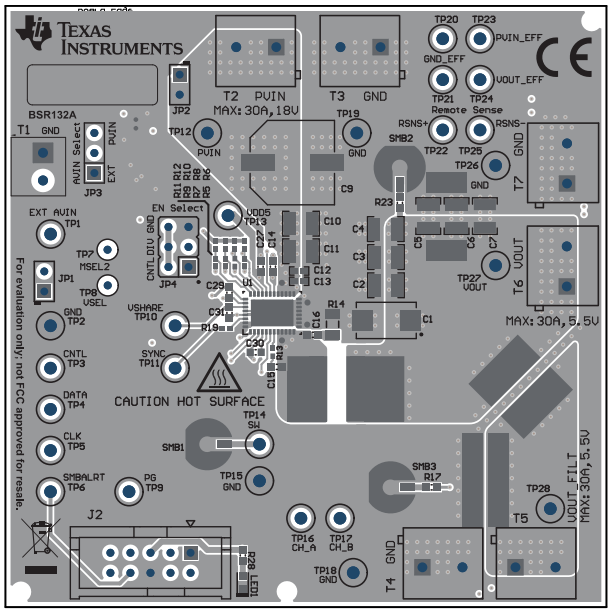


Figure 8-3. TPS546A24AEVM-1PH Top Side Component View (Top View)

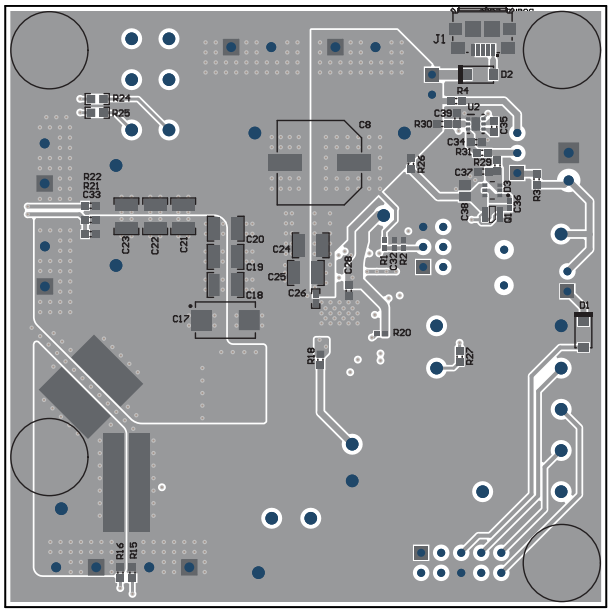


Figure 8-4. TPS546A24AEVM-1PH Bottom Side Component View (Bottom View)

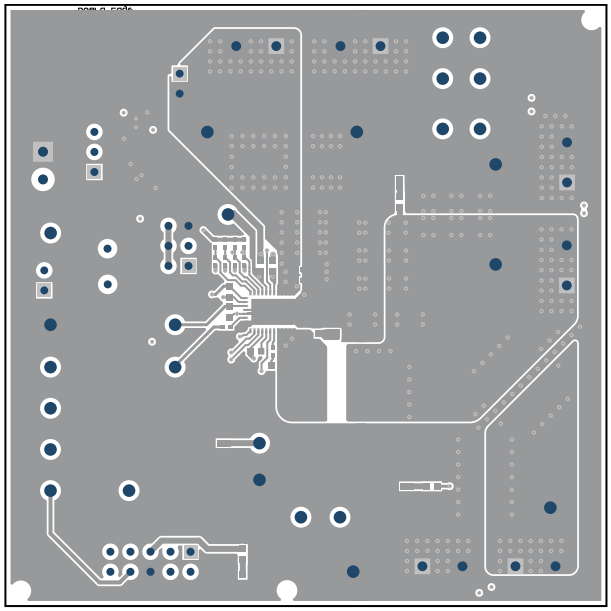


Figure 8-5. TPS546A24AEVM-1PH Top Copper (Top View)

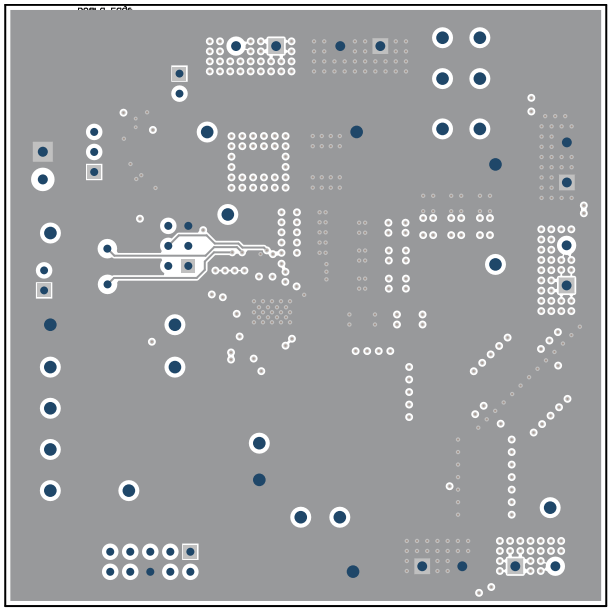


Figure 8-6. TPS546A24AEVM-1PH Internal Layer 1 (Top View)

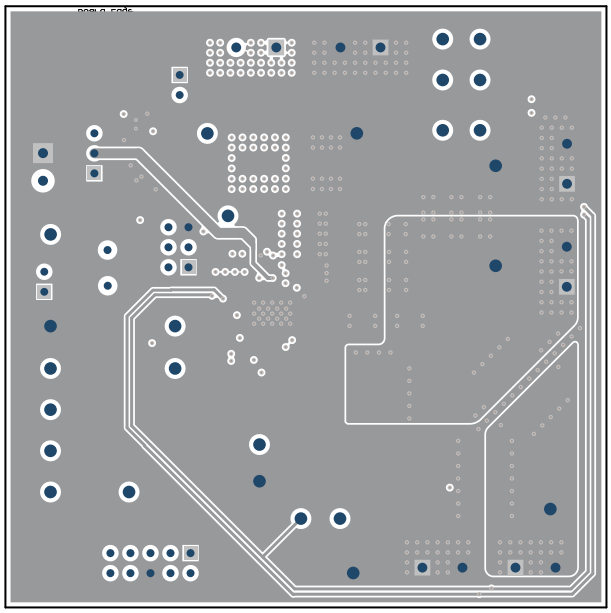


Figure 8-7. TPS546A24AEVM-1PH Internal Layer 2 (Top View)

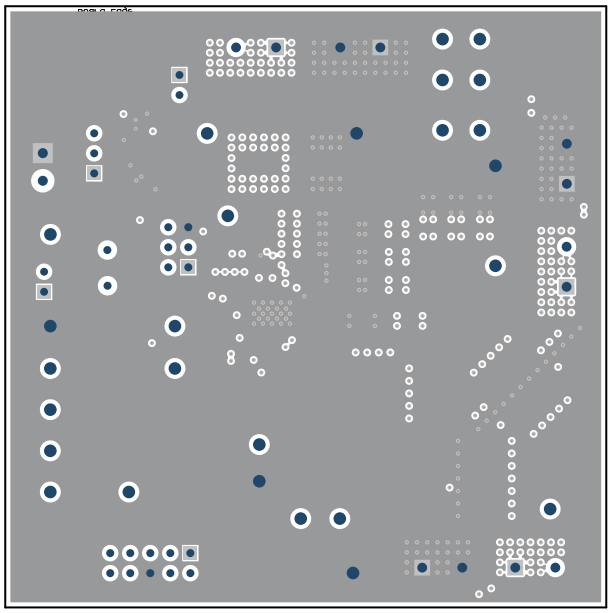


Figure 8-8. TPS546A24AEVM-1PH Internal Layer 3 (Top View)

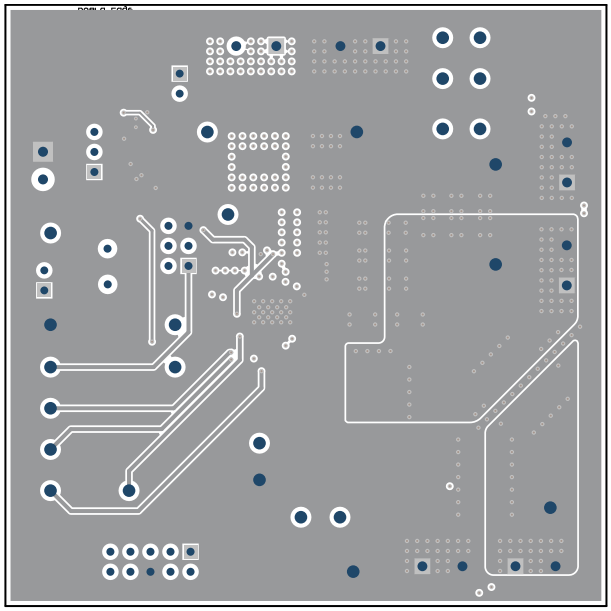


Figure 8-9. TPS546A24AEVM-1PH Internal Layer 4 (Top View)

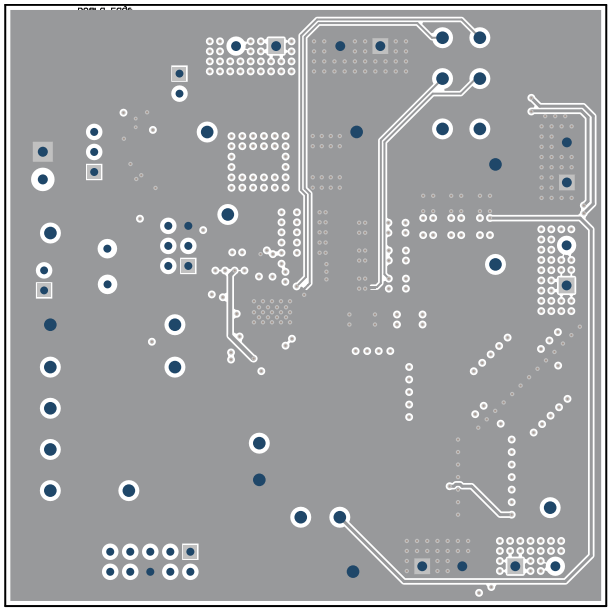


Figure 8-10. TPS546A24AEVM-1PH Internal Layer 5 (Top View)

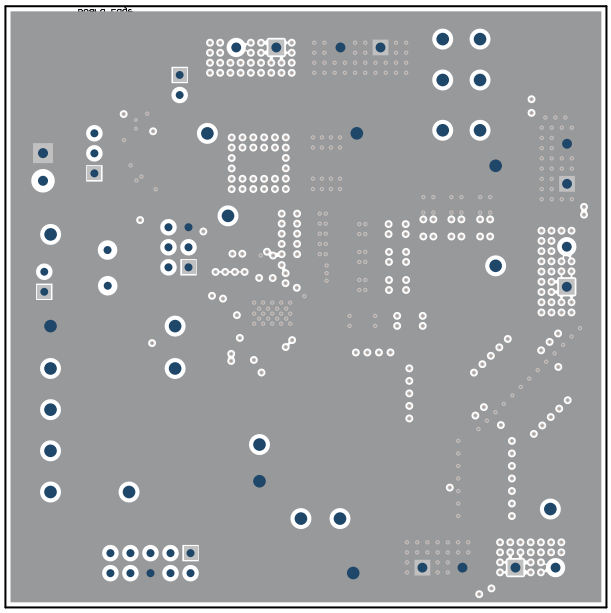


Figure 8-11. TPS546A24AEVM-1PH Internal Layer 6 (Top View)

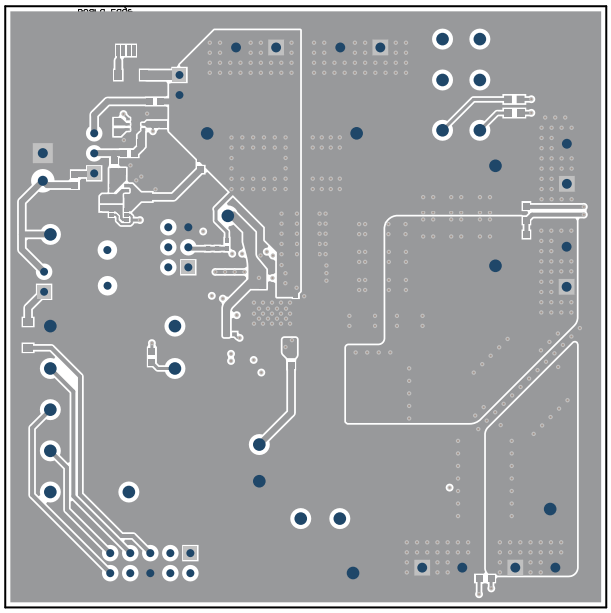


Figure 8-12. TPS546A24AEVM-1PH Internal Bottom Layer (Top View)

9 Bill of Materials

Table 9-1 lists the BOM for the TPS546A24AEVM-1PH.

Table 9-1. Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board		BSR132	Any
C2, C3, C18, C19	4	100uF	CAP, CERM, 100 µF, 6.3 V,+/- 20%, X7S, 1210	1210	GRM32EC70J107ME15L	MuRata
C9	1	100uF	CAP, AL, 100 uF, 35 V, +/- 20%, 0.15 ohm, SMD	SMT Radial G	EEE-FC1V101P	Panasonic
C10, C11, C24, C25	4	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X6S, 1210	1210	GRM32EC81E226KE15L	MuRata
C12, C13, C26	3	6800pF	CAP, CERM, 6800 pF, 50 V,+/- 10%, X7R, 0402	0402	GCM155R71H682KA55D	MuRata
C14	1	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C15	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C16	1	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	0603	06031C102JAT2A	AVX
C27	1	4.7uF	CAP, CERM, 4.7 uF, 10 V, +/- 10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet
C29	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C1608C0G1H101J080AE	TDK
C30	1	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C32	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
C34, C35, C37, C39	4	2.2uF	CAP, CERM, 2.2 µF, 25 V,+/- 10%, X7S, 0603	0603	GRM188C71E225KE11D	MuRata
C36	1	0.22uF	CAP, CERM, 0.22 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	GCM155R71C224KE02D	MuRata
C38	1	10uF	CAP, CERM, 10 µF, 25 V,+/- 20%, X6S, 0805	0805	GRM21BC81E106ME51L	MuRata
D1, D2	2	30V	Diode, Schottky, 30 V, 2 A, AEC-Q101, SOD-123FL	SOD-123FL	MBR230LSFT1G	ON Semiconductor
D3	1		DIODE ARRAY SCHOTTKY 40V SOT363	SOT363	SD103ATW-7-F	Diodes
H5, H6, H7, H8	4		Bumpon, Hemisphere, 0.375 X 0.235, Black	Black Bumpon	SJ61A2	3M
J1	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	MICRO USB CONN, R/A	1981568-1	TE Connectivity
J2	1		Header (shrouded), 100mil, 5x2, Gold, TH	5x2 Shrouded header	5103308-1	TE Connectivity
JP3	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
JP4	1		Header, 100mil, 3x2, Gold, TH	Sullins 100mil, 2x3, 230 mil above insulator	PBC03DAAN	Sullins Connector Solutions
L1	1	680nH	Inductor, Shielded, Composite, 680 nH, 37 A, 0.0014 ohm, SMD	8.1 x 8 x 8.6mm	XAL8080-681MEB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
LED1	1	Green	LED, Green, SMD	LED_0603	150060GS75000	Wurth Elektronik
Q1	1	30V	MOSFET, 2-CH, N/P-CH, 30 V, 0.65 A, SOT-363	SOT-363	DMC3400SDW-7	Diodes Inc.
R1	1	30.1k	RES, 30.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040230K1FKED	Vishay-Dale
R2	1	8.66k	RES, 8.66 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04028K66FKED	Vishay-Dale
R3, R4	2	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R6, R13, R19	3	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R8	1	68.1k	RES, 68.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040268K1FKED	Vishay-Dale
R11	1	3.16k	RES, 3.16 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K16FKED	Vishay-Dale
R12	1	5.62k	RES, 5.62 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04025K62FKED	Vishay-Dale
R14	1	1.0	RES, 1.0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW12061R00JNEA	Vishay-Dale
R18, R23	2	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R20	1	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R21, R22	2	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RFKEA	Vishay-Dale

Table 9-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
R24, R25	2	10.0	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
R28	1	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
SH-JP3, SH-JP4	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
SMB1, SMB2	2		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
T1	1		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
T2, T3, T6, T7	4		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
TP1, TP12, TP13, TP23, TP24, TP27	6		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2, TP15, TP18, TP19, TP20, TP21, TP26	7		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP3, TP4, TP5, TP6, TP9, TP10, TP11, TP14, TP16, TP17, TP22, TP25	12		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
U1	1		2.95-16V 10A PMBUS Stackable Synchronous Buck Converter, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS546A24ARVFR	Texas Instruments
U2	1		5 V, Step-Up Charge Pump Regulator, 140 mA, 2.7 to 5.5 V Input, -40 to 85 degC, 6-pin SON (DRV6), Green (RoHS & no Sb/Br)	DRV0006A	TPS60150DRVR	Texas Instruments
C1, C17	0	330uF	CAP, Tantalum Polymer, 330 uF, 10 V, +/- 20%, 0.006 ohm, 7343-43 SMD	7343-43	T530X337M010ATE006	Kemet
C4, C5, C6, C7, C20	0	100uF	CAP, CERM, 100 µF, 6.3 V,+/- 20%, X7S, 1210	1210	GRM32EC70J107ME15L	MuRata
C8	0	100uF	CAP, AL, 100 uF, 35 V, +/- 20%, 0.15 ohm, SMD	SMT Radial G	EEE-FC1V101P	Panasonic
C21, C22, C23	0	47uF	CAP, CERM, 47 uF, 10 V, +/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
C28	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C31, C33	0	33pF	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C330J5GACTU	Kemet
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
JP1, JP2	0		Header, 100mil, 2x1, Tin, TH	Header, 2x1, 100mil, TH	5-146278-2	TE Connectivity
R5, R7, R9, R10	0	10.5k	RES, 10.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K5FKED	Vishay-Dale
R15, R16	0	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RFKEA	Vishay-Dale
R17	0	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R26, R27, R29, R30, R31	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
SH-JP1, SH-JP2	0	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
SMB3	0		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
T4, T5	0		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
TP7, TP8	0		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP28	0		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone

10 Using the Fusion GUI

10.1 Opening the Fusion GUI

The Fusion GUI should include *IC_DEVICE_ID* in the scanning mode to find TPS546A24A. The EVM needs power to be recognized by the Fusion GUI. See Section 5 for the recommended procedure.

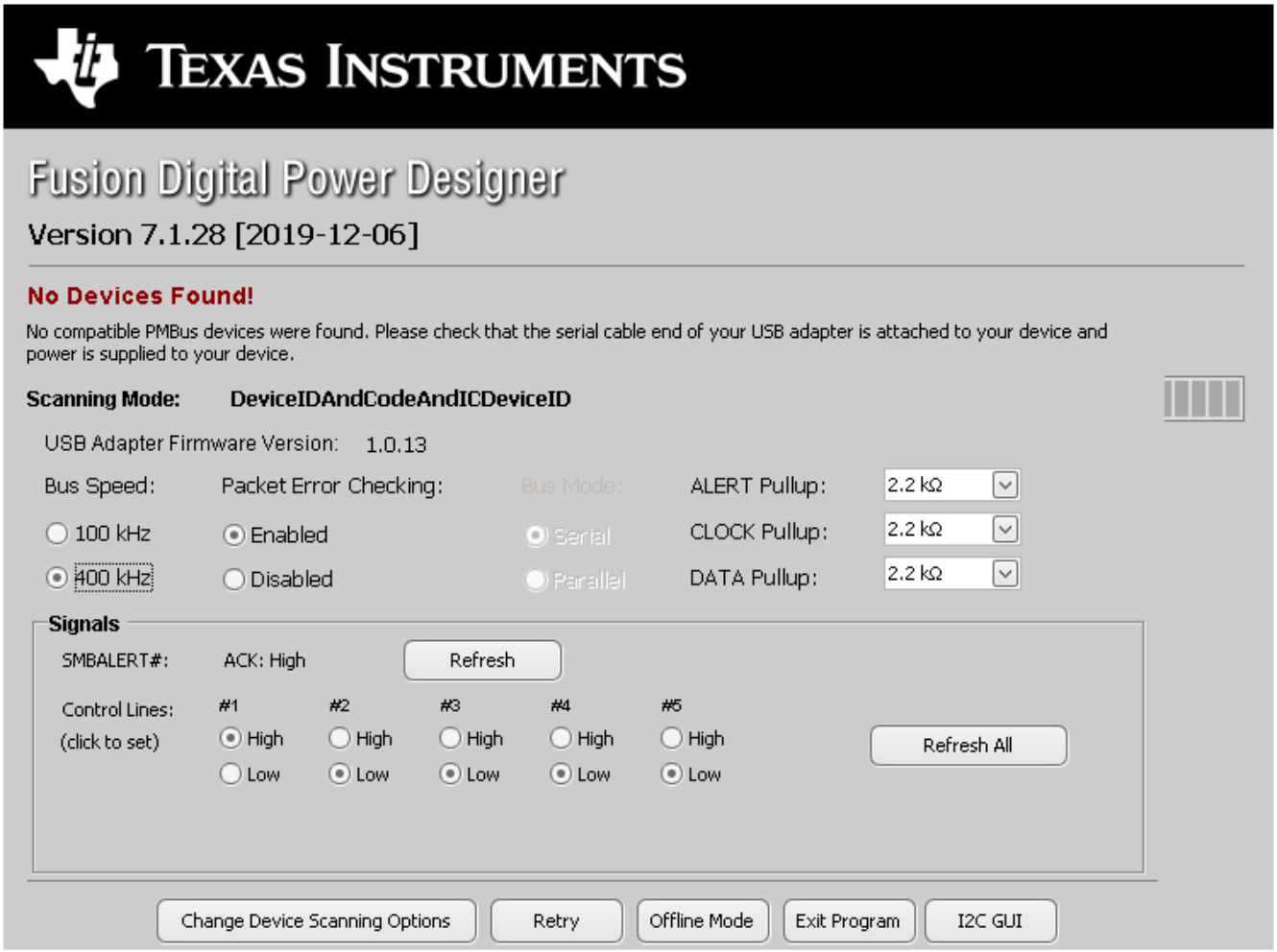


Figure 10-1. Select Device Scanning Mode

10.2 General Settings

Figure 10-2 shows the *General Settings* that can be used to configure the following:

- Vout settings, power good limits and margin voltages
- OC Fault, OC Warn and Fault response
- OT Fault, OT Warn (Die Temperature) and Fault response
- Vin on and off UVLO
- On/Off Config
- Soft Start (Output rise time), other Turn On Timing and Turn Off Timing
- Switching frequency
- Compensation

After clicking *Write to Hardware* to make changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking *Store Config to NVM*. This action prompts a pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in non-volatile memory.

Both the loop master device and the loop slave device are tied to same bus interface. In a two-phase stacking system, the master device will receive and respond to all PMBus communication and slave devices do not need to be connected to the PMBus. If the master receives commands which require updates to the PMBus registers of the slave, the master will relay these commands to the slaves. All commands on this tab are for PHASE = 0xFF.

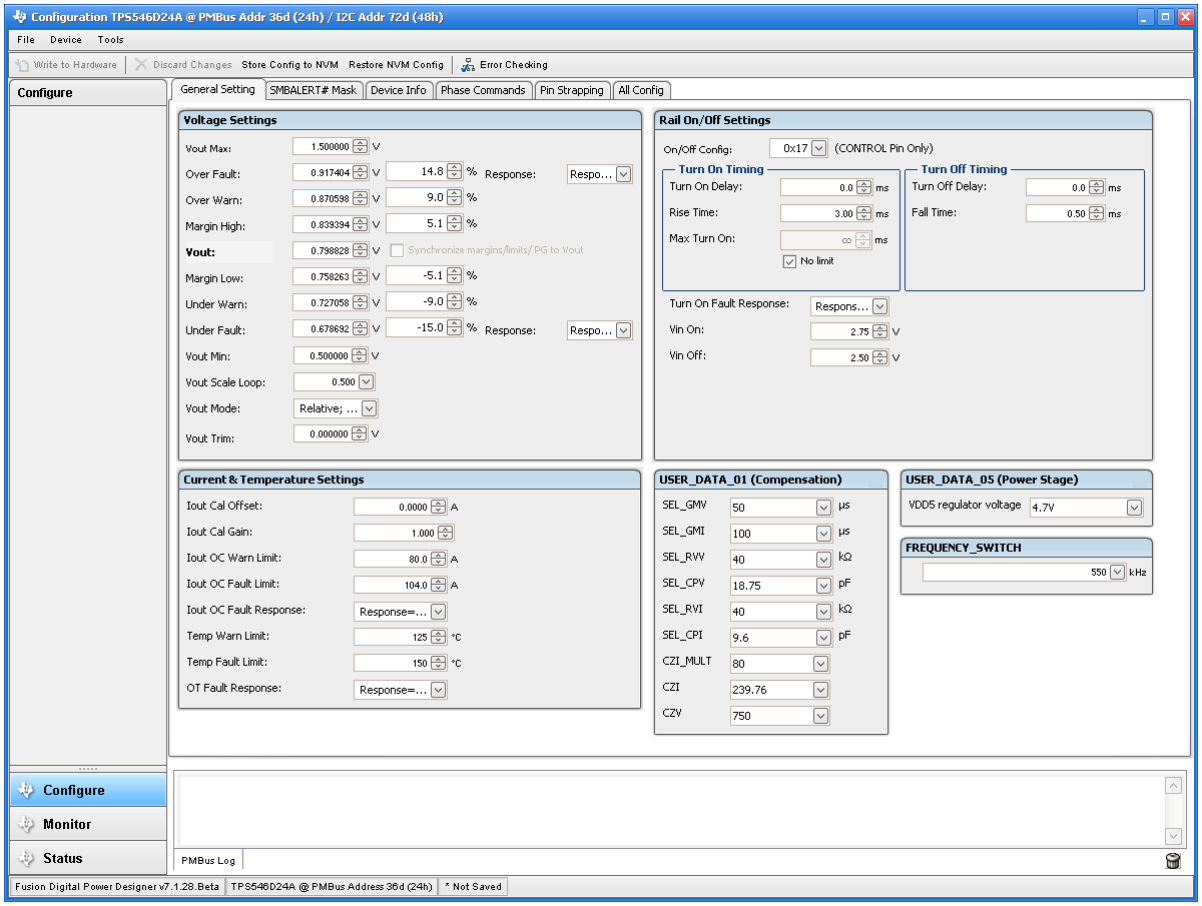


Figure 10-2. General Settings

10.3 Changing ON_OFF_CONFIG

Changing the *On/Off Config* prompts a pop-up window with details of the options shown in Figure 10-3. This pop-up gives multiple options on what turns on and off power conversion. By default the TPS546A24A is configured to *CONTROL Pin Only*. This is the EN/UVLO pin.

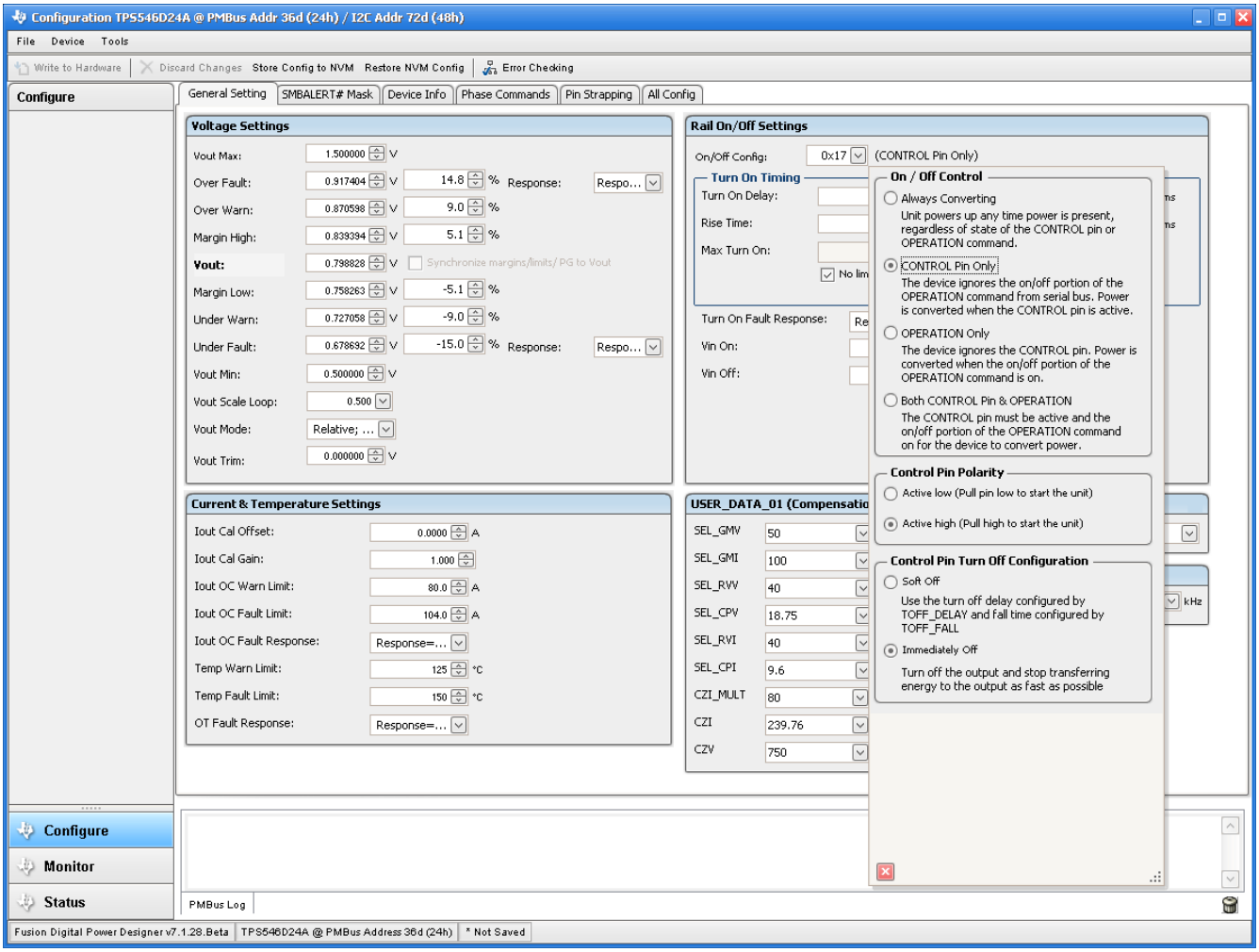


Figure 10-3. Configure – ON_OFF_CONFIG

10.4 Pop-up for Some Commands While Conversion is Enabled

Some commands will cause a pop-up like the one shown in Figure 10-4 when trying to change them while conversion is enabled. The settings in the GUI which will cause this pop-up include *FREQUENCY_SWITCH*, *USER_DATA_01 (Compensation)*, *Vout Mode* and *Vout Scale Loop*. To change these settings to a new value, click on *Stop Power Conversion* then *Close and continue*. The GUI will automatically disable conversion, write the new value, and enable conversion again.

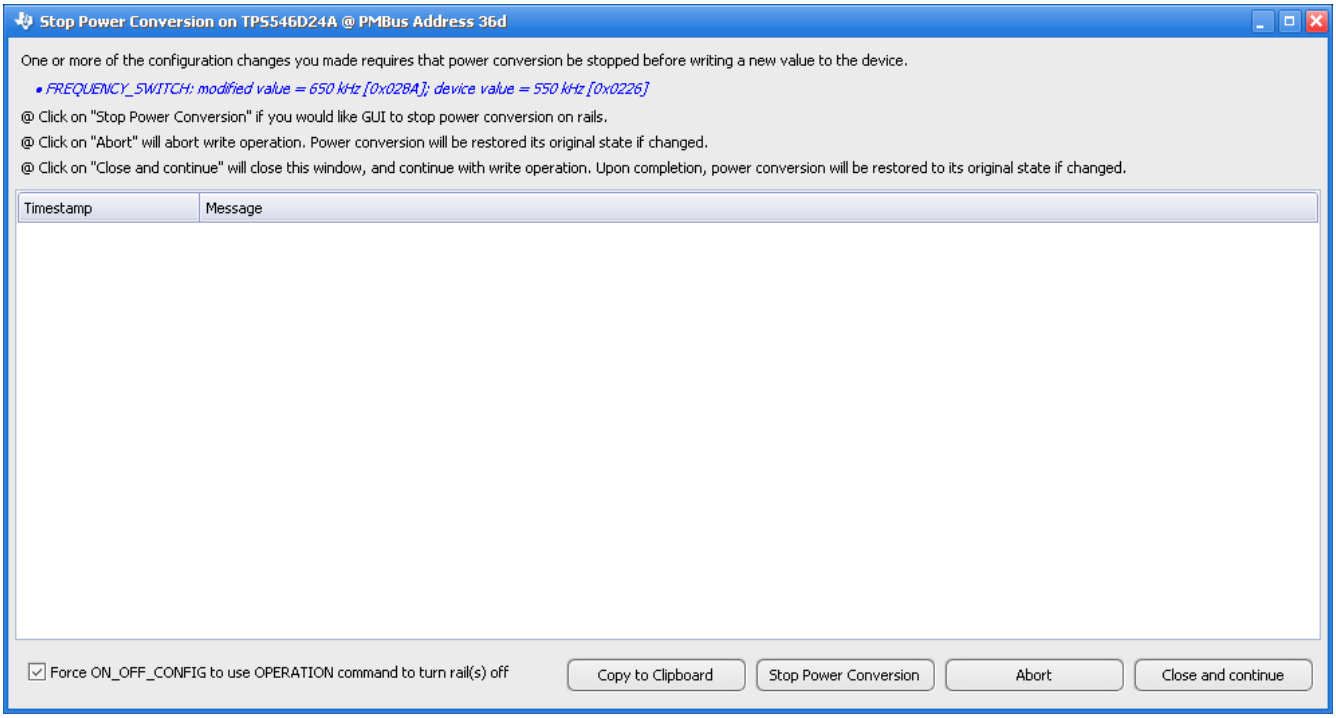


Figure 10-4. Pop-up When Trying to Change FREQUENCY_SWITCH With Conversion Enabled

10.5 SMBALERT# Mask

The sources of SMBALERT which can be masked are found and configured on the *SMBALERT # Mask* tab (Figure 10-5).

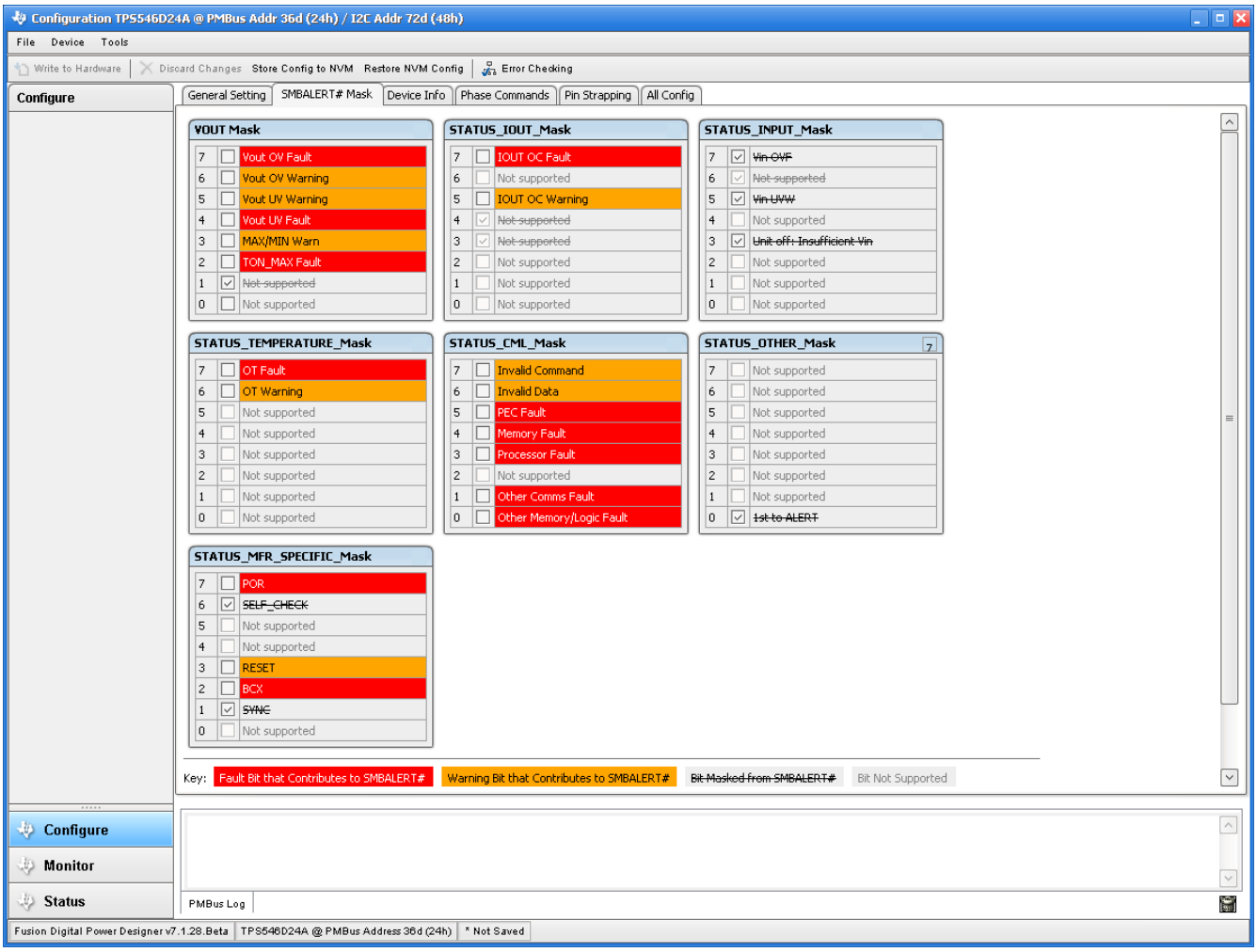


Figure 10-5. Configure – SMBALERT # Mask

10.6 Device Info

The device information, Write Protection options, the configuration of *Vout Scale Loop*, *Vout Transition Rate*, and *Iout Cal Offset* are found on the *Device Info* tab (see Figure 10-6).

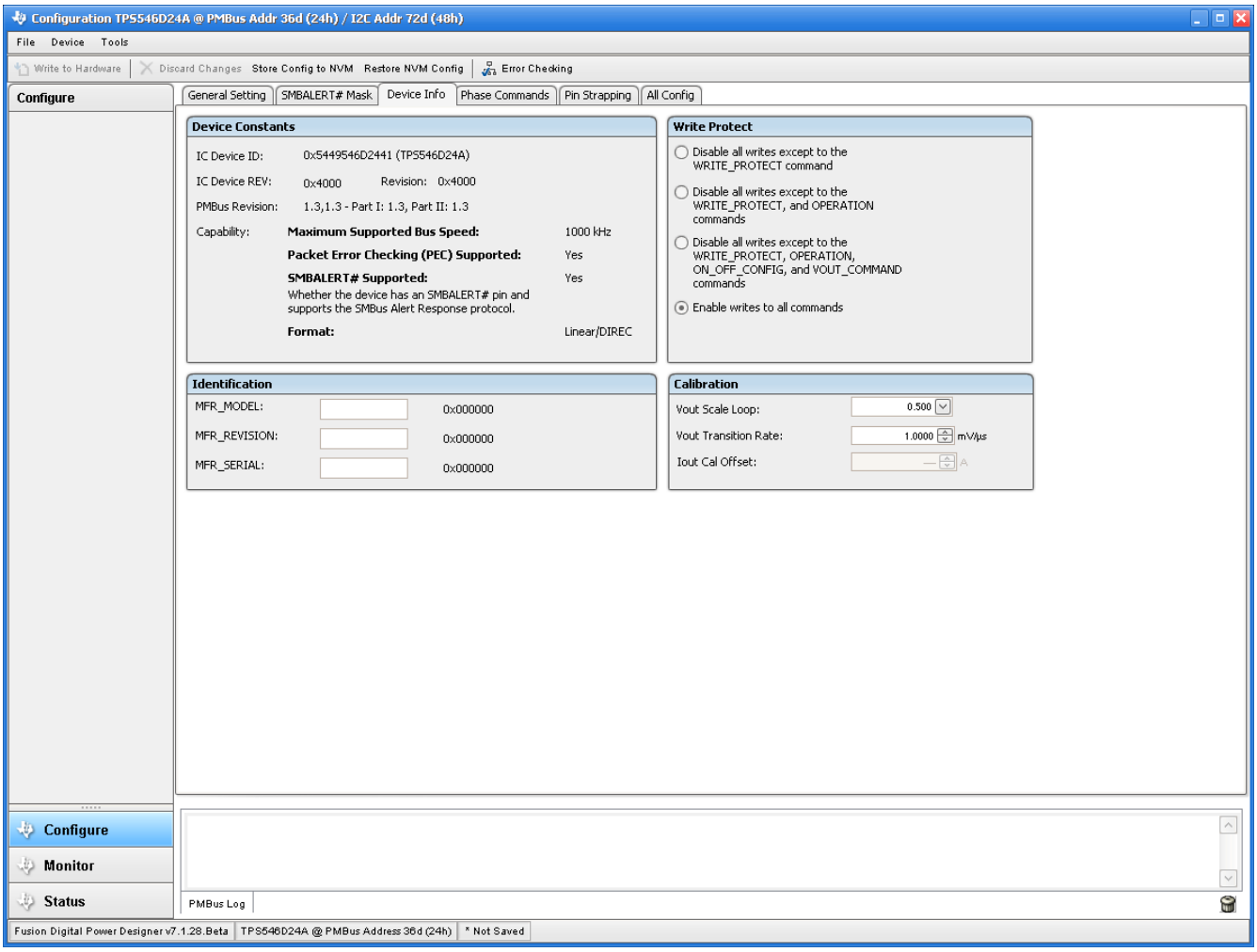


Figure 10-6. Configure – Device Info

10.7 Phase Commands

Use the *Phase Command* tab (see Figure 10-7) to calibrate the *IOUT/Temp* of each phase.

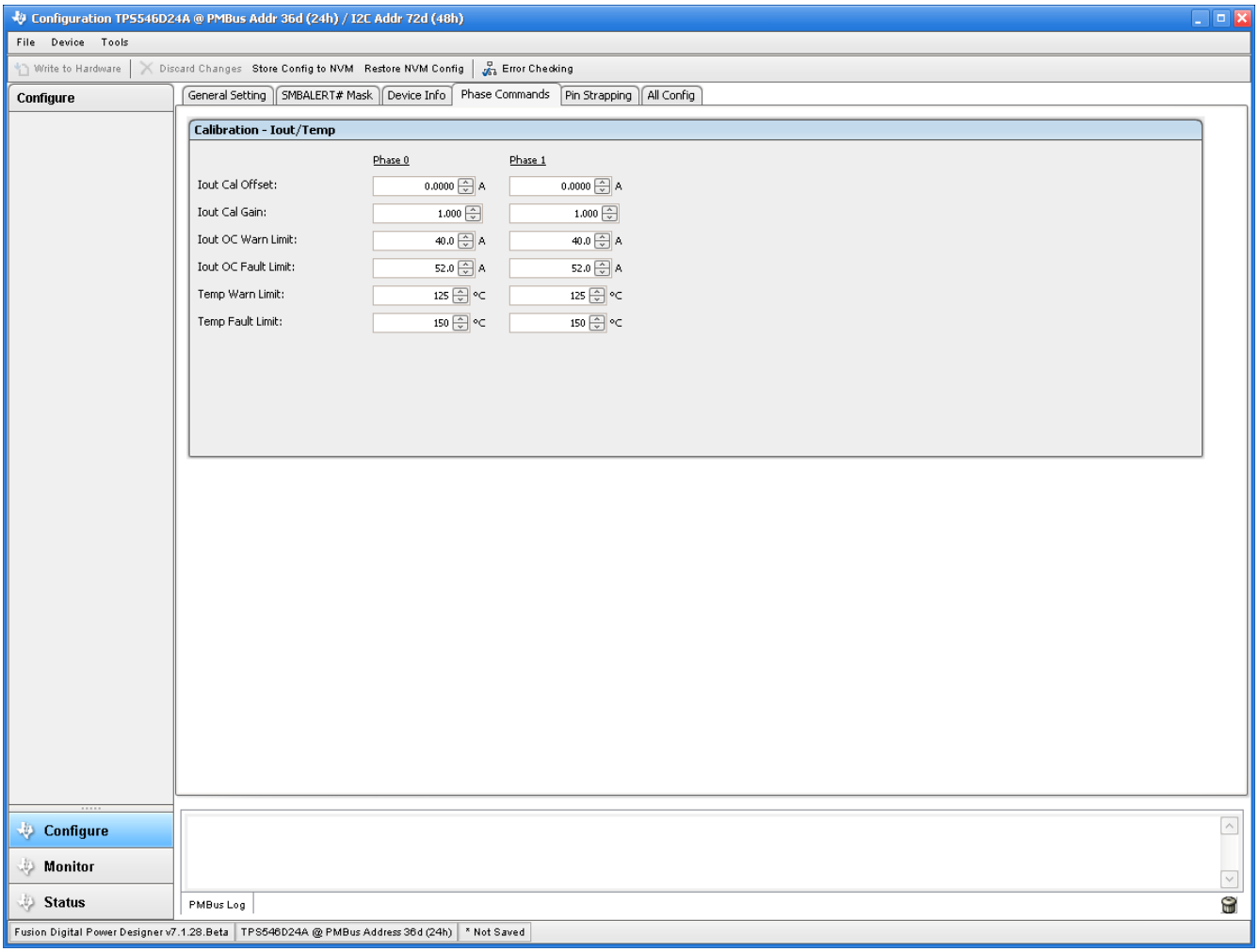


Figure 10-7. Phase Commands

10.8 All Config

Use the *All Config* tab (Figure 10-8) to configure all of the configurable parameters, which also shows other details like Hex encoding.

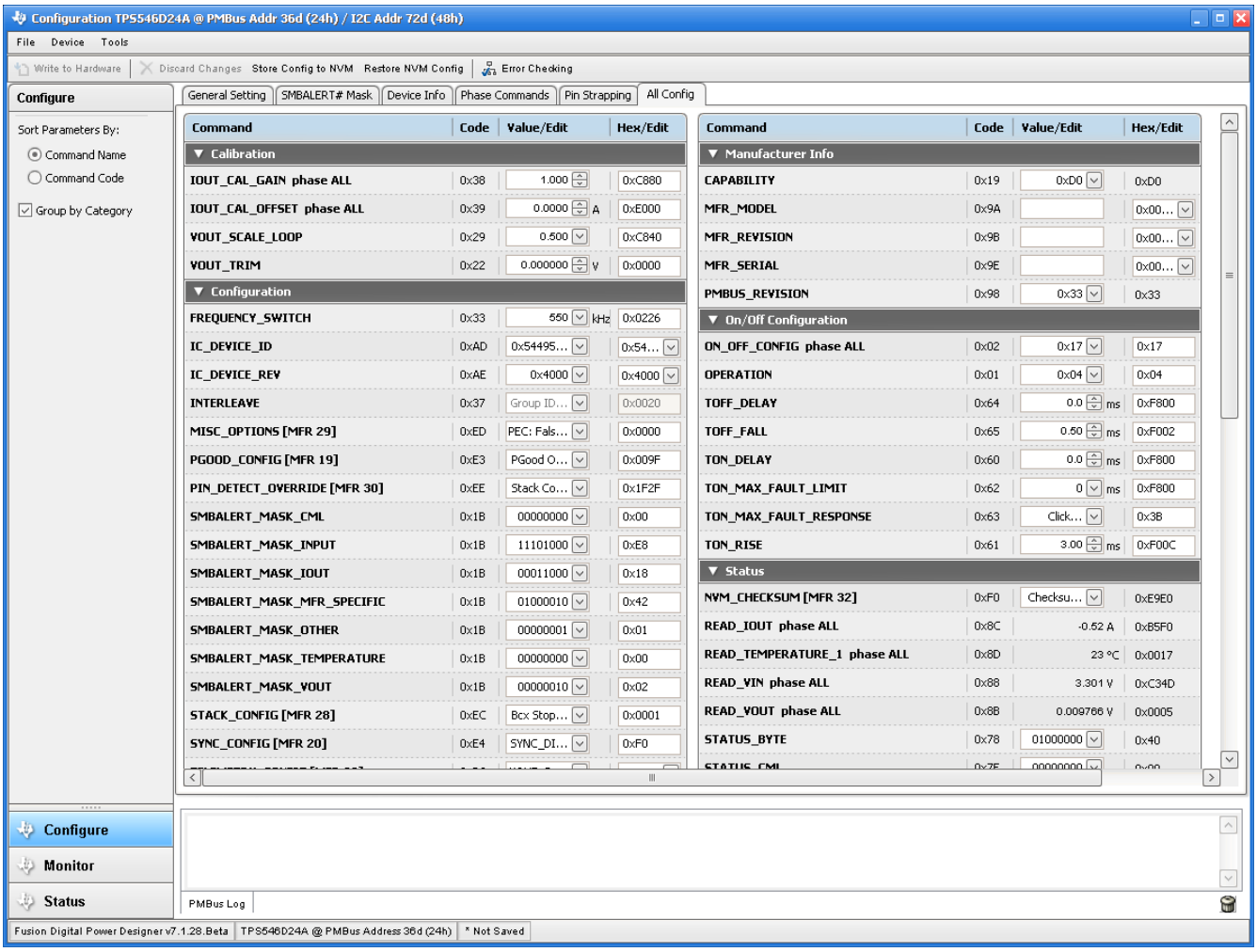


Figure 10-8. Configure – All Config

10.9 Pin Strapping

Use the *Pin Strapping* tab (Figure 10-8) to aid in selection of external pin strapping resistors used to program some of the PMBus commands at power-up. The *EEPROM Value* column shows the values currently configured to the related PMBus commands.

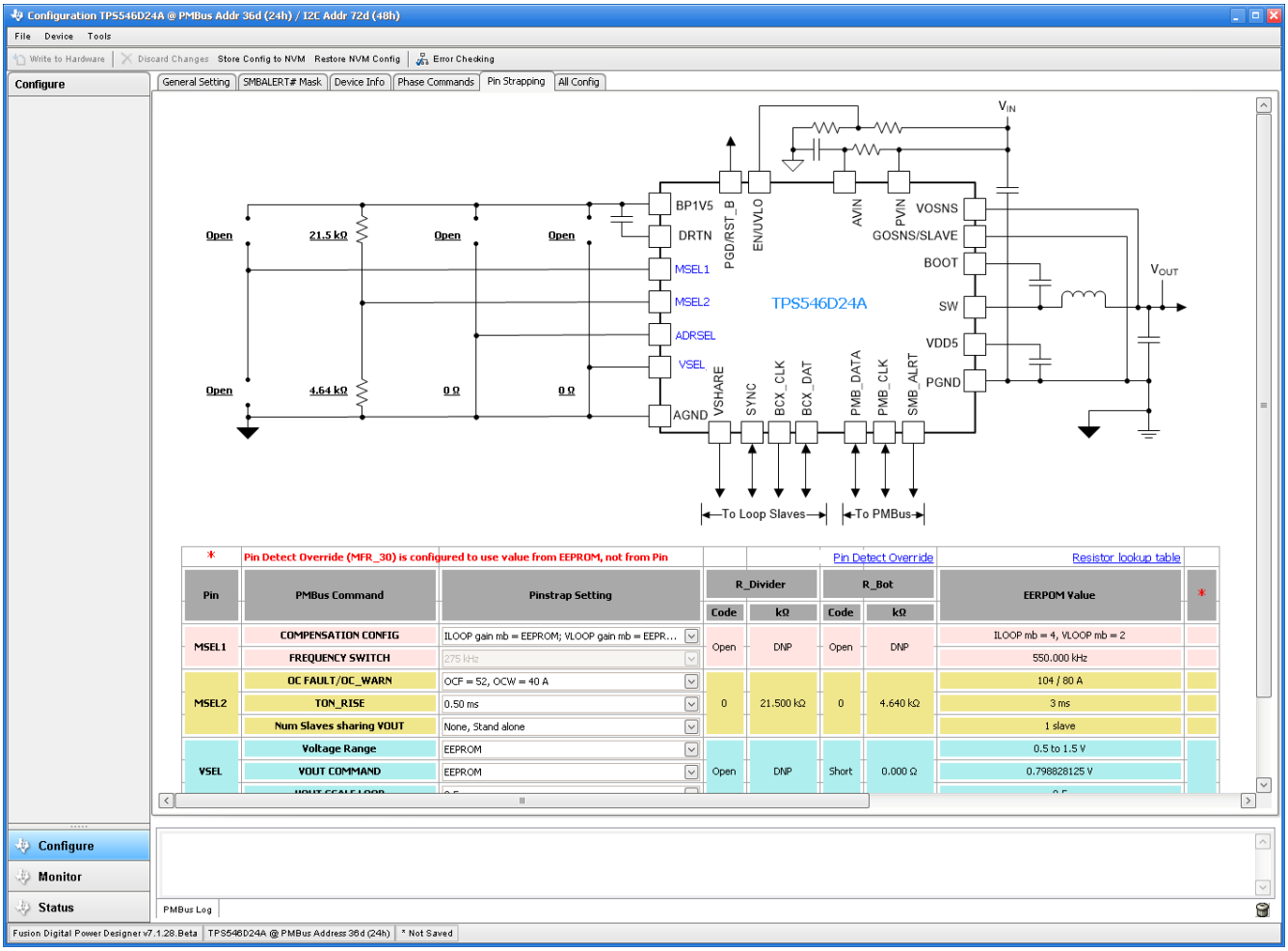


Figure 10-9. Configure – Pin Strapping

10.10 Monitor

When the *Monitor* screen (Figure 10-10) is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of *Vout*, *Iout*, *Vin*, *Pout*, and *Temperature*
- *Start and Stop Polling* which turns ON or OFF the realtime display of data
- Quick access to *On/Off Config*
- Control pin activation and *OPERATION* command
- Margin control
- Clear Fault: Selecting ***Clear Faults*** clears any prior fault flags.

With two devices stacked together, the *Iout* reading is the total load supported by both devices. There is also an *Iout* which shows the current in each phase.

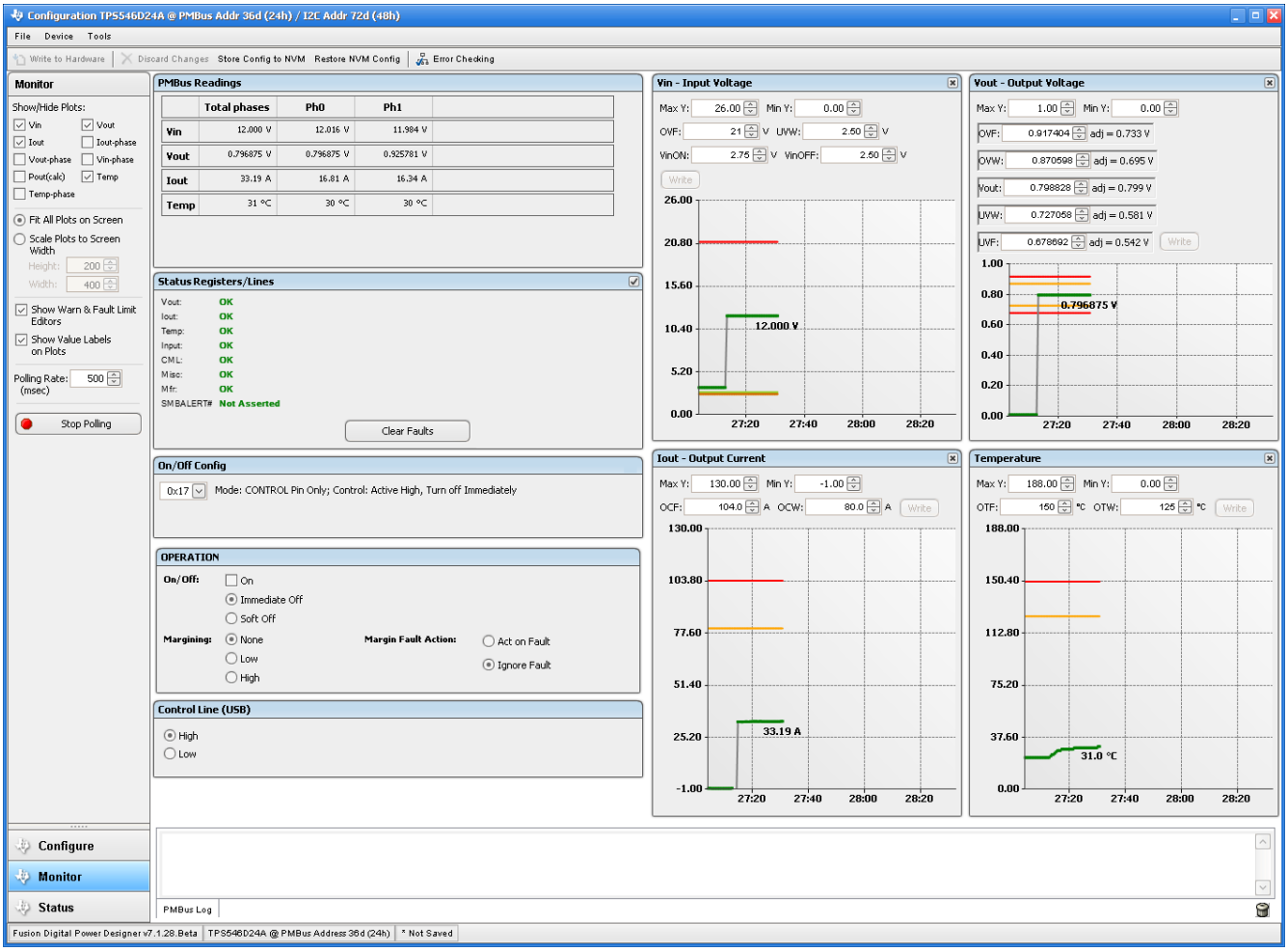


Figure 10-10. Monitor Screen

10.11 Status

Selecting *Status* screen from lower left corner (Figure 10-11) shows the status of the device.

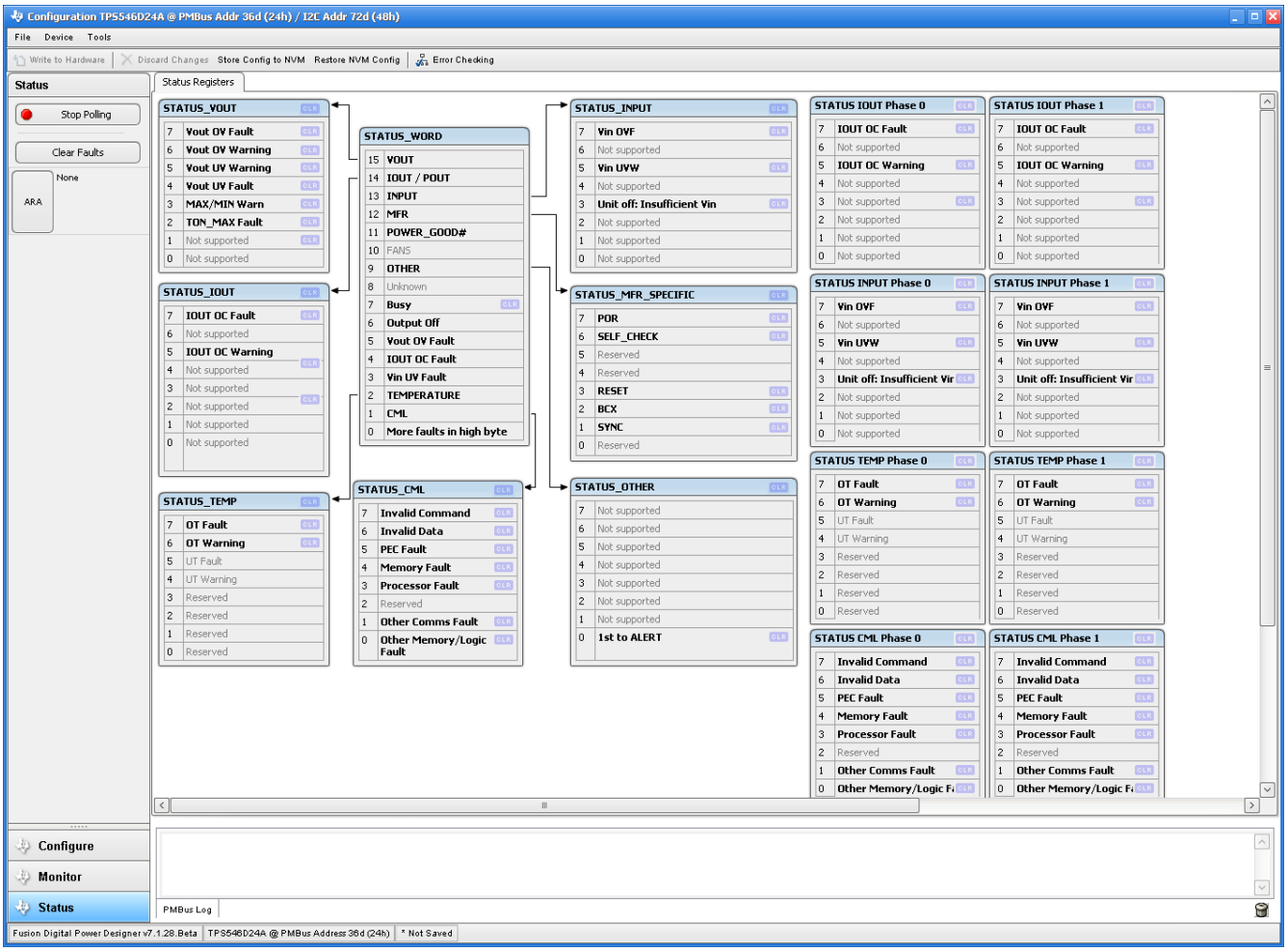


Figure 10-11. Status Screen

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2020) to Revision A (April 2021)	Page
• Updated user's guide title	2

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