User's Guide

TPS546B24A 2-Phase SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

The TPS546B24AEVM-2PH evaluation module (EVM) is a two-phase buck converter with two TPS546B24A devices. The TPS546B24A device is a stackable synchronous buck with PMBus interface that can operate from a nominal 2.95-V to 18-V supply. The device allows programming and monitoring through the interface.

Two TPS546B24A devices are configured as two-phase buck converter in factory default. Output current is evenly distributed in the two devices; both the negative and positive output terminals are connected together.

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Trademarks

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1 Description

The TPS546B24AEVM-2PH is a two-phase buck design stacking two TPS546B24A devices. It designed for a nominal 12-V bus and to produce a regulated 0.8-V output at up to 40 A of load current. The TPS546B24AEVM-2PH is designed to demonstrate stacking operation of the TPS546B24A in a two-phase, low-output voltage application while providing a number of test points to evaluate the performance of the devices. The TPS546B24AEVM-2PH can be modified to single-phase buck converters by changing the components assembled. See Section 4.3 for more information on single-phase configuration.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS546B24AEVM-2PH. Observe all safety precautions.

Warning The TPS546B24AEVM-2PH circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces, or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than one power supply, check the equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to the equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the battery potential of the EVM.

1.2 Typical Applications

The TPS546B24A device is designed for the following applications:

- High-density power solutions
- Wireless infrastructure
- Switcher
- Router network
- Server
- Storage
- Smart power systems

1.3 Features

This EVM has the following features:

- Regulated 0.8-V output up to 40-A_{DC} steady-state output current
- The output voltage is marginable and trimmable using the PMBus interface
  - Programmable UVLO, soft-start, and enable via the PMBus interface
  - Programmable overcurrent warning and fault limits and programmable response to faults through the PMBus interface
  - Programmable overvoltage and undervoltage warning and fault limits and programmable response to faults through the PMBus interface
  - Programmable turn-on and turn-off delays
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 2-1 lists the electrical performance specifications in room temperature (20 to 25°C). Characteristics are given for an input voltage of V_{IN} = 12 V, unless otherwise specified.

Table 2-1. TPS546B24AEVM-2PH Electrical Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input Characteristics					
Input voltage range, V_{IN}		5	12	18	V
Full load input current	I_{OUT} = 40 A		3.1		A
Full load input current	V_{IN} = 5 V, I_{OUT} = 40 A		7.3		A
No load input current	I_{OUT} = 0 A, switching enabled		100		mA
Enable switching threshold	Set by default resistor divider, JP2_P1 and JP2_P2 pins 3 and 4 shorted		5.26		V
Disable switching threshold	Set by default resistor divider, JP2_P1 and JP2_P2 pins 3 and 4 shorted		4.75		V
Output Characteristics					
Output voltage, V_{OUT}			0.8		V
Output load current, I_{OUT}		0		40	A
Output voltage regulation	Line regulation: V_{IN} = 5 V to 18 V		0.1%		
	Load regulation: I_{OUT} = 0 A to 40 A		0.1%		
Output voltage ripple	I_{OUT} = 40 A		9		mVpp
Output voltage undershoot	I_{OUT} = 10-A to 30-A step at 10 A/µs		100		mV
Output voltage overshoot	I_{OUT} = 30-A to 10-A step at 10 A/µs		100		mV
Output overcurrent fault threshold	Phase current limit setting of U1_P1 programmed by MSEL2		26		A
	Phase current limit setting of U1_P2 programmed by MSEL2		26		A
Systems Characteristics					
Switching frequency	Programmed by MSEL1		550		kHz
Full load efficiency, V_{OUT} (1)	I_{OUT} = 40 A		86.8%		
Operating case temperature	I_{OUT} = 40 A, 10 minute soak		50		°C
Loop bandwidth	I_{OUT} = 20 A		60		kHz
Phase margin			56		°
PMBus Interface and Pin-Strapping					
U1_P1 PMBus address	Programmed by NVM and ADRSEL		36		Decimal
U1_P1 Voltage reference	Default setting of VOUT_COMMAND programmed by VSEL		800		mV
U1_P1 Soft-start time (TON_RISE)	Default setting of TON_RISE programmed by MSEL2		3		ms

(1) The efficiency is measured using the test points listed in Table 6-2 to minimize the effect of DC drops caused by on-board copper traces.

3 Schematic

Figure 3-1 through Figure 3-3 illustrate the TPS546B24AEVM-2PH schematics.

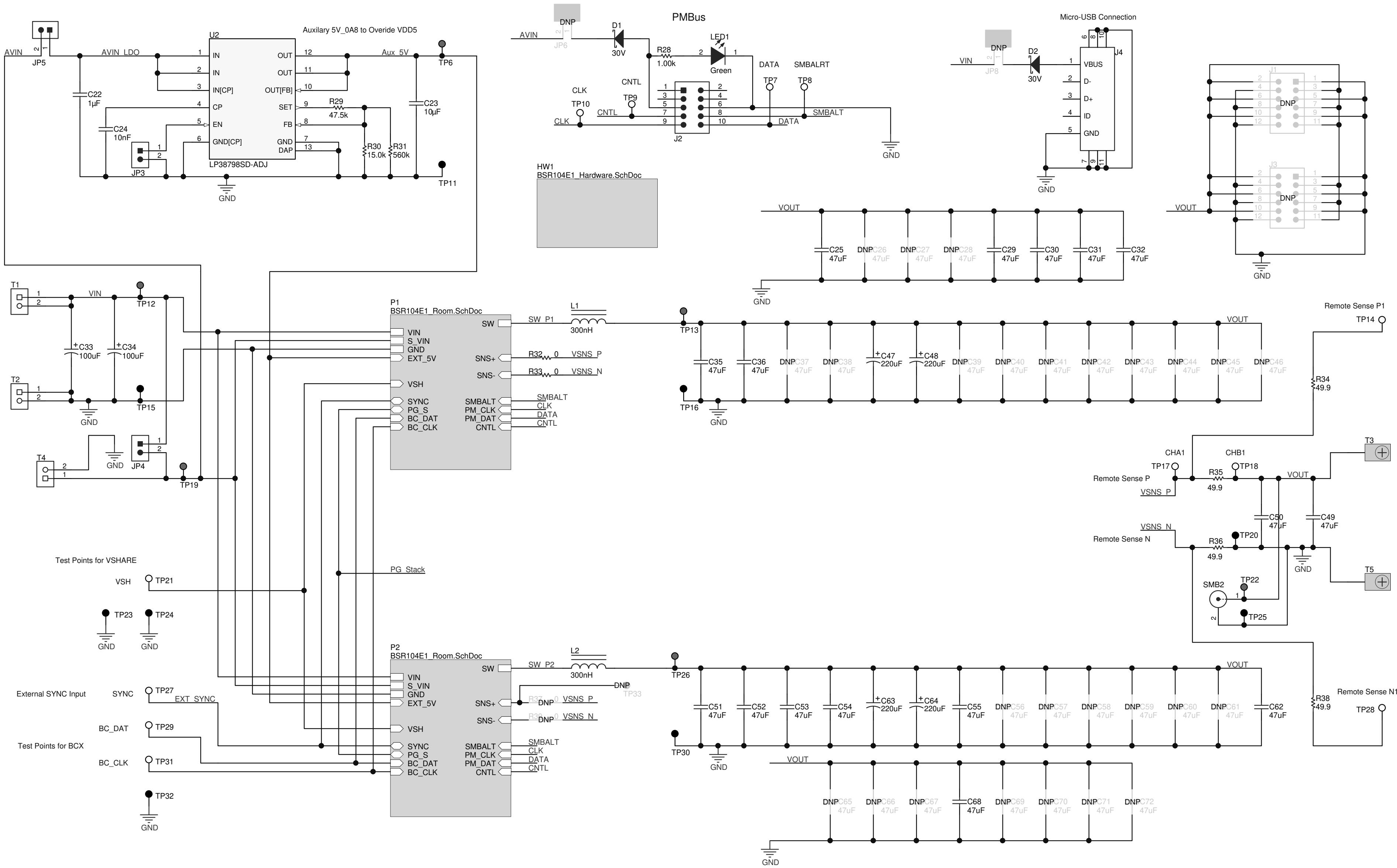


Figure 3-1. TPS546B24AEVM-2PH Schematic Page 1

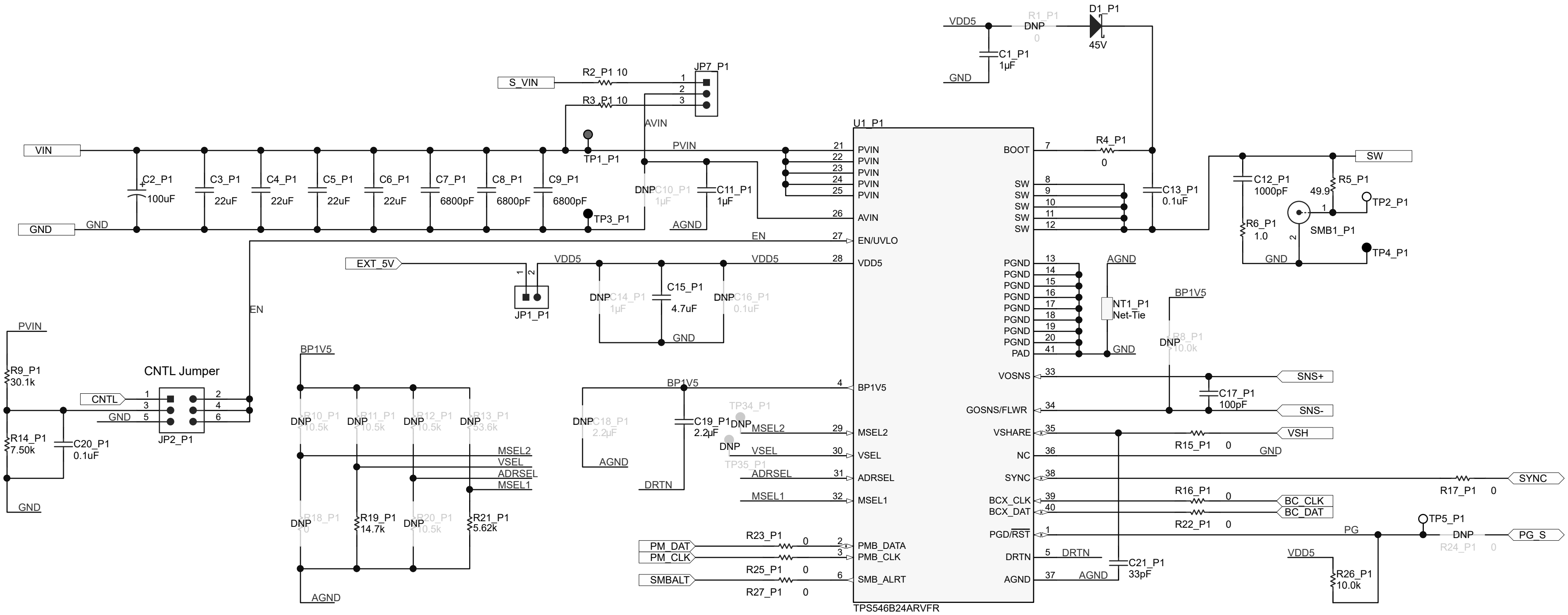


Figure 3-2. TPS546B24AEVM-2PH Schematic Page 2 (U1_P1 Loop Controller)

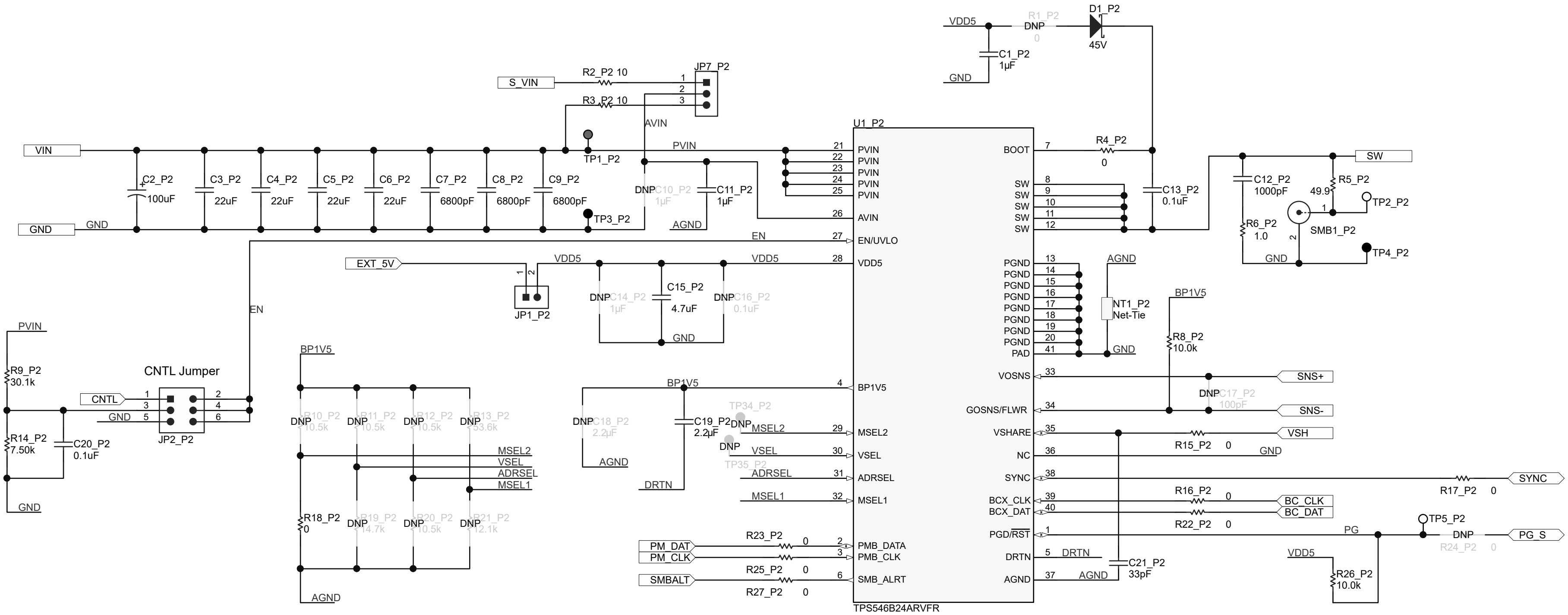


Figure 3-3. TPS546B24AEVM-2PH Schematic Page 3 (U1_P2 Loop Follower)

4 Test Setup

4.1 Test and Configuration Software

To change any of the default configuration parameters on the EVM through PMBus, obtain the *TI Fusion Digital Power Designer* software.

4.1.1 Description

The *TI Fusion Digital Power Designer* is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPS546B24A power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter described in Section 4.2.6.

4.1.2 Features

Some of the tasks the user can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data that is continuously monitored and displayed by the GUI:
  - Input voltage
  - Output voltage
  - Output current
  - Die temperature
  - Warnings and faults
- Configure common operating characteristics such as the following:
  - V_{OUT} trim and margin
  - UVLO
  - Soft-start time
  - Warning and fault thresholds
  - Fault response
  - On/off modes

4.2 Test Equipment

4.2.1 Voltage Source

The input voltage source, V_{IN}, should be a 0-V to 20-V variable DC source capable of supplying a minimum of 8 ADC to support 40-A load with 5-V input. Connect input VIN and GND to T1 and T2. If the output voltage of the EVM is increased, the power supply may need to be capable of supplying more current.

4.2.2 Multimeters

TI recommends using two separate multimeters: one meter to measure V_{IN} and the other to measure V_{OUT}.

4.2.3 Output Load

A variable electronic load is recommended for the test setup. To test the full load current this EVM supports, the load should be capable of sinking at least 40 A.

4.2.4 Oscilloscope

When using an oscilloscope to measure the switching node voltage or voltage ripple, measure using a *Tip-and-Barrel* method as Figure 4-1 shows, or better.

4.2.5 Fan

During prolonged operation at high loads, it can be necessary to provide forced air cooling with a small fan aimed at the EVM. Maintain the surface temperature of the devices on the EVM below their rated temperature.

4.2.6 USB-to-GPIO Interface Adapter

A communications adapter is required between the EVM and the host computer. This EVM is designed to use TI's USB-to-GPIO adapter. Purchase this adapter at http://www.ti.com/tool/usb-to-gpio.

4.2.7 Recommended Wire Gauge

- Input VIN and GND to T1 and T2 (GND) (12-V input) – The recommended wire size is AWG #12, with the total length of wire less than two feet (1-foot input, 1-foot return).
- Output T3 and GND T5 (0.8-V output) – The minimum recommended wire size is AWG #10 with the total length of wire less than two feet (1-foot output, 1-foot return). A thicker wire gauge can be required to minimize the voltage drop the wires.

4.3 Tip and Barrel Measurement

Figure 4-1 illustrates the tip and barrel measurement for switching node waveform on TP2_P1 with TP4_P1 or TP2_P2 with TP4_P2.

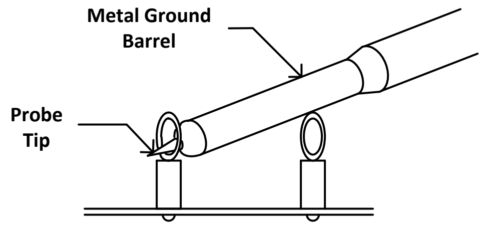


Figure 4-1. Tip and Barrel Measurement

4.4 List of Test Points, Jumpers, and Connectors

Table 4-1 lists the test point functions.

Table 4-1. Test Point Functions

Test Point	Type	Name	Description
TP1_P1	T-H Loop	PVIN_P1	PVIN pin voltage of U1_P1 device measurement point
TP1_P2	T-H Loop	PVIN_P2	PVIN pin voltage of U1_P2 device measurement point
TP2_P1	T-H Loop	SW_P1	Switching node of output rail phase 1 measurement point, reference to TP4_P1
TP2_P2	T-H Loop	SW_P2	Switching node of output rail phase 2 measurement point, reference to TP4_P2
TP3_P1	T-H Loop	GND_P1	GND pin voltage of U1_P1 device measurement point
TP3_P2	T-H Loop	GND_P2	GND pin voltage of U1_P2 device measurement point
TP4_P1	T-H Loop	GND_P1	GND reference for switch node measurement of U1_P1
TP4_P2	T-H Loop	GND_P2	GND reference for switch node measurement of U1_P2
TP5_P1	T-H Loop	PG_S_P1	PGOOD signal of phase 1
TP5_P2	T-H Loop	PG_S_P2	PGOOD signal of phase 2
TP6	T-H Loop	AUX_5V	External 5-V measurement point for VDD5
TP7	T-H Loop	DATA	DATA signal on J2 header
TP8	T-H Loop	SMBALRT	SMBALERT signal on J2 header
TP9	T-H Loop	CNTL	CNTL signal on J2 header
TP10	T-H Loop	CLK	CLK signal on J2 header
TP11	T-H Loop	GND	GND reference
TP12	T-H Loop	PVIN	VIN + measurement point
TP13	T-H Loop	VOUT_P1	U1_P1 output voltage measurement point for efficiency, reference to TP16
TP14	T-H Loop	Remote SNS+	OUTPUT remote sense + voltage point
TP15	T-H Loop	GND	VIN- measurement point
TP16	T-H Loop	GND_P1	U1_P1 output voltage referencing GND for efficiency measurement
TP17	T-H Loop	CH_A	OUTPUT for small signal loop gain measurements (B/A setup)
TP18	T-H Loop	CH_B	INPUT for small signal loop gain measurements (B/A setup)
TP19	T-H Loop	Ext_AVIN	AVIN measurement point
TP20	T-H Loop	GND	GND reference
TP21	T-H Loop	VSHARE	VSHARE measurement point. Sensitive signal

Table 4-1. Test Point Functions (continued)

Test Point	Type	Name	Description
TP22	T-H Loop	VOUT	VOUT + measurement point
TP23	T-H Loop	GND	GND reference
TP24	T-H Loop	GND	GND reference
TP25	T-H Loop	GND	VOUT – measurement point
TP26	T-H Loop	VOUT_P2	U1_P2 output voltage measurement point for efficiency, reference to TP30
TP27	T-H Loop	SYNC	Synchronization connection between U1_P1 and U1_P2. External SYNC input
TP28	T-H Loop	Remote SNS–	OUTPUT remote sense – voltage point
TP29	T-H Loop	BC_DAT	Data for back-channel communications between stacked devices
TP30	T-H Loop	GND_P2	U1_P2 output voltage referencing GND for efficiency measurement
TP31	T-H Loop	BC_CLK	Clock for back-channel communications between stacked devices
TP32	T-H Loop	GND	GND reference
TP33	T-H Loop	VOSNS_P2	VOSNS measurement point for U1_P2
TP34_P1, TP34_P2	T-H Loop	MSEL2_P1, MSEL2_P2	MSEL2 measurement point for U1_P1 and U1_P2
TP35_P1, TP35_P2	T-H Loop	VSEL_P1, VSEL_P2	VSEL measurement point for U1_P1 and U1_P2

Table 4-2 lists the EVM jumpers.

Table 4-2. Jumpers

Jumper	Type	Name	Description
JP1_P1, JP1_P2	Header, 100 mil, 2 × 1	EXT_5.1V_P1, EXT_5.1V_P2	Short to connect VDD5 of U1_P1 or U1_P2 to the 5.1 V from U2
JP2_P1, JP2_P2	Header, 100 mil, 3 × 2	CNTL_SEL1, CNTL_SEL2	U1_P1 and U1_P2 EN/UVLO pin selections
JP3	Header, 100 mil, 2 × 1	EN to GND	Short to disable the auxiliary 5 V
JP4	Header, 100 mil, 2 × 1	AVIN-PVIN	Short to connect to connect AVIN input to PVIN
JP5	Header, 100 mil, 2 × 1	AVIN-LDO	Short to connect to connect AVIN input to U2 input
JP6	Header, 100 mil, 2 × 1	PMBus3.3V-AVIN	Short to connect USB-to-GPIO 3.3 V to AVIN
JP7_P1, JP7_P2	Header, 100 mil, 3 × 1	AVIN-U1_P1, AVIN-U1_P2	U1_P1 and U1_P2 AVIN input source selections
JP8	Header, 100 mil, 2 × 1	Micro_USB-PVIN	Short to connect PVIN to Micro USB connector

Table 4-3 lists the options for the EN/UVLO pin selections on JP2_P1 and JP2_P2.

Table 4-3. JP2_P1 and JP2_P2 Selections

Shunt Position	Selection
Pin 1 to 2 shorted	PMBus adaptor control signal
Pin 3 to 4 shorted	Resistor divider to PVIN
Pin 5 to 6 shorted	EN/UVLO short to ground

Table 4-4 lists the options for the EN/UVLO pin selections on JP2_P1 and JP2_P2.

Table 4-4. JP7_P1 and JP7_P2 Selections

Shunt Position	Selection
Pin 1 to 2 shorted	AVIN pin connected to AVIN input through 10-Ω resistor. Use this selection when testing with a split rail input.
Pin 2 to 3 shorted	AVIN pin connected to PVIN through 10-Ω resistor

Table 4-5 lists the EVM connector functions.

Table 4-5. Connector Functions

Connector	Type	Name	Description
J1	Header, 100 mil, 6 × 2	N/A	Do not use
J2	Header, 100 mil, 5 × 2	PMBus connector	PMBus socket for TI FUSION adaptor
J3	Header, 100 mil, 6 × 2	N/A	Do not use
J4	Micro USB	Micro USB	Micro USB connector to power EVM from a 5 V USB source
T1	Terminal block, 2 × 1	PVIN	VIN+ connector
T2	Terminal block, 2 × 1	GND	VIN– connector
T3	Terminal 90A Lug	VOUT	VOUT+ connector
T4	Terminal block, 2 × 1	Ext_AVIN	External AVIN connector
T5	Terminal 90A Lug	GND	VOUT– connector

4.5 Evaluating Single Phase Operation

The default configuration of the EVM is for 2-phase operation. For a single-phase operation, modify the EVM as follows:

1. Short MSEL2 of U1_P1 to GND to program single-phase operation by populating R18_P1 with a 0-Ω resistor.
2. If U1_P2 is left populated, disconnect VSHARE of the loop follower device from the loop controller by depopulating R15_P1 (this is a 0-Ω resistor and can be used for MSEL2 pin of U1_P1 in the previous step).
3. If U1_P2 is left populated, disable U1_P2 by moving the JP2_P2 jumper to position 5-6 (GND).

Note

This will leave the AVIN (pin 26) of U1_P2 powered. If no-load leakage current or light-light efficiency measurement is important, the U1_P2 AVIN pin should also be disconnected from the input supply. Disconnect the loop follower U1_P2 AVIN from V_{IN} by removing the jumper from JP7_P2.

4.6 Evaluating Split Rail Input

The default configuration of the EVM is for single rail input. Split rail input enables operation with 3.3-V PVIN. For split rail operation, configure the jumpers on the EVM as follows:

1. Open JP4 to disconnect AVIN from PVIN.
2. Move the jumper JP7_P1 and JP7_P2 to position 1-2 to disconnect the AVIN pin from the PVIN pins.
3. Apply the AVIN input to T4. 4-V or greater AVIN is required to bring the VDD5 voltage high enough to enable conversion.
4. If operation with 3.3-V PVIN is needed and the CNTL jumpers (JP2_P1 and JP2_P2) are in position 3-4, the resistor divider at the EN/UVLO will need to be changed. Alternately, move the CNTL jumpers to position 1-2 and use the control signal to enable conversion or use the ON_OFF_CONFIG and OPERATION commands to enable conversion.

4.7 Configuring EVM to Overdrive VDD5

The EVM has an external LDO (U2) that can be used to overdrive VDD5. The output of this LDO is set for 5.1 V by default. This LDO is useful to minimize the power dissipation in the TPS546B24A IC when using a single rail input. Overdriving VDD5 moves the loss from the internal LDO of the TPS546B24A to the external LDO (U2). To use this LDO, configure the jumpers on the EVM as follows:

1. Short JP4 and JP5 to connect the input of the LDO to the input supply.
2. Open JP3 to enable the LDO.
3. Short JP1_P1 and JP1_P2 to connect the LDO output to the VDD5 pin.
4. Ensure the VDD5 output of the TPS546B24A is set below the external output voltage of the LDO.

5 EVM Configuration Using the Fusion GUI

The TPS546B24A IC leaves the factory pre-configured. The factory default settings for the parameters can be found in the data sheet. If configuring the EVM to settings other than the factory defaults, use the software described in Section 4.1. It is necessary to have the input voltage applied to the EVM prior to launching the software so that the TPS546B24A can respond to the GUI and the GUI can recognize the device. The default configuration for the EVM to stop converting is set by the EN/UVLO resistor divider to a nominal input voltage of 4.75 V; therefore, if it is necessary to avoid any converter activity during configuration, an input voltage less than 4.75 V should be applied. TI recommends an input voltage of 3.3 V.

5.1 Configuration Procedure

1. Adjust the input supply to provide 3.3 V_{DC}, current limited to 1 A.
2. Apply the input voltage to the EVM. See Section 4.2 for connections and test setup.
3. Launch the Fusion GUI software. See the screen shots in Section 10 for more information.
4. Configure the EVM operating parameters as desired.

By default, the pinstrap resistors configure U1_P1 as the loop controller and U1_P2 as the loop follower.

6 Test Procedure

6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as Section 4.2 and Section 6.2 describe.
2. Set the electronic load to draw 0 A_{DC}.
3. Increase V_{IN} from 0 V to 12 V using voltage meter to measure input voltage.
4. Use the other voltage meter to measure output voltage V_{OUT}.
5. Vary the load from 0 to 40 A_{DC}. V_{OUT} should remain in regulation as defined in Table 2-1.
6. Vary V_{IN} from 5 V to 18 V. V_{OUT} should remain in regulation as defined in Table 2-1.
7. Decrease the load to 0 A.
8. Decrease V_{IN} to 0 V.

6.2 Efficiency Measurement Test Points

To evaluate the efficiency of the power train (device and inductor), it is important to measure the voltages at the correct location. This is necessary because otherwise the measurements will include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which should not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

Table 6-1 shows the measurement points for input voltage and output voltage. VIN and VOUT are measured to calculate the efficiency. Using these measurement points will result in efficiency measurements that excluded losses due to the wires and connectors.

Table 6-1. Test Points for Efficiency Measurements

Test Point	Node Name	Description	Comment
TP12	PVIN	Input voltage measurement point for VIN+	The pair of test points is connected to the PVIN/PGND pins of U1_P1. The voltage drop between input terminal to the device pins is included for efficiency measurement.
TP15	PGND	Input voltage measurement point for VIN– (GND)	
TP22	VOUT	Output voltage measurement point for VOUT+	The pair of test points is connected near the output terminals. The voltage drop from the output point of the inductor to the output terminals is included for efficiency measurement.
TP25	GND	Output voltage measurement point for VOUT– (GND)	

For more accurate efficiency measurements of the power train, the voltage drop between the power train and the terminals should also be removed from the measurement. Using the test points in Table 6-2 will reduce these losses. To average the voltages at each test point so that only one meter is needed for PVIN and VOUT, add some resistance between the each test point and the meter. For the measurements taken in this user's guide, a 1.5-kΩ resistor was added in series with each test point. Using these test points reduced the measured power loss at 40 A load by approximately 0.15 W. This power is lost in the copper traces of the PCB.

Table 6-2. Test Points for Better Efficiency Measurements

Test Point	Node Name	Description	Comment
TP1_P1	PVIN_P1	Input voltage measurement point for VIN+	This pair of test points is connected to PVIN and PGND near the pins of U1_P1.
TP4_P1	GND_P1	Input voltage measurement point for VIN– (PGND)	
TP1_P2	PVIN_P2	Input voltage measurement point for VIN+	This pair of test points is connected to PVIN and PGND near the pins of U1_P2.
TP4_P2	GND_P2	Input voltage measurement point for VIN– (PGND)	
TP13	VOUT_P1	Output voltage measurement point for VOUT+	This pair of test points is connected to VOUT and GND near the output inductor for U1_P1.
TP16	GND_P1	Output voltage measurement point for VOUT– (GND)	
TP26	VOUT_P2	Output voltage measurement point for VOUT+	This pair of test points is connected to VOUT and GND near the output inductor for U1_P2.
TP30	GND_P2	Output voltage measurement point for VOUT– (GND)	

6.3 Control Loop Gain and Phase Measurement Procedure

The TPS546B24AEVM-2PH includes a 49.9-Ω series resistor in the feedback loop for V_{OUT}. The resistor is accessible at the test points TP17 and TP18 for loop response analysis. These test points should be used during loop response measurements as the perturbation injecting points for the loop. See the description in Table 6-3.

Table 6-3. List of Test Points for Loop Response Measurements

Test Point	Node Name	Description	Comment
TP18	CH_B	Input to feedback divider of V_{OUT}	The amplitude of the perturbation at this node should be limited to less than 30 mV.
TP17	CH_A	Resulting output of V_{OUT}	Bode can be measured by a network analyzer with a CH_B/CH_A configuration.

Measure the loop response with the following procedure:

1. Set up the EVM as described in Section 4.2.
2. For V_{OUT}, connect the isolation transformer of the network analyzer from TP18 to TP17.
3. Connect the input signal measurement probe to TP18. Connect the output signal measurement probe to TP17.
4. Connect the ground leads of both probe channels to TP20.
5. On the network analyzer, measure the Bode as TP18/TP17 (In/Out).

7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-4 present typical performance curves for the TPS546B24AEVM-2PH. The input voltage is 12 V and the oscilloscope measurements use 20-MHz bandwidth limiting, unless otherwise noted.

7.1 Efficiency

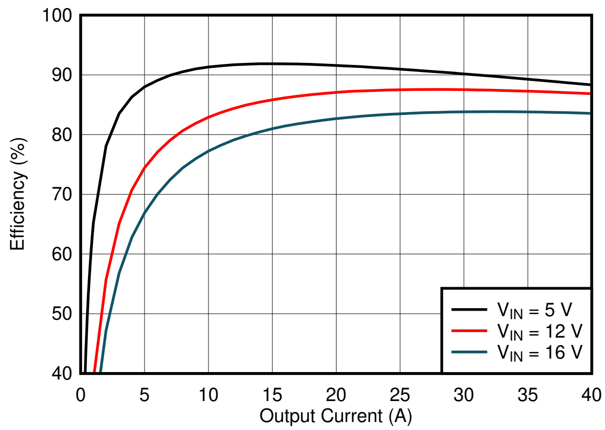


Figure 7-1. Efficiency, V_{OUT} Measured Using TP13, TP16, TP26, and TP30

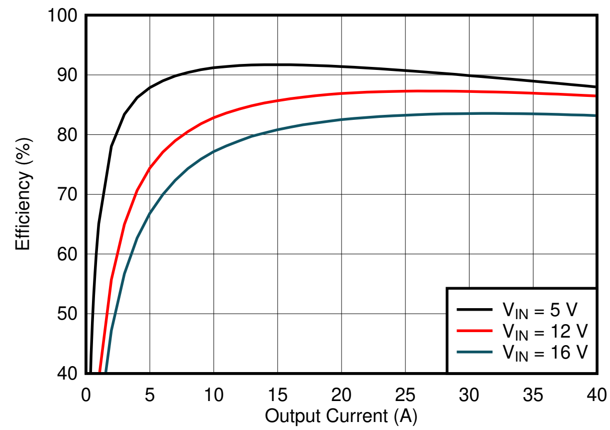


Figure 7-2. Efficiency, V_{OUT} Measured Using TP22 and TP25

7.2 Load and Line Regulation (Measured Between TP22 and TP25)

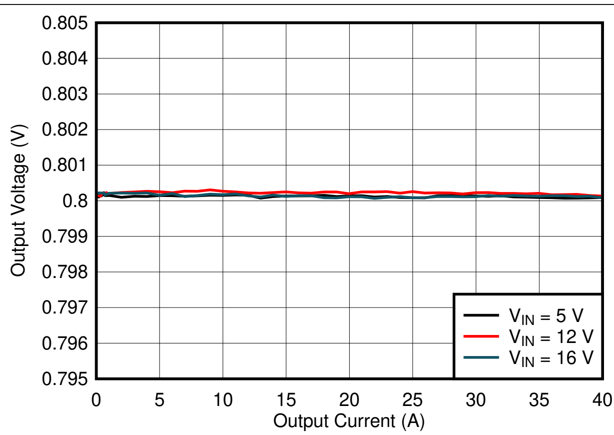


Figure 7-3. Load Regulation

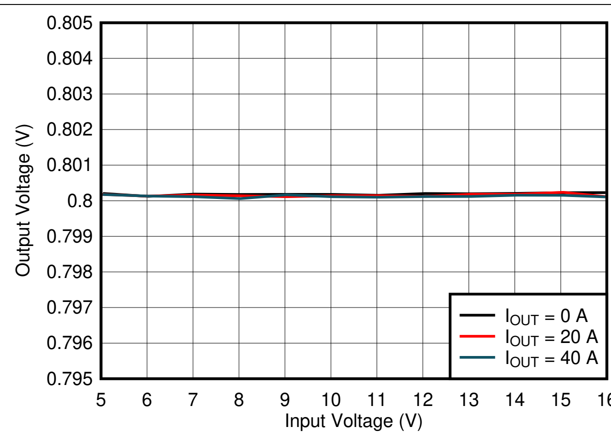


Figure 7-4. Line Regulation

7.3 Transient Response

Figure 7-5 shows the transient response waveform with a 10-A to 30-A transient at 10 A/μs.

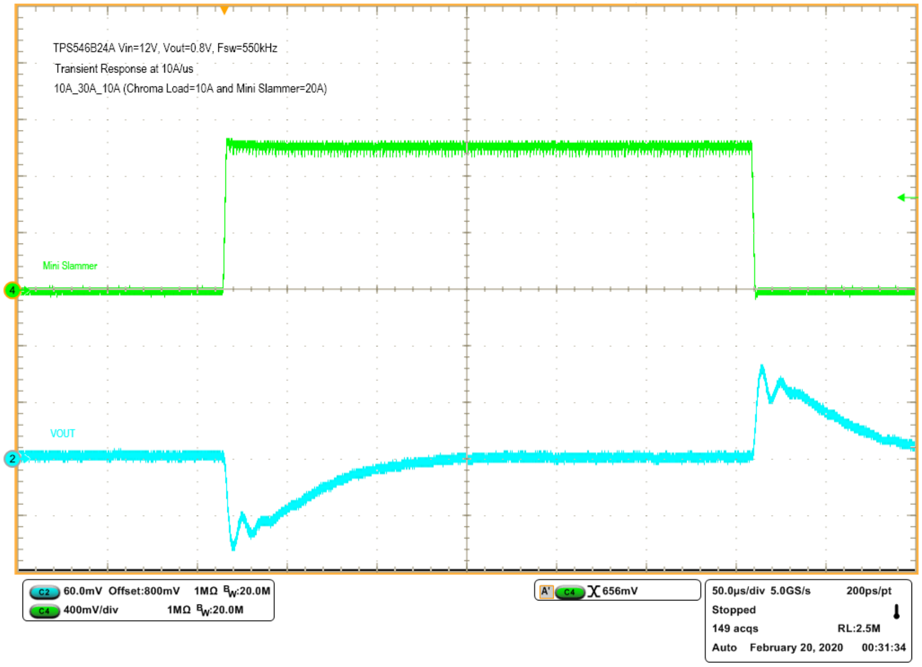


Figure 7-5. Transient Response

7.4 Control Loop Bode Plot

Figure 7-6 is the control loop bode plot.

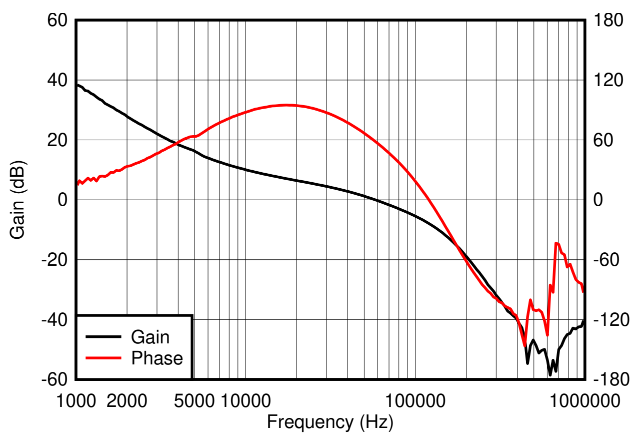


Figure 7-6. Bode Plot at 0.8-V Output at 12 V_{IN}, 20-A Load

7.5 Output Ripple

Figure 7-7 and Figure 7-8 show the output ripple waveforms at 0-A and 40-A load.

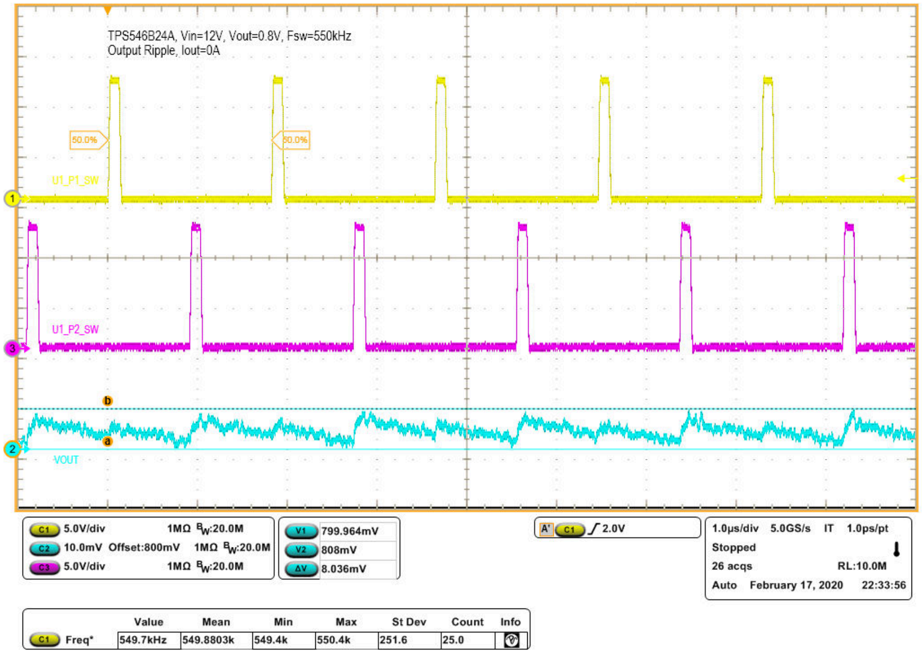


Figure 7-7. Output Ripple With 0-A Load

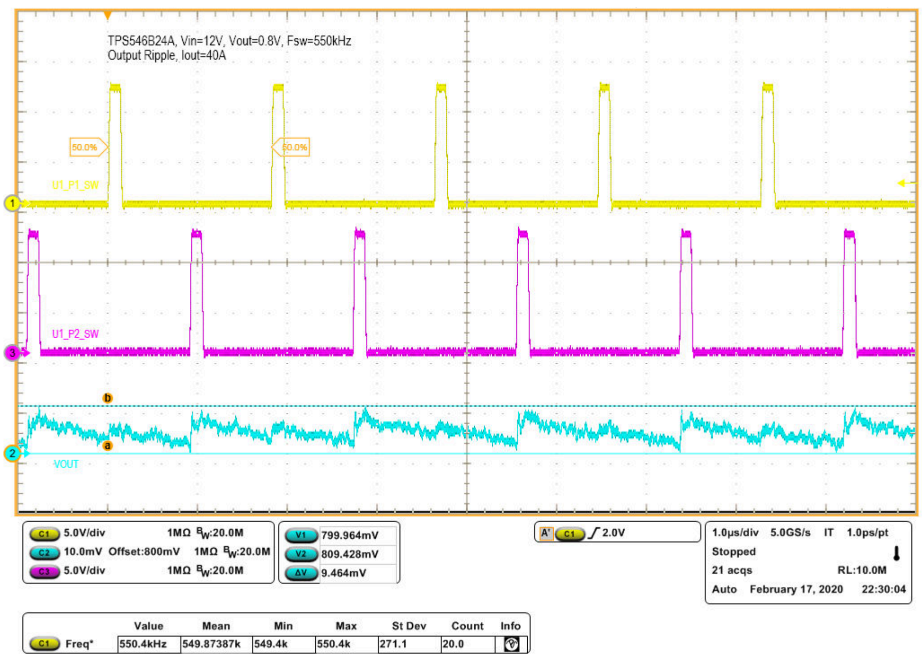


Figure 7-8. Output Ripple With 40-A Load

7.6 Power MOSFET Drain-Source Voltage

Figure 7-9 and Figure 7-10 show the low-side and high-side MOSFET drain-source voltage (V_{DS}) at 40-A load. The voltage is measured with 1-GHz bandwidth and at the solder mask openings near the U1_P1 IC using a 1-GHz differential probe.

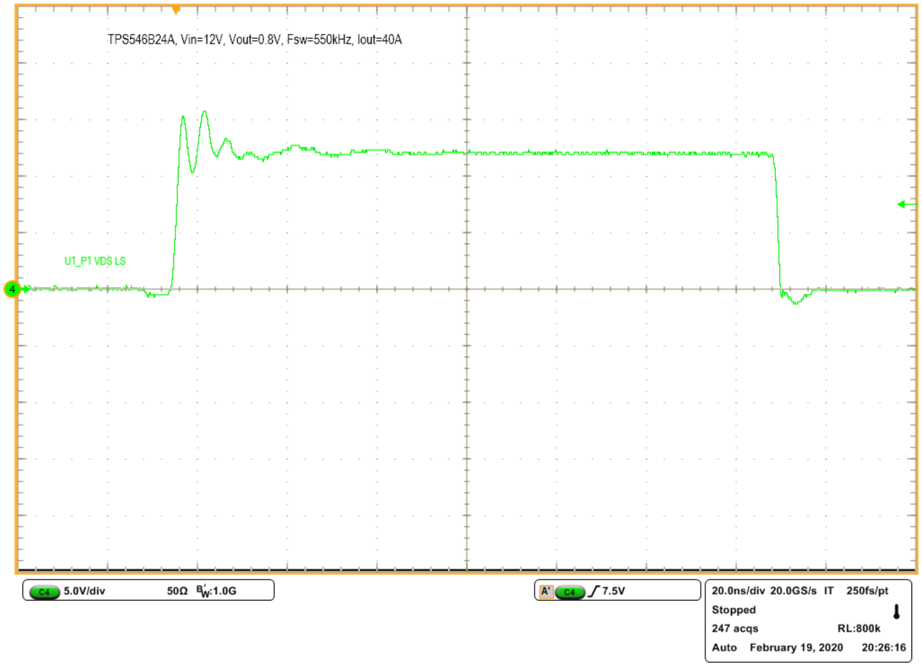


Figure 7-9. Low-Side MOSFET V_{DS}

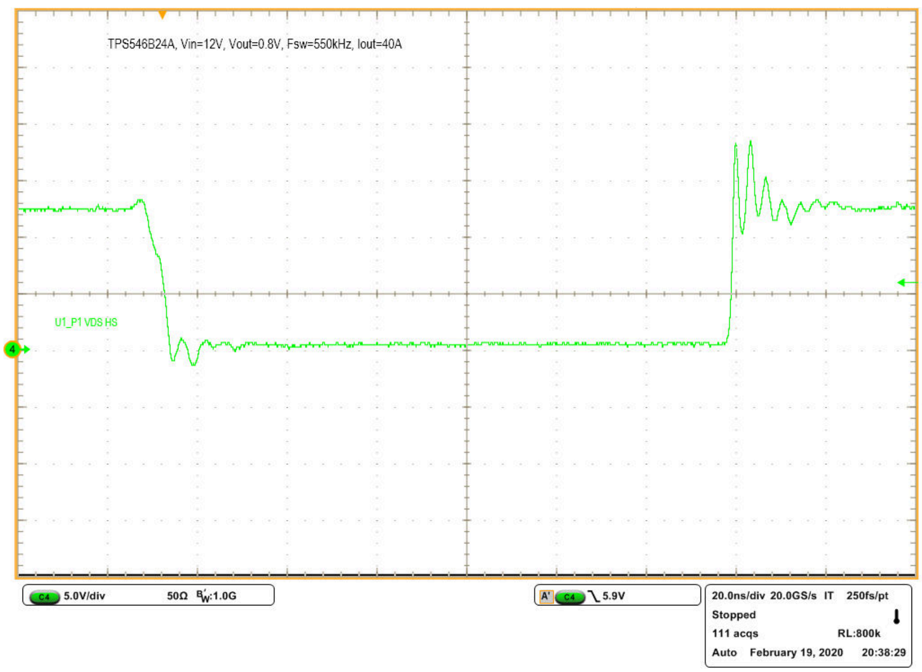


Figure 7-10. High-Side MOSFET V_{DS}

7.7 Control On

Figure 7-11 and Figure 7-12 illustrate the start-up from control on waveforms at 0-A and 40-A output.

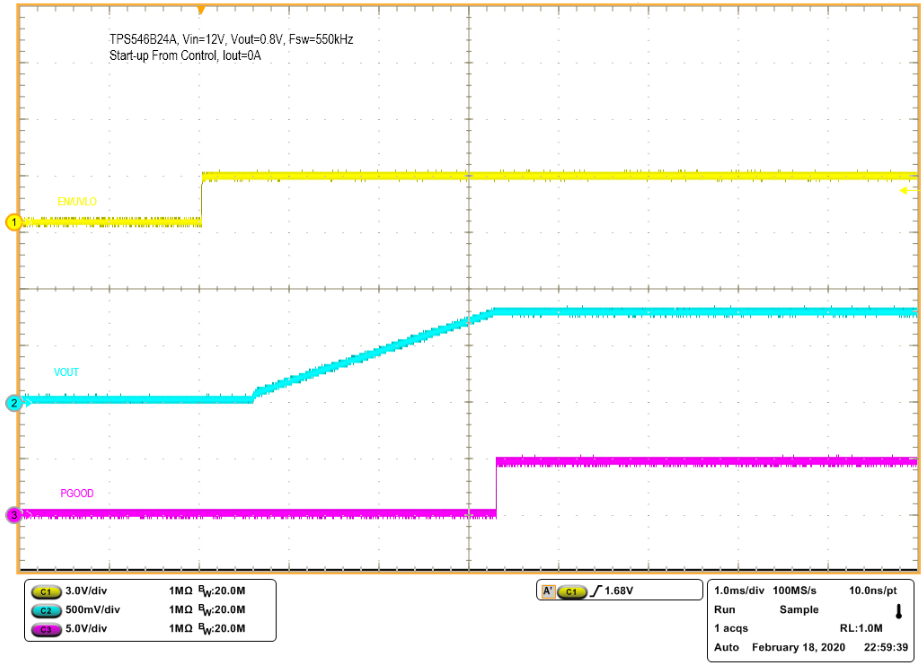


Figure 7-11. Start-Up From Control, 0-A Load

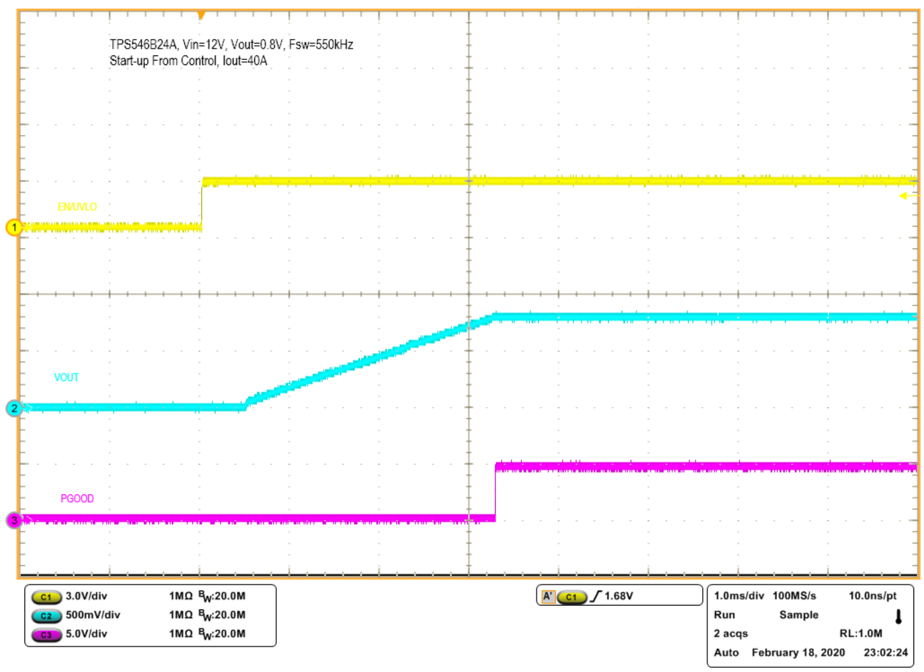


Figure 7-12. Start-Up From Control, 40-A CC Load

7.8 Control Off

Figure 7-13 and Figure 7-14 illustrate the control off waveforms at 0-A and 20-A outputs, respectively.

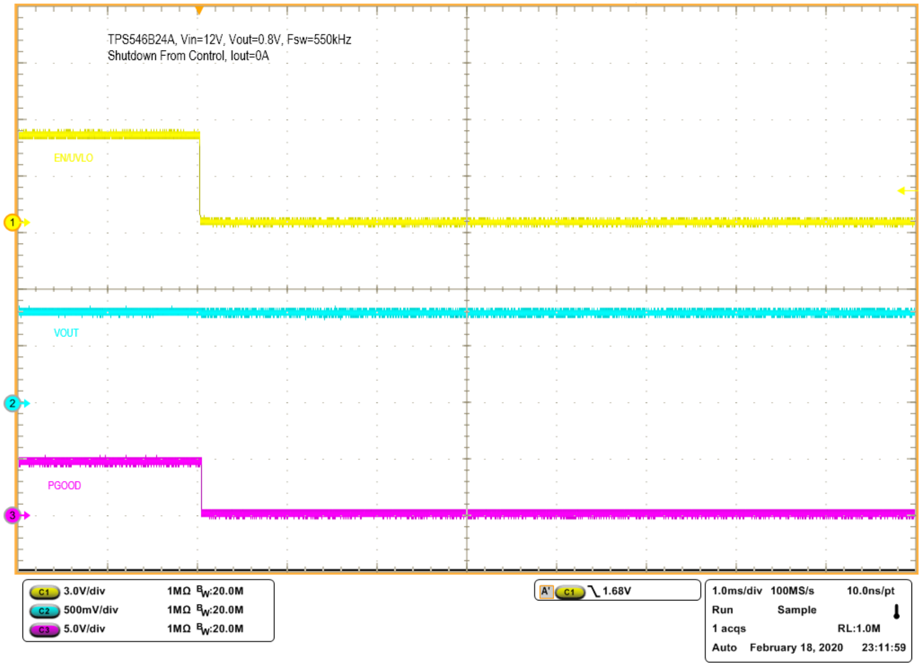


Figure 7-13. Shutdown From Control, 0-A Load

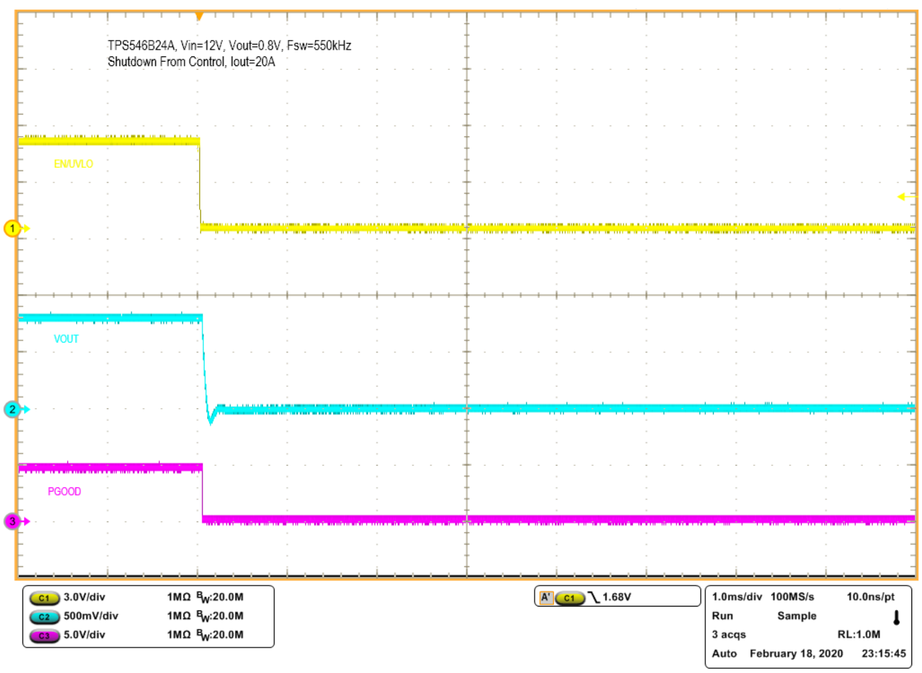


Figure 7-14. Shutdown From Control, 20-A CC Load

7.9 Control On with Pre-Biased Output

Figure 7-15 illustrates the control on waveforms with a pre-biased output voltage.

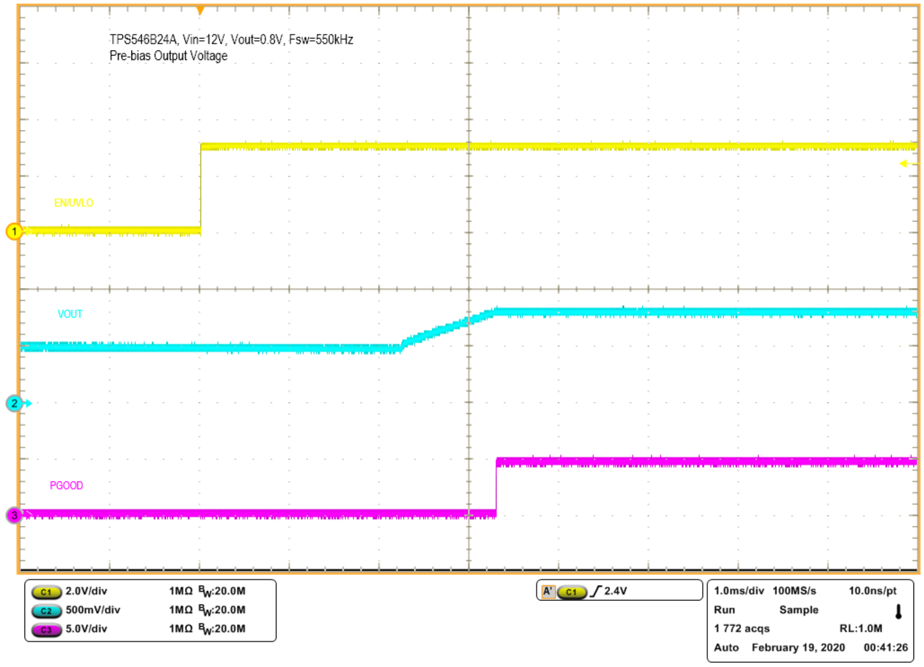


Figure 7-15. Start-Up From Control With Pre-Biased Output

7.10 Current Sharing Between Two Phases

Figure 7-16 illustrates the current sharing between two phases.

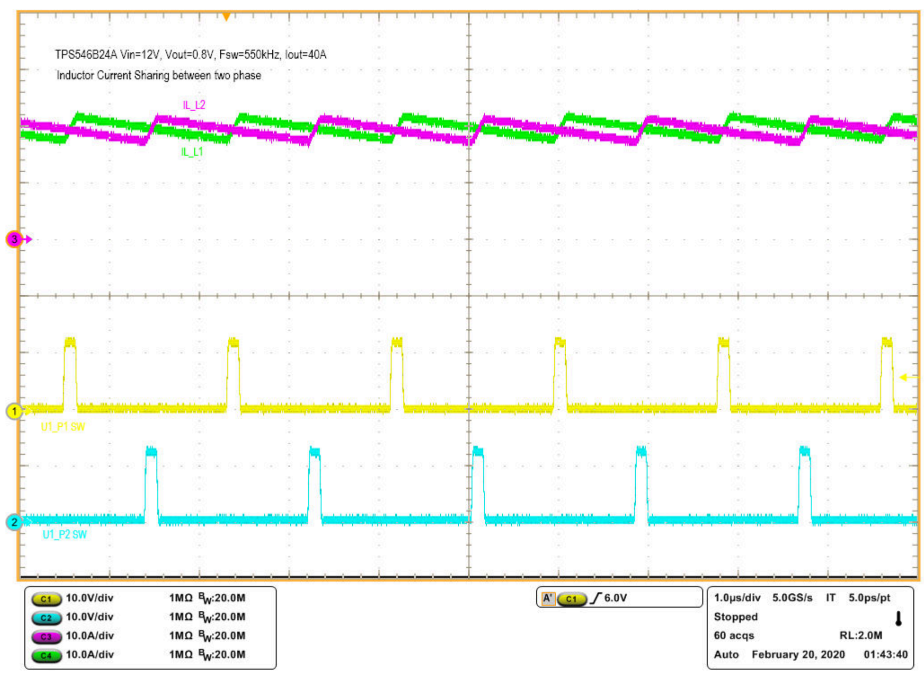
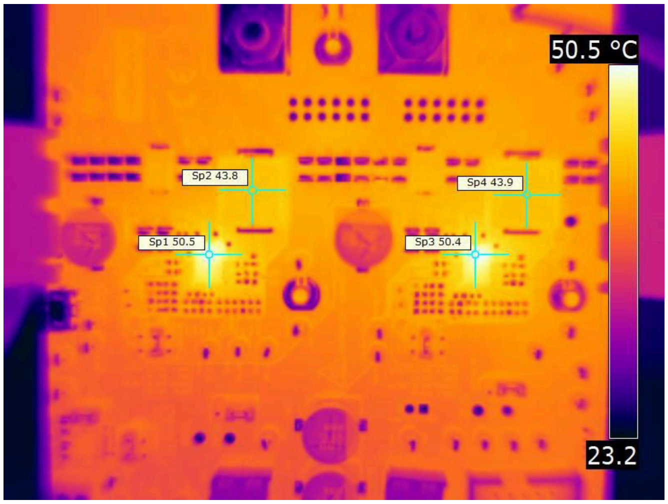


Figure 7-16. Inductor Current and Switch Node Waveform, 40-A Load

7.11 Thermal Image

Figure 7-17 shows the TPS546B24AEVM-2PH thermal image.



V_{IN} = 12 V, I_{OUT} = 40 A

Figure 7-17. Thermal Image

8 EVM Assembly Drawing and PCB Layout

Figure 8-3 through Figure 8-10 show the design of the TPS546B24AEVM-2PH printed circuit board.

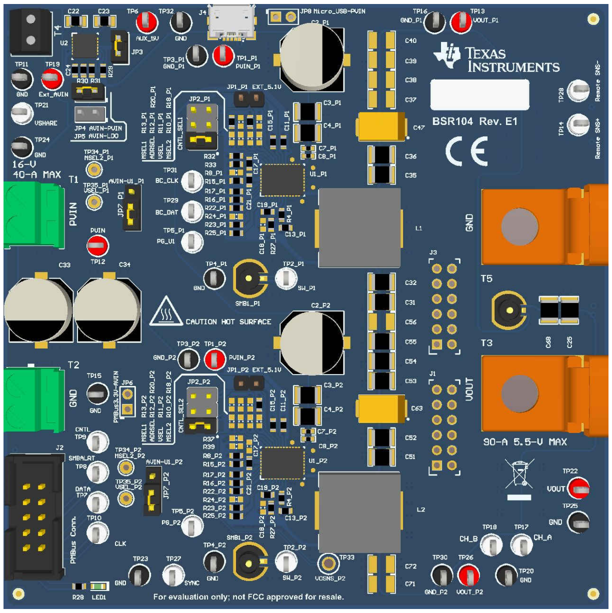


Figure 8-1. TPS546B24AEVM-2PH 3D (Top View)

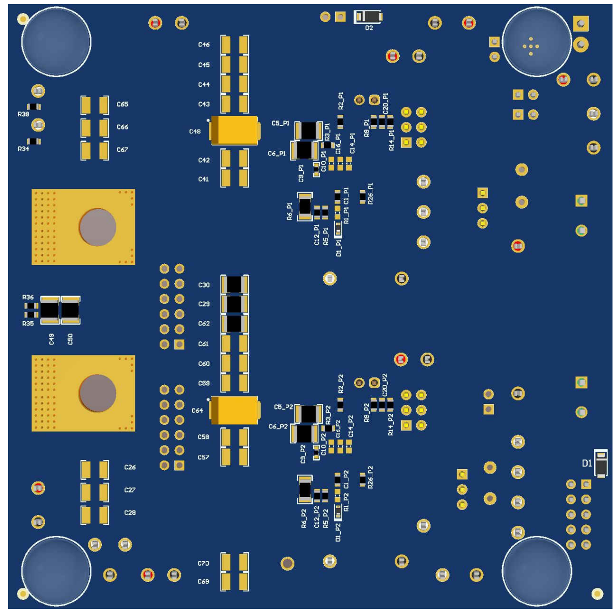


Figure 8-2. TPS546B24AEVM-2PH 3D (Bottom View)

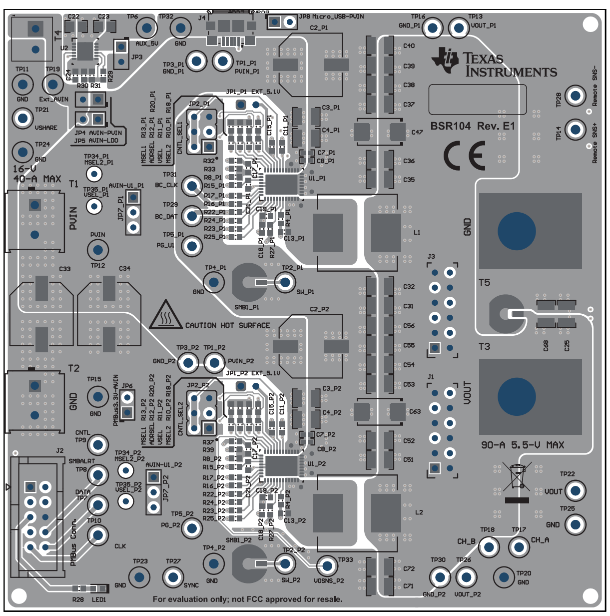


Figure 8-3. TPS546B24AEVM-2PH Top Side Component View (Top View)

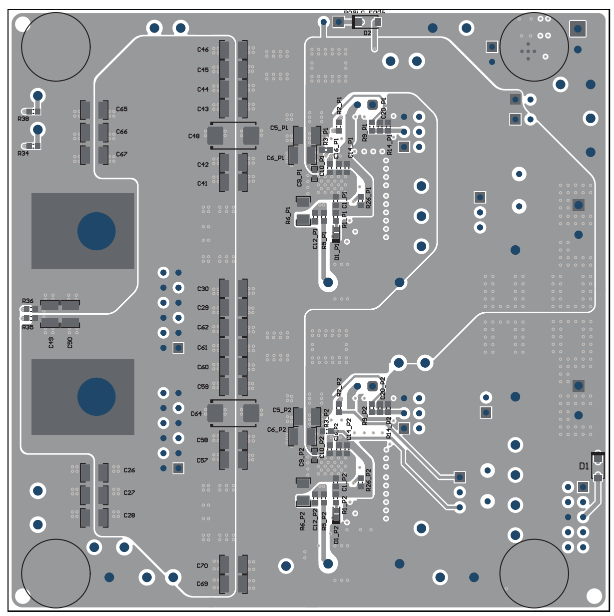


Figure 8-4. TPS546B24AEVM-2PH Bottom Side Component View (Bottom View)

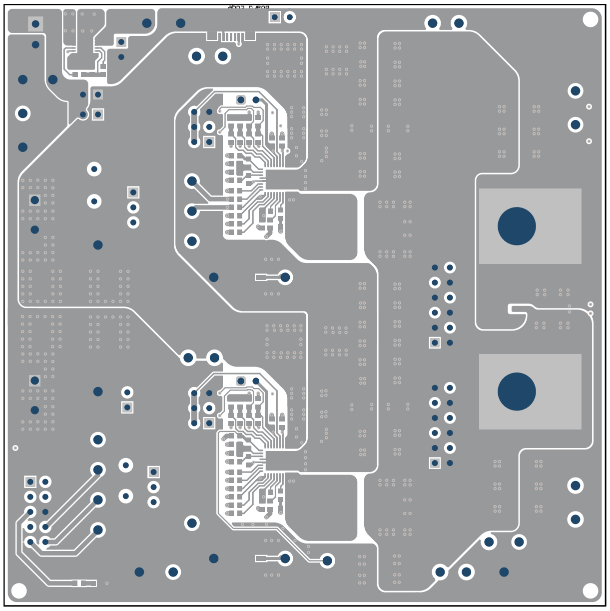


Figure 8-5. TPS546B24AEVM-2PH Top Copper (Top View)

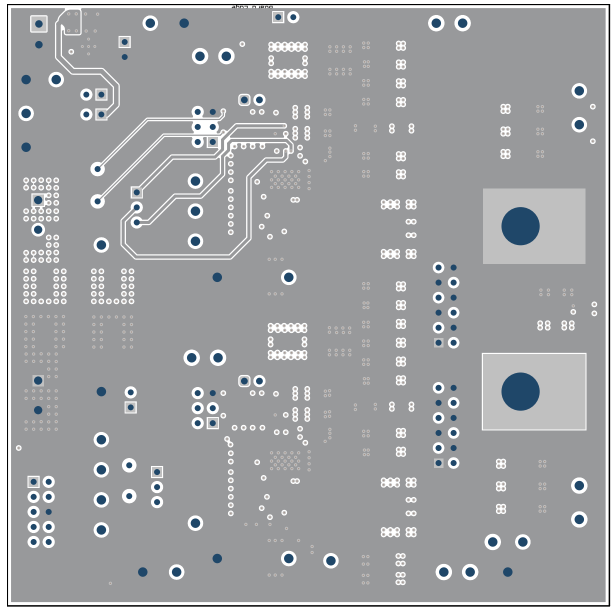


Figure 8-6. TPS546B24AEVM-2PH Internal Layer 1 (Top View)

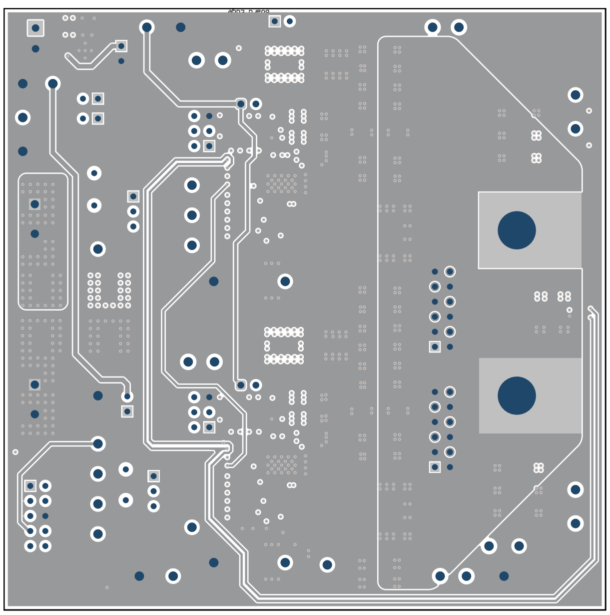


Figure 8-7. TPS546B24AEVM-2PH Internal Layer 2 (Top View)

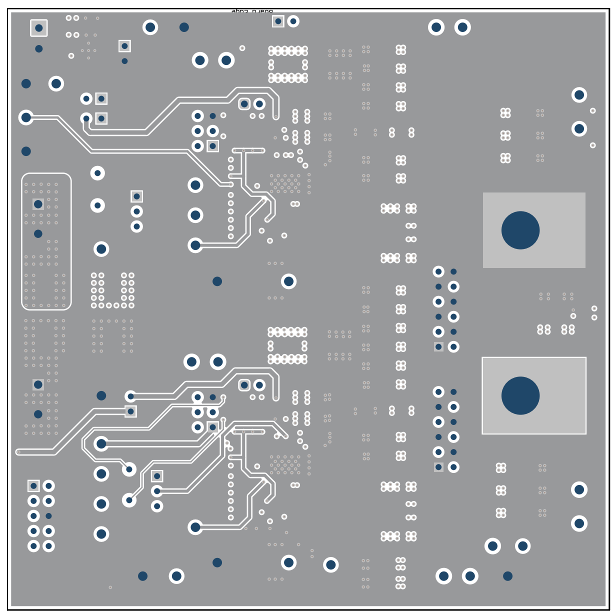


Figure 8-8. TPS546B24AEVM-2PH Internal Layer 3 (Top View)

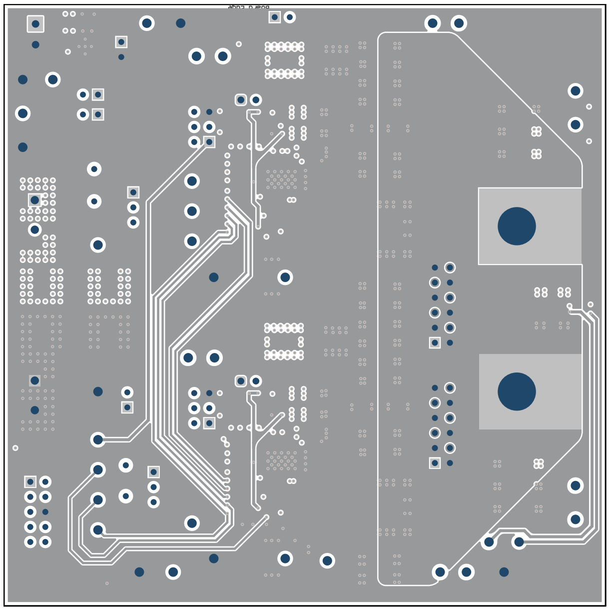


Figure 8-9. TPS546B24AEVM-2PH Internal Layer 4 (Top View)

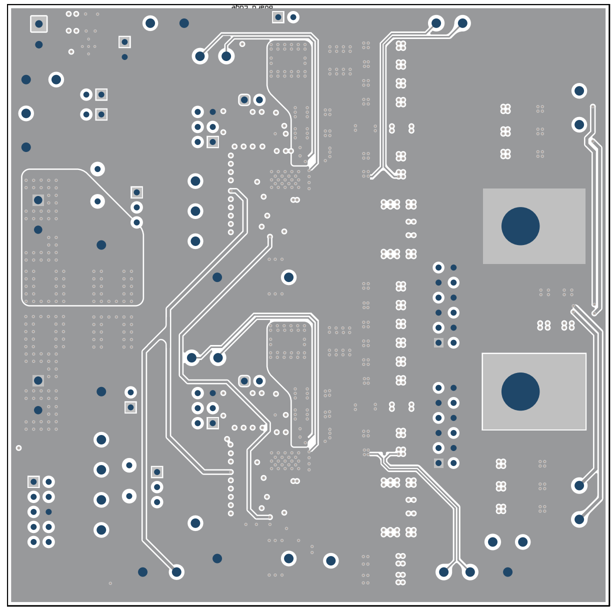


Figure 8-10. TPS546B24AEVM-2PH Internal Layer 5 (Top View)

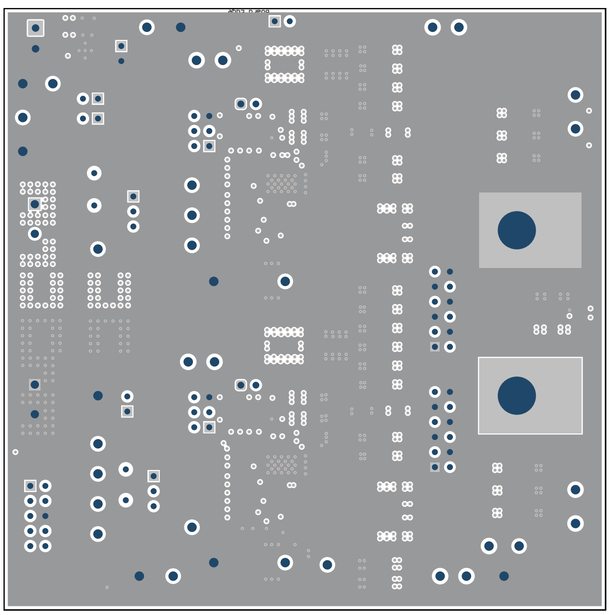


Figure 8-11. TPS546B24AEVM-2PH Internal Layer 6 (Top View)

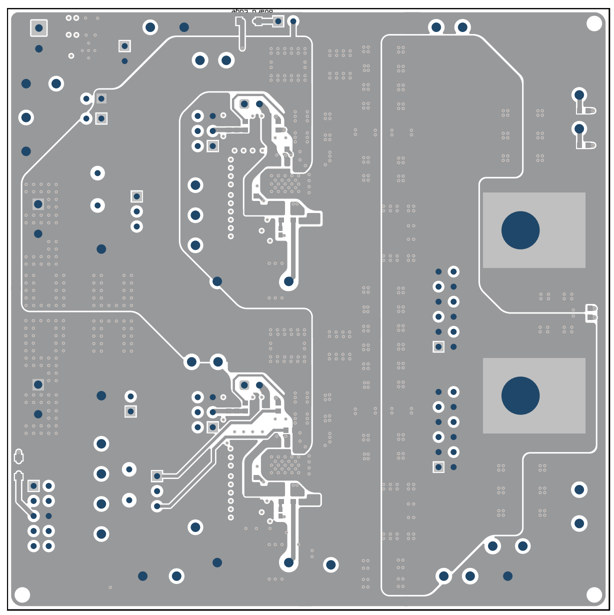


Figure 8-12. TPS546B24AEVM-2PH Internal Bottom Layer (Top View)

9 Bill of Materials

Table 9-1 lists the BOM for the TPS546B24AEVM-2PH.

Table 9-1. TPS546B24AEVM-2PH Bill of Materials

Designator[(1)]	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BSR104	Any
C1_P1, C1_P2, C11_P1, C11_P2	4	1 µF	CAP, CERM, 1 uF, 25 V, ±10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C2_P1, C2_P2, C33, C34	4	100 µF	CAP, AL, 100 µF, 35 V, ±20%, 0.15 Ω, SMD	SMT Radial G	EEE-FC1V101P	Panasonic
C3_P1, C3_P2, C4_P1, C4_P2, C5_P1, C5_P2, C6_P1, C6_P2	8	22 µF	CAP, CERM, 22 µF, 25 V, ±10%, X6S, 1210	1210	GRM32EC81E226KE15L	MuRata
C7_P1, C7_P2, C8_P1, C8_P2, C9_P1, C9_P2	6	6800 pF	CAP, CERM, 6800 pF, 50 V, ±10%, X7R, 0402	0402	GRM155R71H682KA88D	MuRata
C12_P1, C12_P2	2	1000 pF	CAP, CERM, 1000 pF, 100 V, ±5%, X7R, 0603	0603	06031C102JAT2A	AVX
C13_P1, C13_P2, C20_P1, C20_P2	4	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C15_P1, C15_P2	2	4.7 µF	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet
C17_P1	1	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C19_P1, C19_P2	2	2.2 µF	CAP, CERM, 2.2 uF, 16 V, ±10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C21_P1, C21_P2	2	33 pF	CAP, CERM, 33 pF, 50 V, ±5%, C0G/NP0, 0603	0603	C0603C330J5GACTU	Kemet
C22	1	1 µF	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0805	0805	C0805C105K5RACTU	Kemet
C23	1	10 µF	CAP, CERM, 10 µF, 10 V, ±20%, X7R, 0805	0805	C2012X7R1A106M125AC	TDK
C24	1	0.01 µF	CAP, CERM, 0.01 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R72A103KA37J	MuRata
C25, C29, C30, C31, C32, C35, C36, C49, C50, C51, C52, C53, C54, C55, C62, C68	16	47 µF	CAP, CERM, 47 µF, 10 V, ±10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
C47, C48, C63, C64	4	220 µF	CAP, TA, 220 µF, 6.3 V, ±20%, 0.009 Ω, SMD	7343-31	T520D227M006ATE009	Kemet
D1, D2	2	30 V	Diode, Schottky, 30 V, 2 A, AEC-Q101, SOD-123FL	SOD-123FL	MBR230LSFT1G	ON Semiconductor
D1_P1, D1_P2	2	45 V	Diode, Schottky, 45 V, 0.75 A, SOD-523	SOD-523	BAS 52-02V H6327	Infineon Technologies
H1, H2	2		Machine Screw Pan Philips 10-32		PMSSS 102 0050 PH	B&F Fastener Supply
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 × 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H7, H8	2		Machine Screw Nut, Hex, 3/8', Stn, Steel, 10-32		HNSS 102	B&F Fastener Supply
H9, H10	2		Washer, Split Lock, #10		1477	Keystone
J2	1		Header (shrouded), 100mil, 5 × 2, Gold, TH	5 × 2 Shrouded header	5103308-1	TE Connectivity
J4	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	MICRO USB CONN, R/A	1981568-1	TE Connectivity
JP1_P1, JP1_P2	2		Header, 2.54 mm, 2 × 1, Gold, TH	Header, 2.54 mm, 2 × 1, TH	61300211121	Wurth Elektronik
JP2_P1, JP2_P2	2		Header, 100 mil, 3 × 2, Gold, TH	Sullins 100 mil, 2 × 3, 230 mil above insulator	PBC03DAAN	Sullins Connector Solutions
JP3, JP4, JP5	3		Header, 100mil, 2 × 1, Tin, TH	Header, 2 × 1, 100 mil, TH	5-146278-2	TE Connectivity
JP7_P1, JP7_P2	2		Header, 100 mil, 3 × 1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions

Table 9-1. TPS546B24AEVM-2PH Bill of Materials (continued)

Designator[1]	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
L1, L2	2	300nH	Inductor, Shielded, Ferrite, 300 nH, 52 A, 0.00015 Ω, SMD	SMD 13.46 × 8.0 × 12.95 mm	SLC1480-301MLB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	PCB Label 0.650 × 0.200 inch	THT-14-423-10	Brady
LED1	1	Green	LED, Green, SMD	LED_0603	150060GS75000	Wurth Elektronik
R2_P1, R2_P2, R3_P1, R3_P2	4	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R4_P1, R4_P2, R15_P1, R15_P2, R16_P1, R16_P2, R17_P1, R17_P2, R18_P2, R22_P1, R22_P2, R23_P1, R23_P2, R25_P1, R25_P2, R27_P1, R27_P2, R32, R33	19	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R5_P1, R5_P2, R34, R35, R36, R38	6	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R6_P1, R6_P2	2	1.0	RES, 1.0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW12061R00JNEA	Vishay-Dale
R8_P2, R26_P1, R26_P2	3	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R9_P1, R9_P2	2	30.1 k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo
R14_P1, R14_P2	2	7.50 k	RES, 7.50 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF7501V	Panasonic
R19_P1	1	14.7 k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1472V	Panasonic
R21_P1	1	5.62 k	RES, 5.62 k, 1%, 0.1 W, 0603	0603	RC0603FR-075K62L	Yageo
R28	1	1.00 k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R29	1	47.5 k	RES, 47.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347K5FKEA	Vishay-Dale
R30	1	15.0 k	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060315K0FKEA	Vishay-Dale
R31	1	560 k	RES, 560 k, 1%, 0.1 W, 0603	0603	RC0603FR-07560KL	Yageo
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6	6	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
SMB1_P1, SMB1_P2, SMB2	3		Connector, Receptacle, 50 Ω, TH	SMB Connector	SMBR004D00	JAE Electronics
T1, T2	2		Therminal Block, 5 mm, 2-pole, Tin, TH	TH, 2-Leads, Body 10 × 10 mm, Pitch 5 mm	282856-2	TE Connectivity
T3, T5	2		Terminal 90-A Lug	CB70-14-CY	CB70-14-CY	Panduit
T4	1		Terminal Block, 3.5-mm Pitch, 2 × 1, TH	7.0 × 8.2 × 6.5 mm	ED555/2DS	On-Shore Technology
TP1_P1, TP1_P2, TP6, TP12, TP13, TP19, TP22, TP26	8		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2_P1, TP2_P2, TP5_P1, TP5_P2, TP7, TP8, TP9, TP10, TP14, TP17, TP18, TP21, TP27, TP28, TP29, TP31	16		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
TP3_P1, TP3_P2, TP4_P1, TP4_P2, TP11, TP15, TP16, TP20, TP23, TP24, TP25, TP30, TP32	13		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
U1_P1, U1_P2	2		2.95-V to 16-V, 20-A PMBUS Stackable Synchronous Buck Converter, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS546B24ARVFR	Texas Instruments
U2	1		800-mA Ultra-Low-Noise, High-PSRR LDO, DNT0012B (WSON-12)	DNT0012B	LP38798SD-ADJ/NOPB	Texas Instruments
C10_P1, C10_P2, C14_P1, C14_P2	0	1 µF	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet

Table 9-1. TPS546B24AEVM-2PH Bill of Materials (continued)

Designator[(1)]	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C16_P1, C16_P2	0	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C17_P2	0	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C18_P1, C18_P2	0	2.2 µF	CAP, CERM, 2.2 µF, 16 V, ±10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C26, C27, C28, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C56, C57, C58, C59, C60, C61, C65, C66, C67, C69, C70, C71, C72	0	47 µF	CAP, CERM, 47 µF, 10 V, ±10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1, J3	0		Receptacle, 2.54 mm, 6 × 2, Gold, TH	Receptacle, 2.54 mm, 6 × 2, TH	SSQ-106-03-G-D	Samtec
JP6, JP8	0		Header, 100 mil, 2 × 1, Tin, TH	Header, 2 × 1, 100 mil, TH	5-146278-2	TE Connectivity
R1_P1, R1_P2, R18_P1, R24_P1, R24_P2, R37, R39	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R8_P1	0	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R10_P1, R10_P2, R11_P1, R11_P2, R12_P1, R12_P2, R20_P1, R20_P2	0	10.5 k	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K5FKEA	Vishay-Dale
R13_P1, R13_P2	0	53.6 k	RES, 53.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060353K6FKEA	Vishay-Dale
R19_P2	0	14.7 k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1472V	Panasonic
R21_P2	0	12.1 k	RES, 12.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
TP33	0		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP34_P1, TP34_P2, TP35_P1, TP35_P2	0		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone

(1) Unless otherwise noted, all parts can be substituted with equivalents.

10 Using the Fusion GUI

10.1 Opening the Fusion GUI

The Fusion GUI should include *IC_DEVICE_ID* in the scanning mode to find TPS546B24A. The EVM needs power to be recognized by the Fusion GUI. See Section 5 for the recommended procedure.

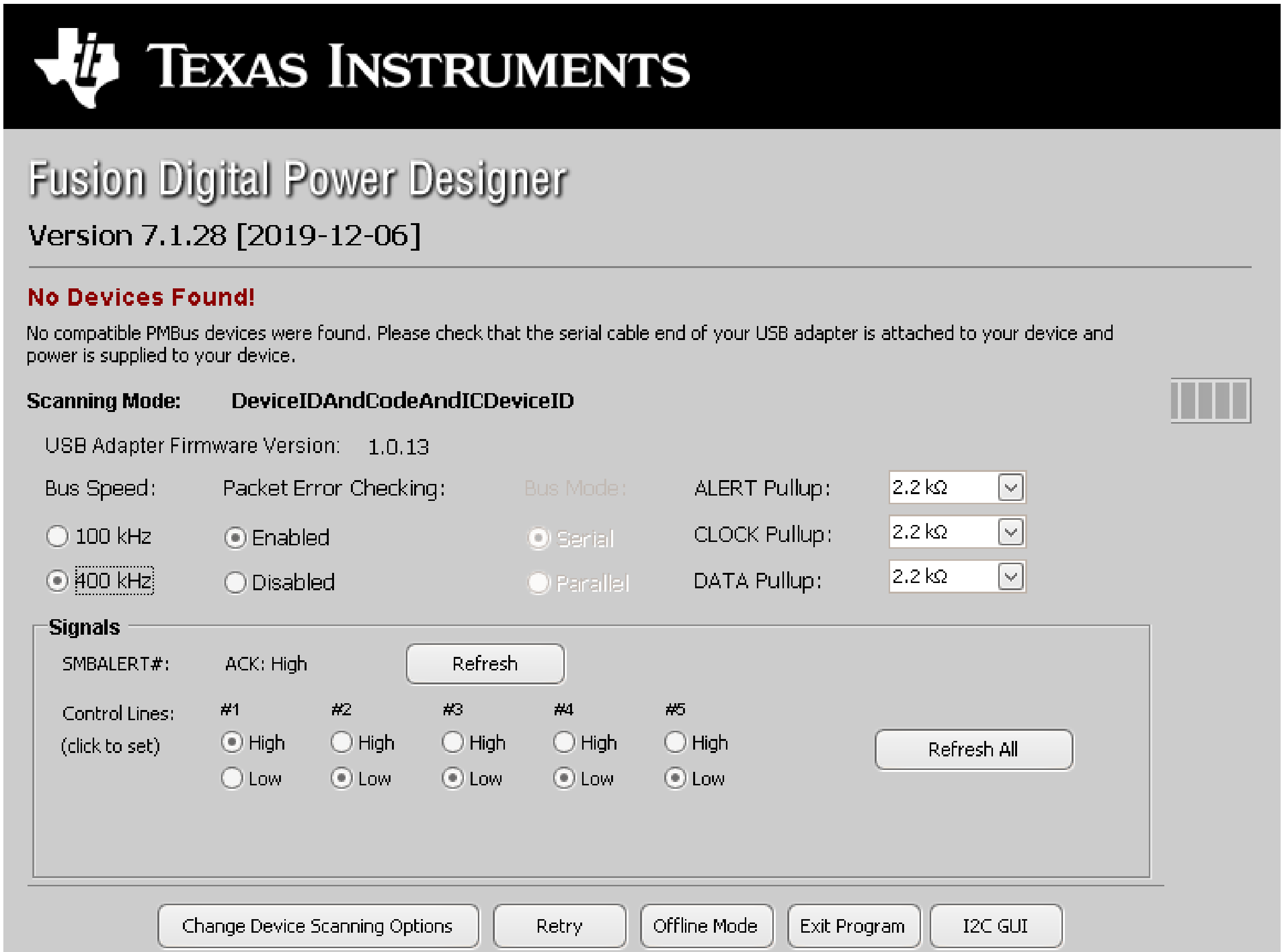


Figure 10-1. Select Device Scanning Mode

10.2 General Settings

Figure 10-2 shows the *General Settings* that can be used to configure the following:

- V_{OUT} settings, power good limits, and margin voltages
- OC Fault, OC Warn, and Fault response
- OT Fault, OT Warn (Die Temperature), and Fault response
- VIN on and off UVLO
- On/Off Config
- Soft Start (Output rise time), other Turn On Timing, and Turn Off Timing
- Switching frequency
- Compensation

After clicking *Write to Hardware* to make changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking *Store Config to NVM*. This action prompts a pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in non-volatile memory.

Both the loop controller device and the loop follower device are tied to same bus interface. In a two-phase stacking system, the controller device will receive and respond to all PMBus communication and follower devices do not need to be connected to the PMBus. If the controller receives commands that require updates to the PMBus registers of the follower, the controller will relay these commands to the followers. All commands on this tab are for PHASE = 0xFF.

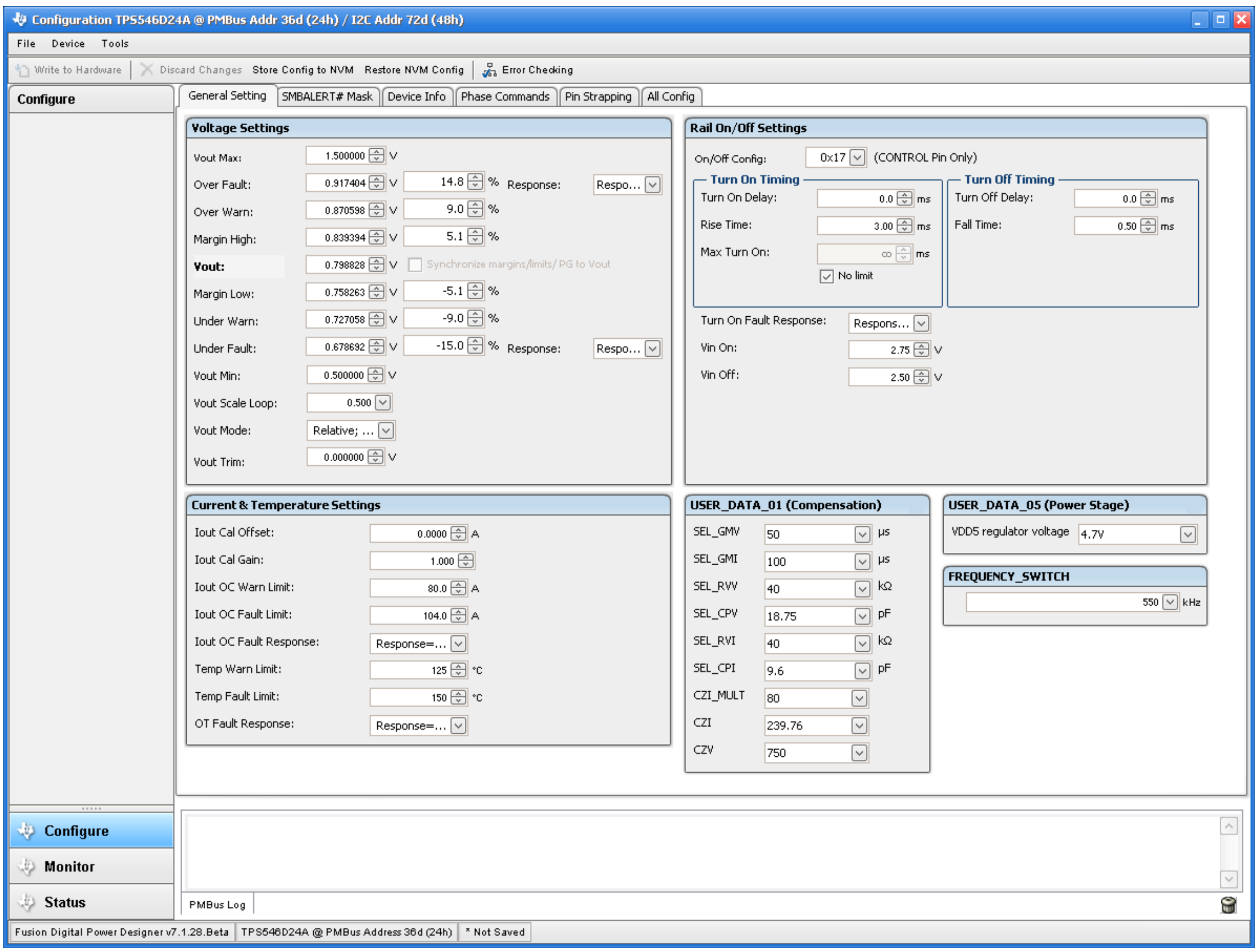


Figure 10-2. General Settings

10.3 Changing ON_OFF_CONFIG

Changing the *On/Off Config* prompts a pop-up window with details of the options shown in Figure 10-3. This pop-up gives multiple options on what turns on and off power conversion. By default, the TPS546B24A is configured to *CONTROL Pin Only*. This is the EN/UVLO pin.

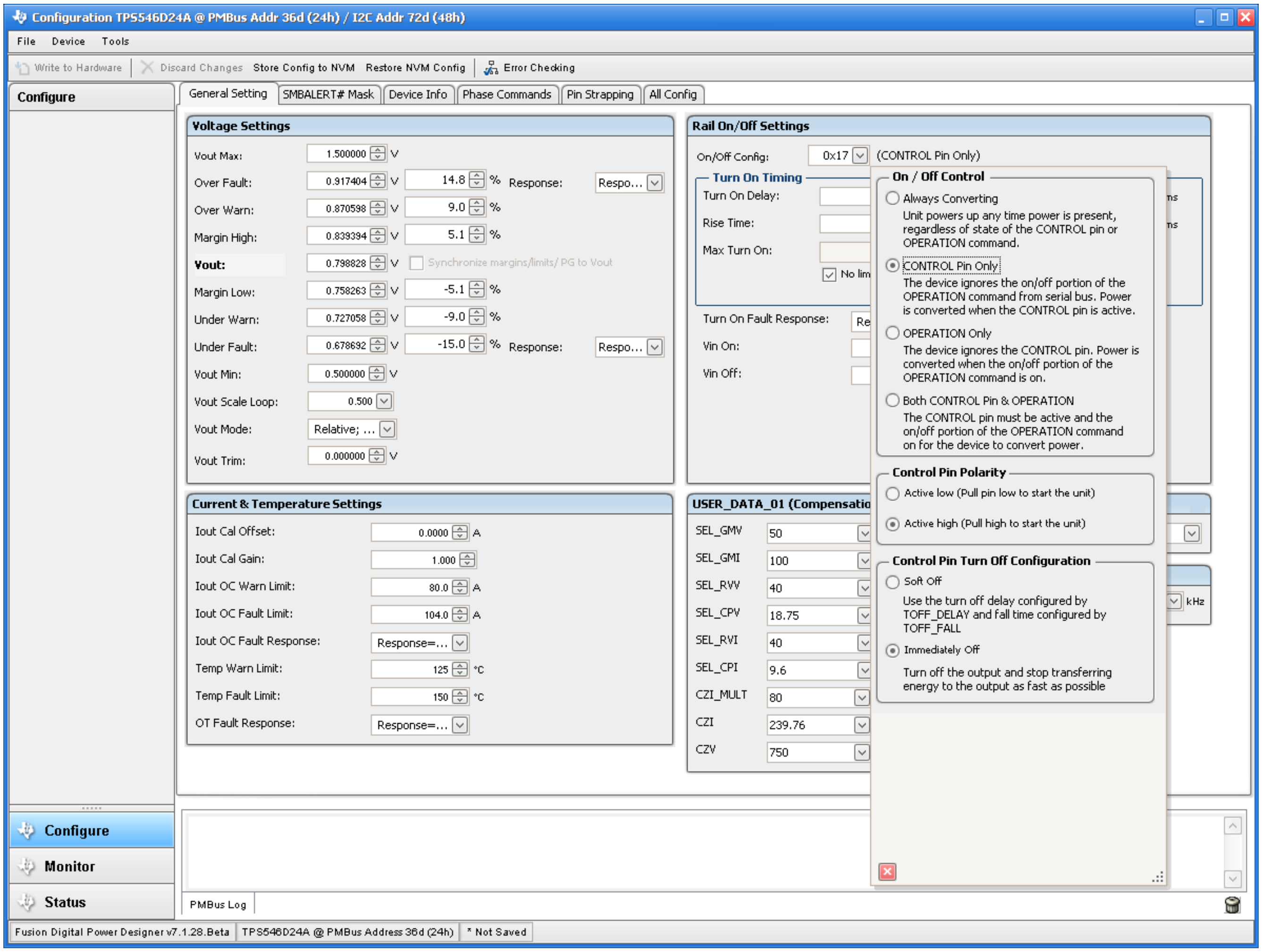


Figure 10-3. Configure – ON_OFF_CONFIG

10.4 Pop-up for Some Commands While Conversion is Enabled

Some commands will cause a pop-up like the one shown in Figure 10-4 when trying to change them while conversion is enabled. The settings in the GUI that will cause this pop-up include the following:

- *FREQUENCY_SWITCH*
- *USER_DATA_01 (Compensation)*
- *Vout Mode*
- *Vout Scale Loop*

To change these settings to a new value, click on *Stop Power Conversion* then *Close and continue*. The GUI will automatically disable conversion, write the new value, and enable conversion again.

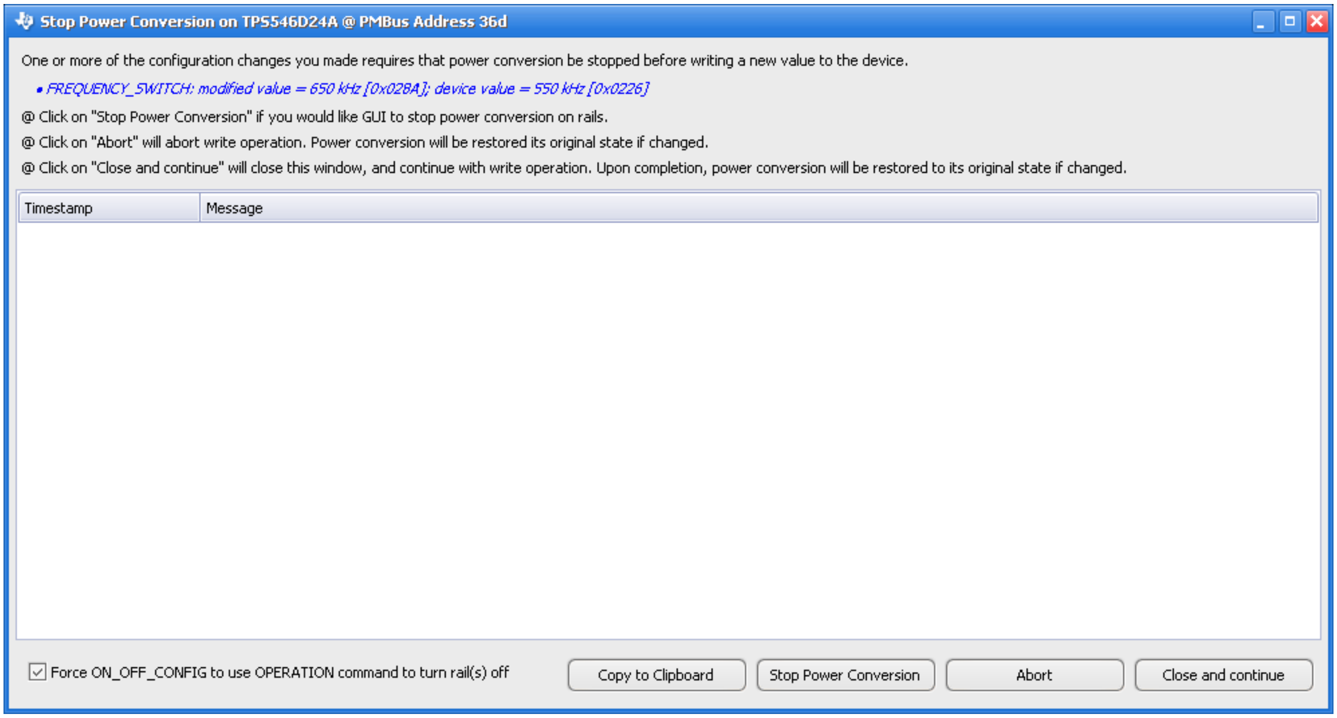


Figure 10-4. Pop-up When Trying to Change FREQUENCY_SWITCH With Conversion Enabled

10.5 SMBALERT# Mask

The sources of SMBALERT that can be masked are found and configured on the *SMBALERT # Mask* tab (Figure 10-5).

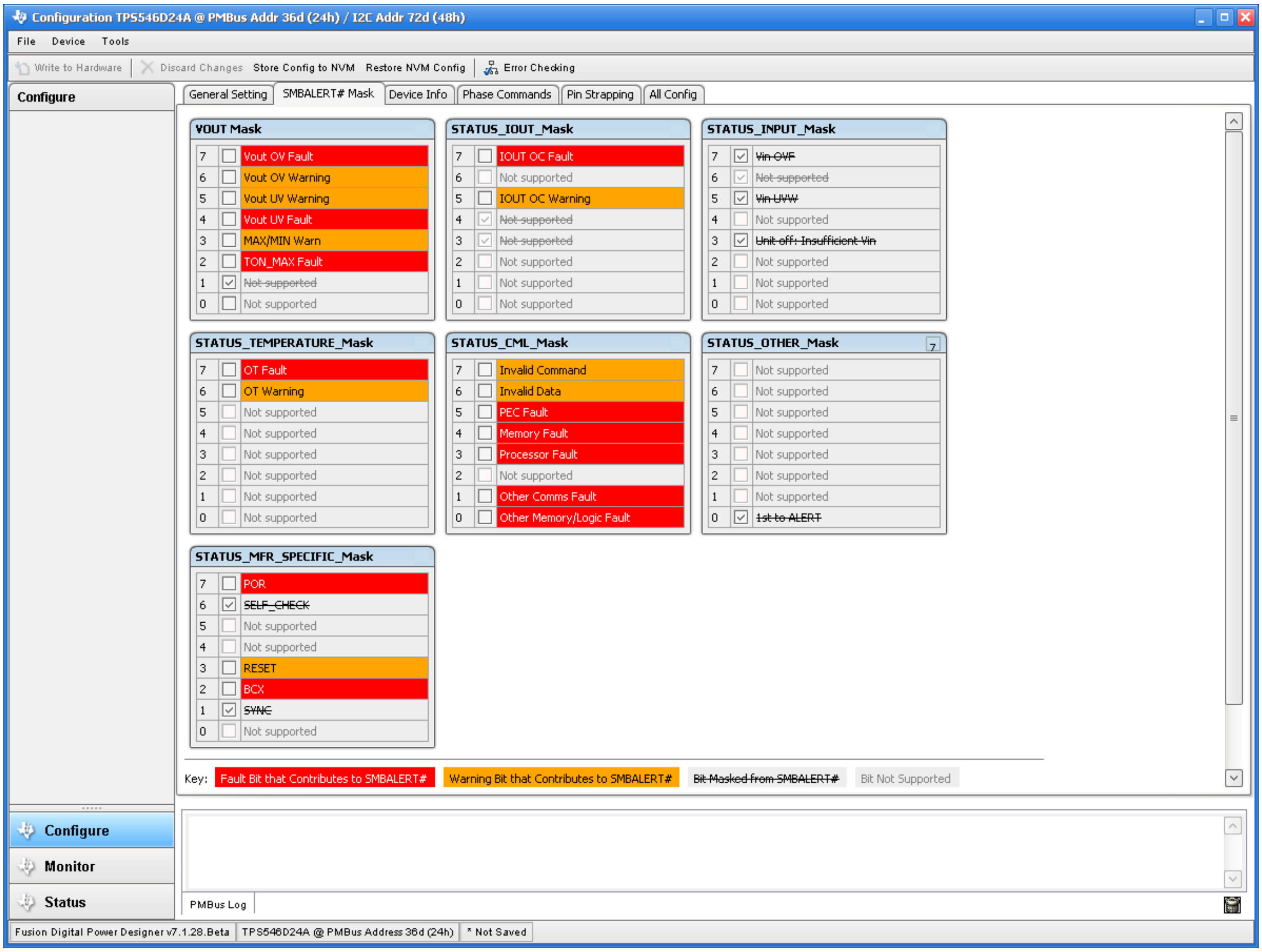


Figure 10-5. Configure – SMBALERT # Mask

10.6 Device Info

The device information, Write Protection options, and the configuration of *Vout Scale Loop*, *Vout Transition Rate*, and *Iout Cal Offset* are found on the *Device Info* tab (Figure 10-6).

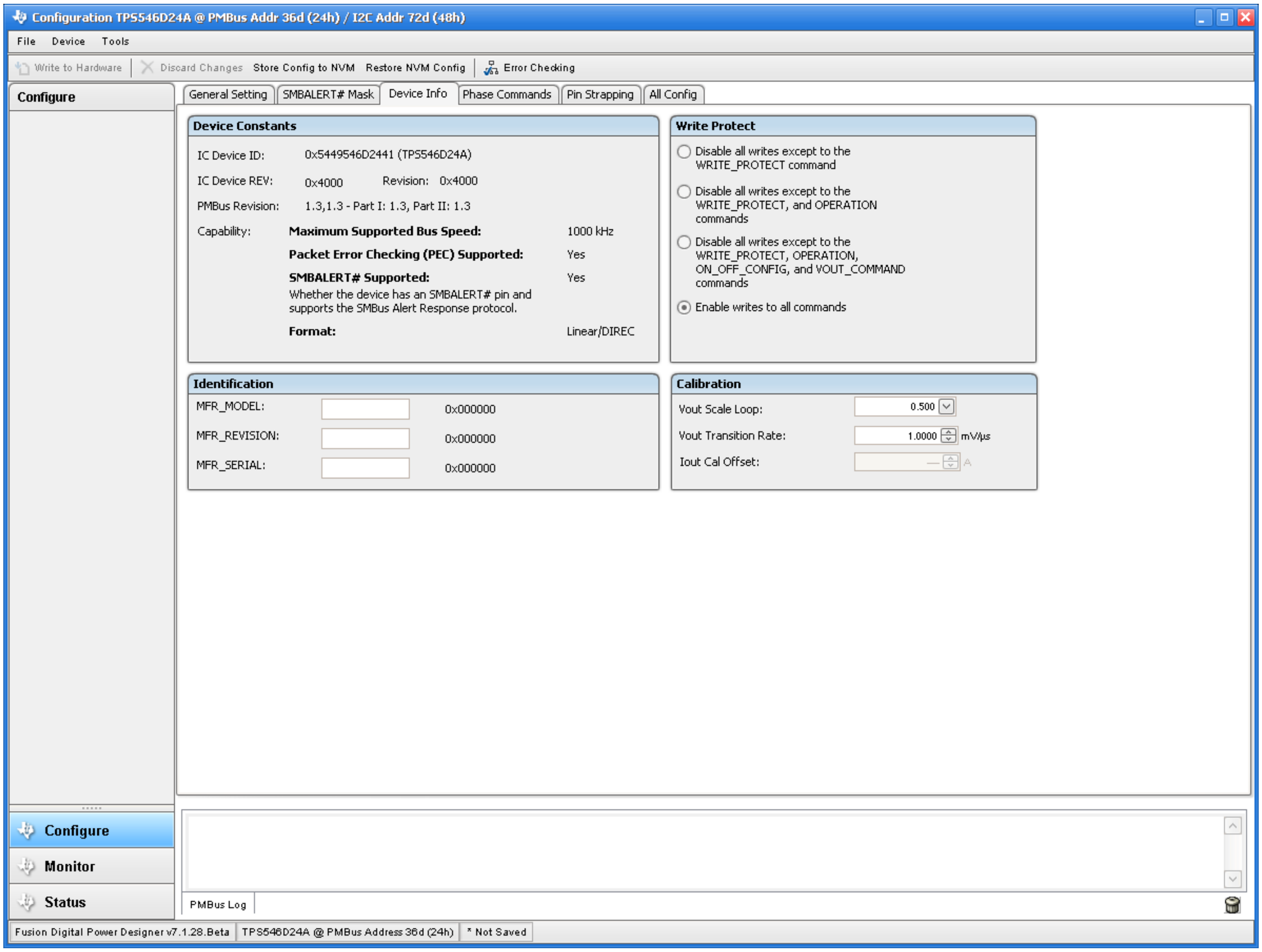


Figure 10-6. Configure – Device Info

10.7 Phase Commands

Use the *Phase Command* tab (Figure 10-7) to calibrate the *IOUT/Temp* of each phase.

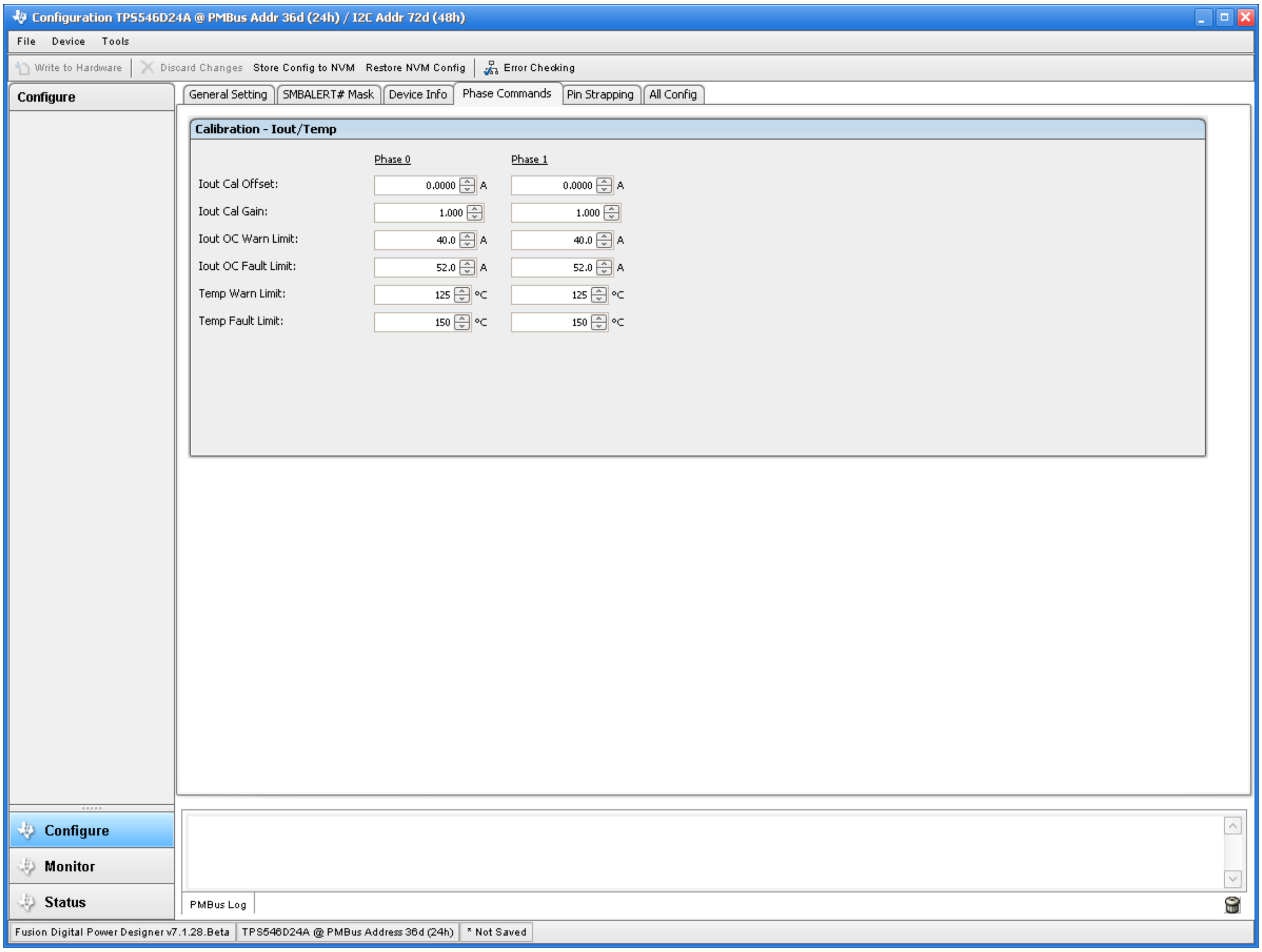


Figure 10-7. Phase Commands

10.8 All Config

Use the *All Config* tab (Figure 10-8) to configure all of the configurable parameters, which also shows other details like Hex encoding.

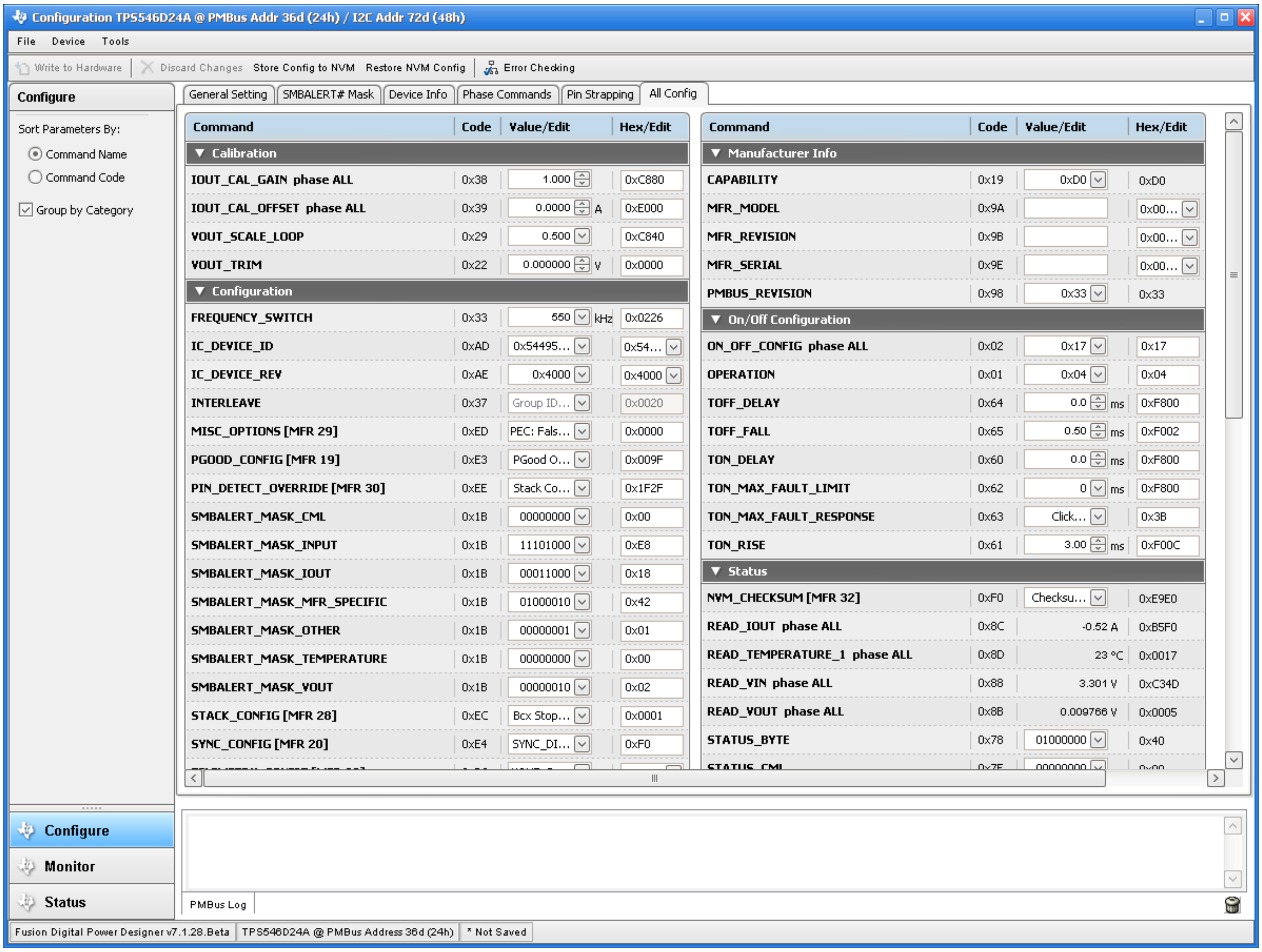


Figure 10-8. Configure – All Config

10.9 Pin Strapping

Use the *Pin Strapping* tab (Figure 10-8) to aid in selection of external pin strapping resistors used to program some of the PMBus commands at power up. The *EEPROM Value* column shows the values currently configured to the related PMBus commands.

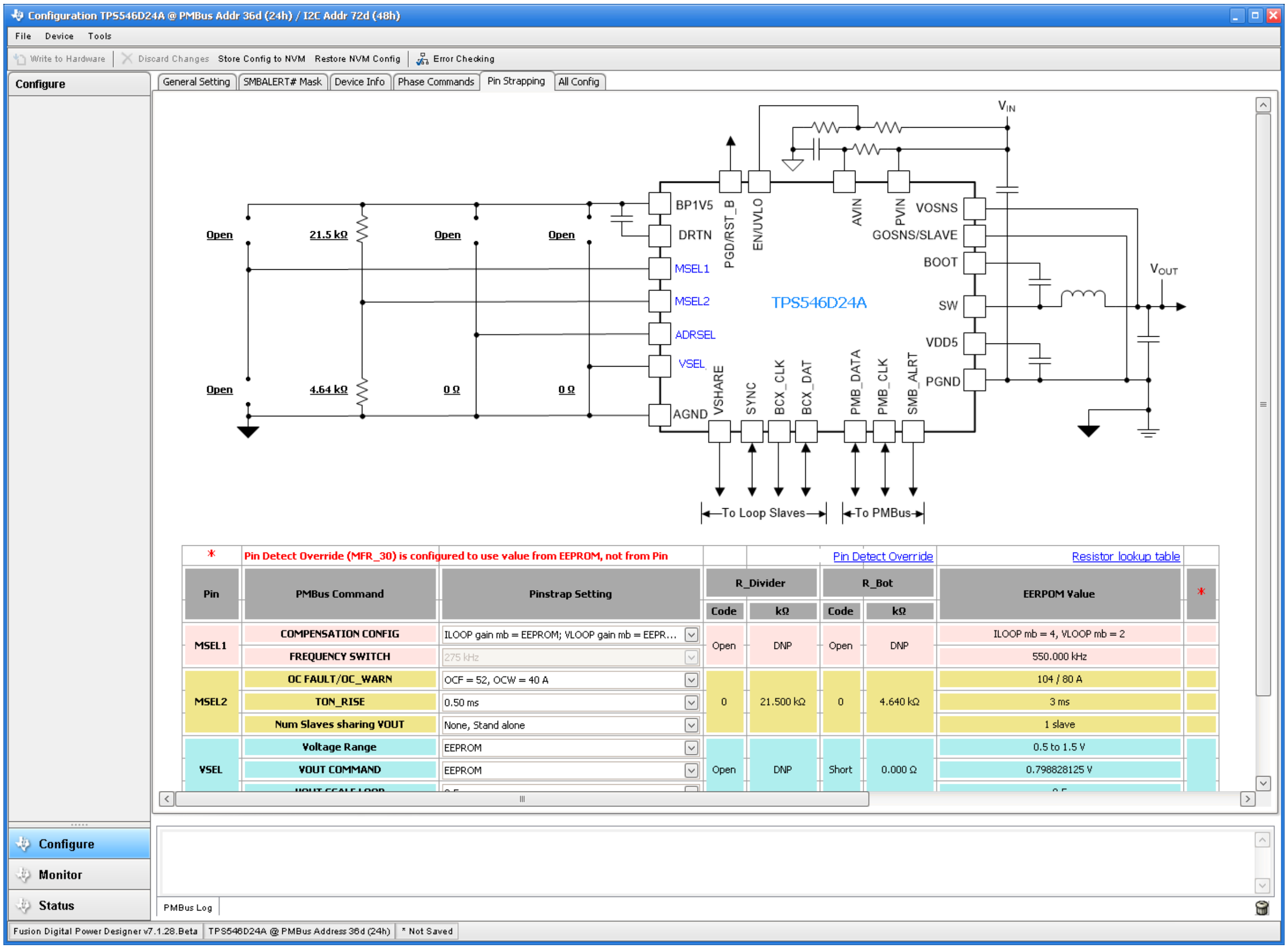


Figure 10-9. Configure – Pin Strapping

10.10 Monitor

When the *Monitor* screen (Figure 10-10) is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of *Vout*, *Iout*, *Vin*, *Pout*, and *Temperature*
- *Start and Stop Polling* which turns ON or OFF the realtime display of data
- Quick access to *On/Off Config*
- Control pin activation and *OPERATION* command
- Margin control
- Clear Fault: Selecting ***Clear Faults*** clears any prior fault flags.

With two devices stacked together, the *Iout* reading is the total load supported by both devices. There is also an *Iout*, which shows the current in each phase.

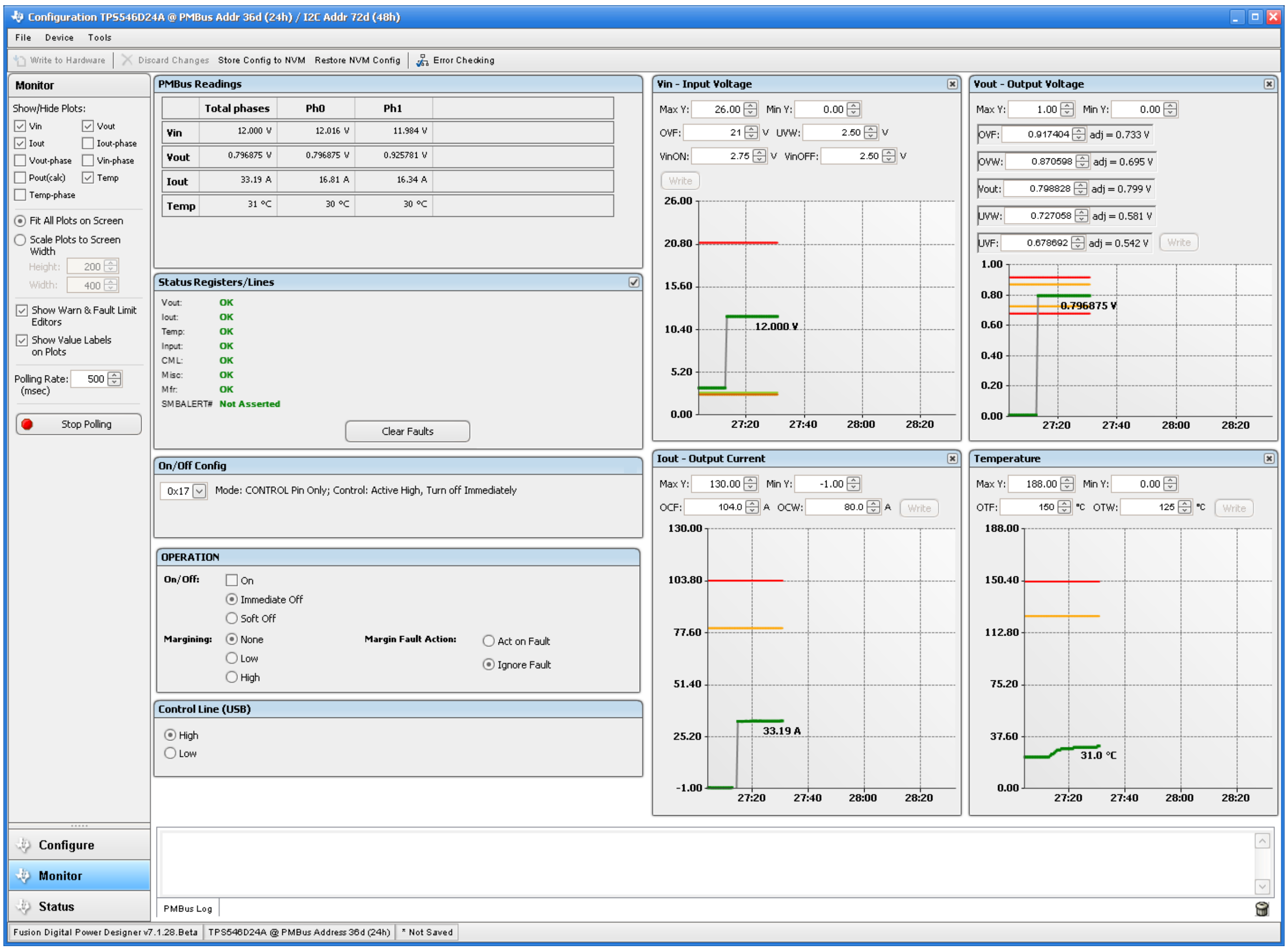


Figure 10-10. Monitor Screen

10.11 Status

Selecting the *Status* screen from lower left corner (Figure 10-11) shows the status of the device.

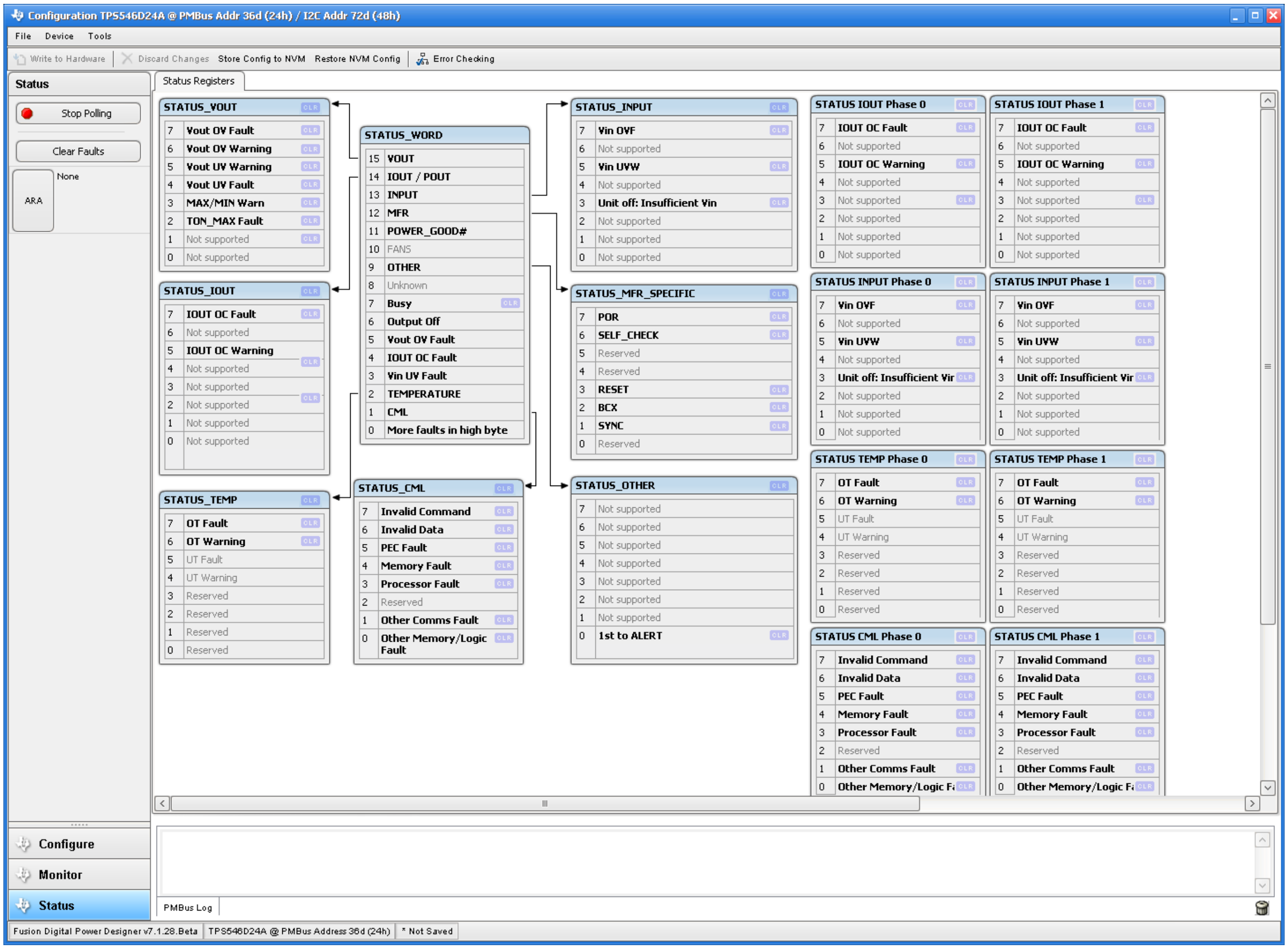


Figure 10-11. Status Screen

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	4
• Updated the user's guide title	4
• Changed all instances of legacy terminology to loop controller and loop follower where PMBus is mentioned.	4