

# **TPS566235 Buck Converter Evaluation Module User's Guide**

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## **ABSTRACT**

This user's guide contains the information for TPS566235EVM-036 evaluation module as well as TPS566235 DC/DC converter. Also included are the specification, schematic, printed-circuit board (PCB) layout, hardware setup, and list of materials.

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## **Table of Contents**

<b>1 Introduction.....</b>	<b>2</b>
<b>2 Specification Summary.....</b>	<b>2</b>
<b>3 Modifications.....</b>	<b>2</b>
3.1 Output Voltage Setpoint.....	2
3.2 Mode Selection.....	2
<b>4 Schematic and Board layout.....</b>	<b>3</b>
4.1 Schematic.....	3
4.2 Board Layout.....	3
<b>5 EVM Test Setup.....</b>	<b>6</b>
5.1 Connectors and Jumpers Description and Placement.....	6
5.2 Start-up Procedure.....	8
<b>6 Test Waveforms.....</b>	<b>9</b>
6.1 Power Up.....	9
6.2 Power Down.....	9
6.3 Output Voltage Ripple.....	10
6.4 Load Transient Response.....	11
6.5 Thermal.....	12
<b>7 List of Materials and Reference.....</b>	<b>13</b>
7.1 List of Materials.....	13
7.2 Reference.....	13
<b>8 Revision History.....</b>	<b>13</b>

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## 1 Introduction

TPS566235 device is a high efficiency, cost effective, synchronous BUCK DC/DC converter with integrated FETs. It employs the proprietary D-CAP3™ control mode that is optimized for low-ESR output capacitors and features fast transient response without external compensation. The operating input voltage range is 4.5 V to 18 V, the output voltage can be programmed between 0.6 V and 7 V, and the output current is up to 6 A. The operating frequency is internally set to nominal 600 kHz in CCM, and there are 3 different operation modes can be configured by MODE pin at light load: Eco-Mode, Out-of-Audio, and FCCM. TPS566235 provides rich functions as well as excellent power supply performance, internal fixed 1mSec soft start, power good indicator, and full protections including UVLO, OCP, OVP, UVP, OTP. The devices are available in 3.0-mm × 2.0-mm HotRod™ package and the die operating temperature is specified from -40°C to 125°C.

TPS566235EVM-036 evaluation module (EVM) is designed for accessing to the features of TPS566235.

## 2 Specification Summary

A summary of TPS566235EVM-036 specification is provided in [Table 2-1](#). TPS566235EVM-036 is designed for  $V_{IN} = 4.5\text{ V} - 18\text{ V}$ ,  $V_{OUT} = 1.05\text{ V}$ , the junction temperature  $T_J$  is 25°C for all measurement, unless otherwise noted.

**Table 2-1. TPS566235EVM-036 Specifications Summary**

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	Unit
Input voltage		4.5	12	18	V
Output voltage set point			1.05		V
Output current range		0		6	A
FB voltage	$T_J = 25^\circ\text{C}$	594	600	606	mV
Operating frequency	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 6\text{ A}$		600		kHz
Soft start time	Internal fixed soft start time		1		ms
Over current limit	Valley current set point		7.6		A

## 3 Modifications

Some modifications can be made to this module for different output voltages and different operation modes.

### 3.1 Output Voltage Setpoint

$V_{OUT}$  is set by the resistor divider network of R3 ( $R_{TOP}$ ) and R8 ( $R_{BOT}$ ). Set R8 value firstly, then changing R3 value can change  $V_{OUT}$  above the reference voltage  $V_{REF} = 0.6\text{ V}$ . The R3 value for a specific output voltage can be calculated using [Equation 1](#).

$$R_{(TOP)} = \frac{R_{(BOT)} \cdot (V_{OUT} - V_{REF})}{V_{REF}} \quad (1)$$

### 3.2 Mode Selection

TPS566235 has a MODE pin to select 3 different operation mode at light load. The device reads the voltage on MODE pin during start-up and latches onto one of the MODE options listed below in [Table 3-1](#).

**Table 3-1. MODE Pin Resistor Setting**

$V_{MODE}$	RECOMMENDED MODE RESISTOR $R_M$	OPERATION MODE
0 - 0.3 V	0 Ω	Eco-Mode
0.3 V - 1.2 V	100 kΩ - 150 kΩ	Out-of-Audio (OOA)
> 1.2 V	Connected to VCC pin (recommend) or > 400 kΩ	Forced CCM (FCCM)

Changing the position of jumper on J3 can modify MODE pin configuration before power on.

## 4 Schematic and Board layout

### 4.1 Schematic

Figure 4-1 illustrates TPS566235EVM-036 Evaluation Module schematic.

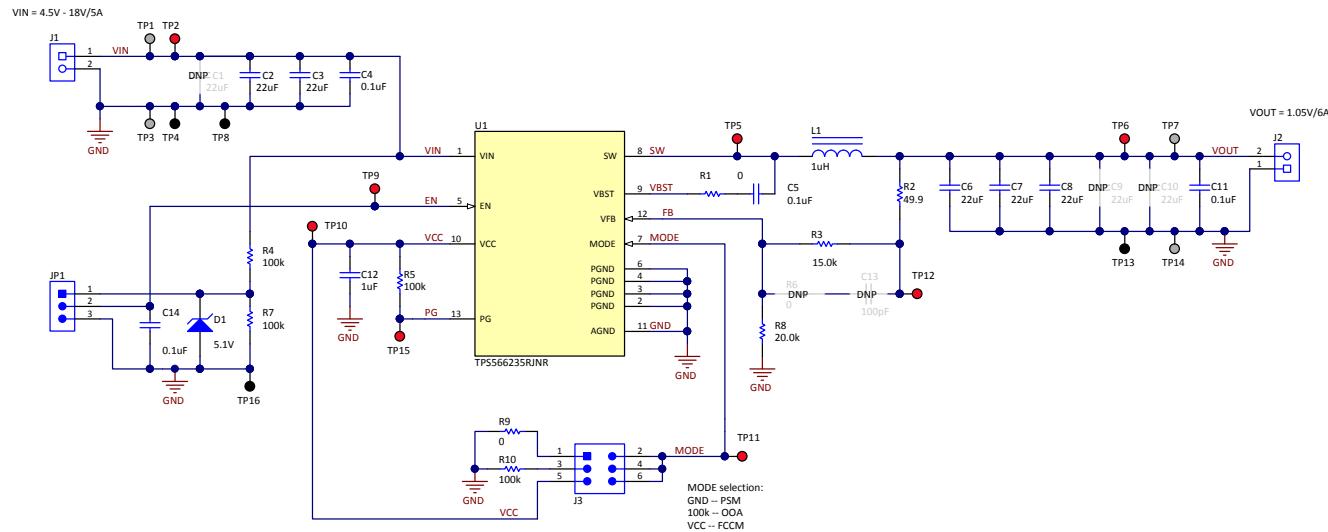


Figure 4-1. TPS566235EVM-036 Evaluation Module Schematic

### 4.2 Board Layout

Figure 4-2 through Figure 4-6 illustrates the TPS566235EVM-036 board layout. The top layer contains the main power traces for  $V_{IN}$ ,  $V_{OUT}$ , and SW, there is a large area filled with ground. The internal layer-1 and layer-2 are ground plane. The bottom layer is another ground plane. The ground traces of each layer are connected together with multiple VIAs. The top and bottom layers are 2-oz copper and internal layers are 1-oz copper.

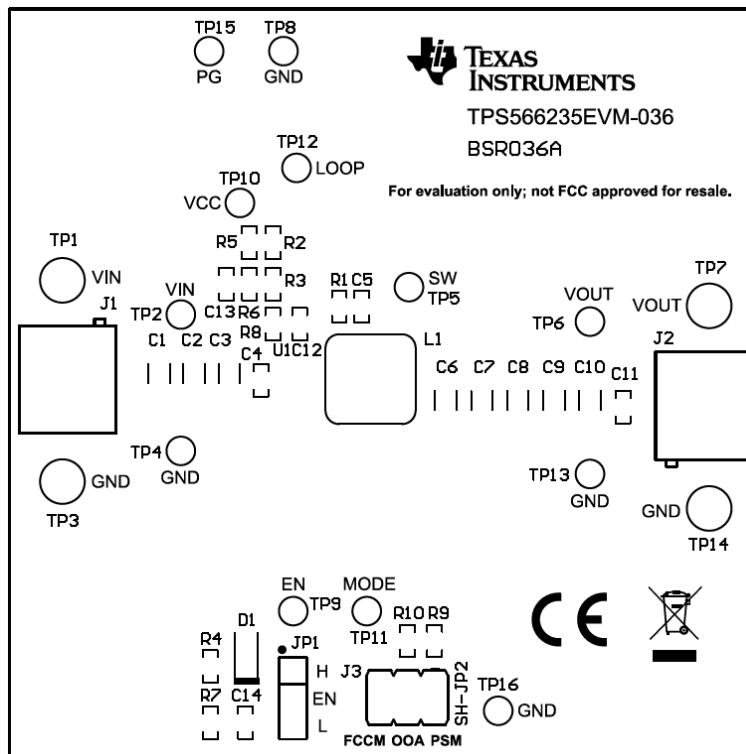
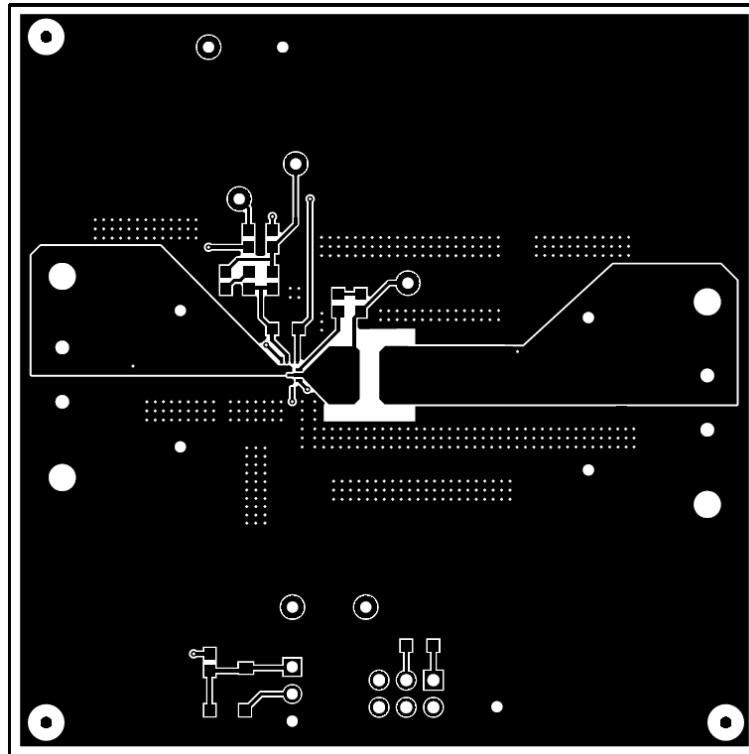
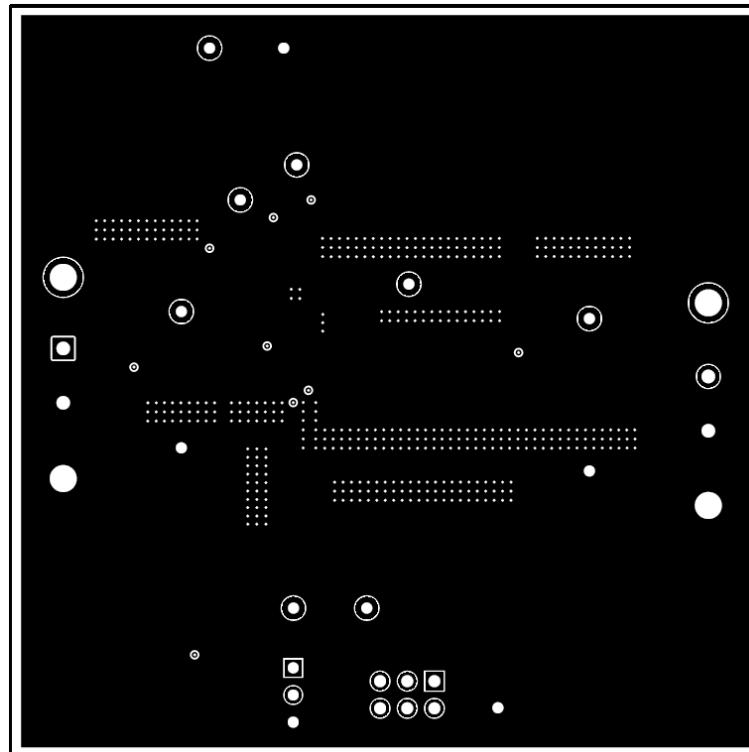


Figure 4-2. Component Placement (Top Layer)



**Figure 4-3. Board Layout (Top Layer)**



**Figure 4-4. Board Layout (Second Layer)**

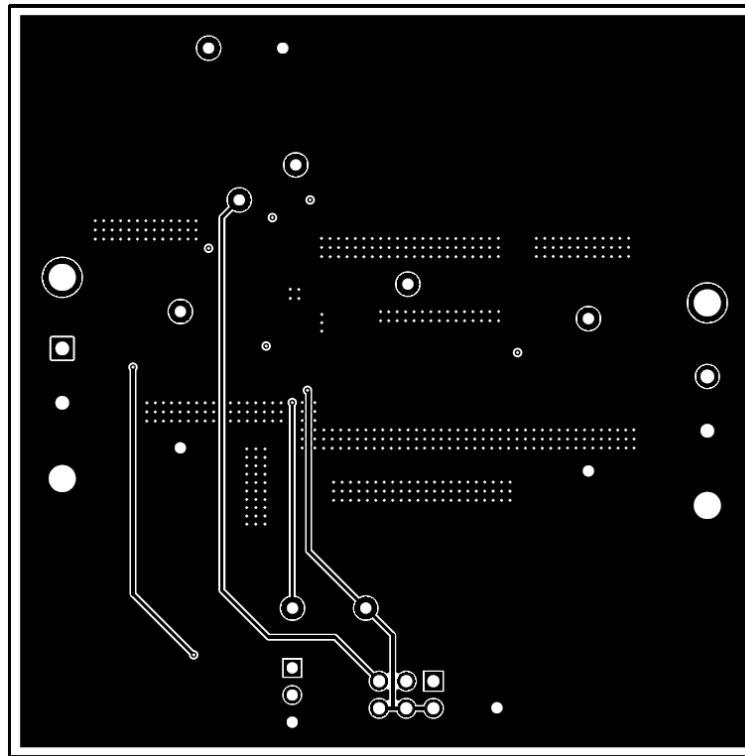


Figure 4-5. Board Layout (Third Layer)

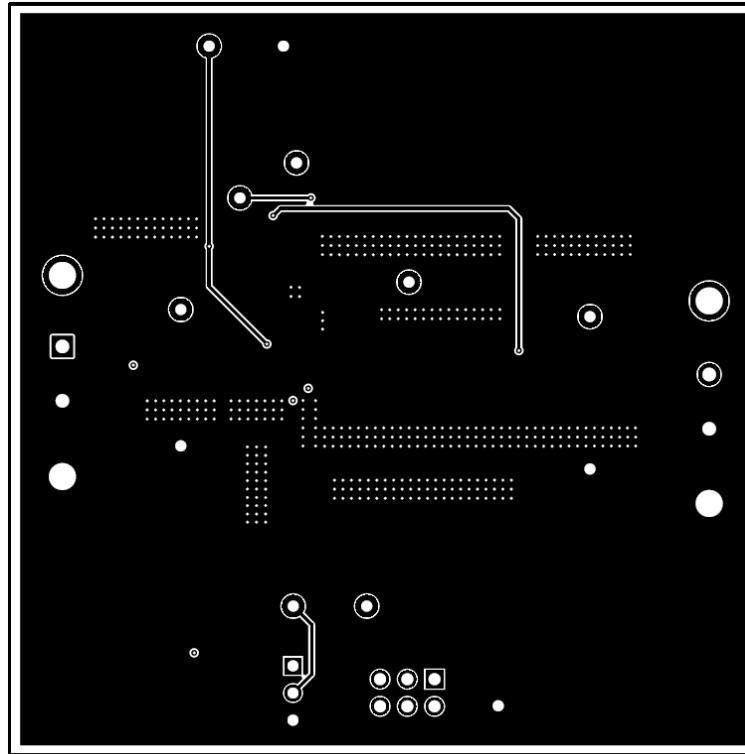


Figure 4-6. Board Layout (Bottom Layer)

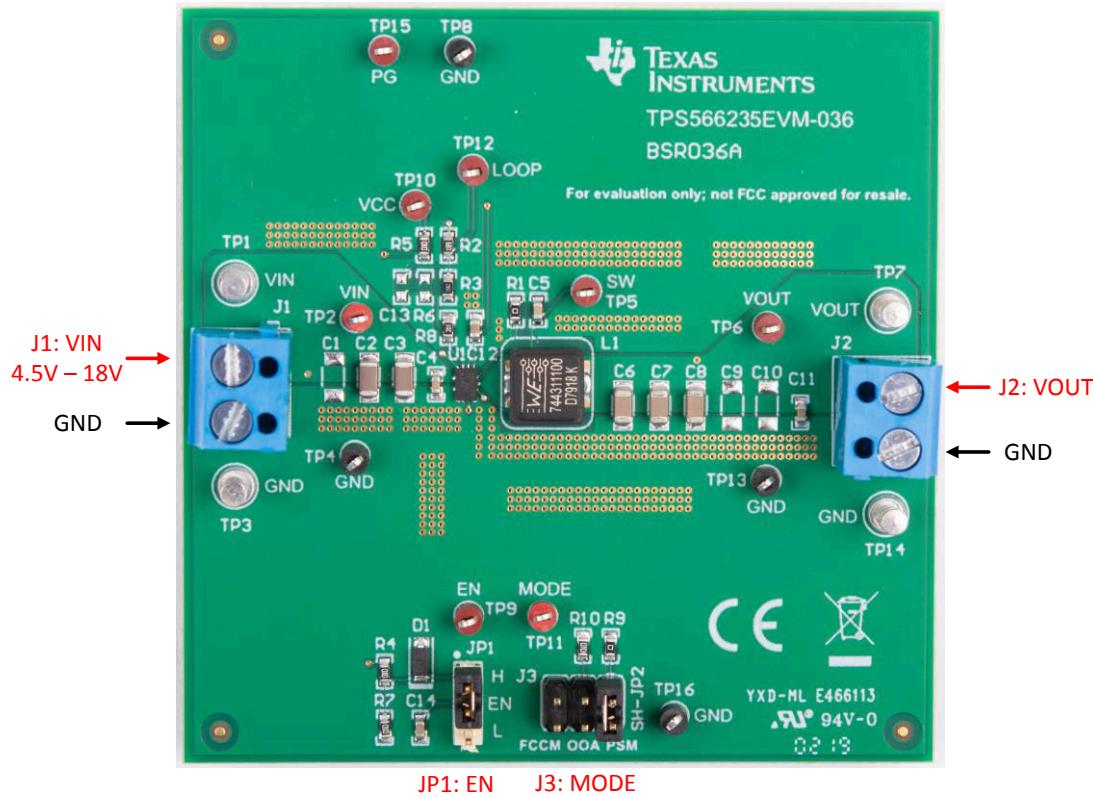
## 5 EVM Test Setup

This section describes how to properly connect, set up, and use TPS566235EVM-036 evaluation module.

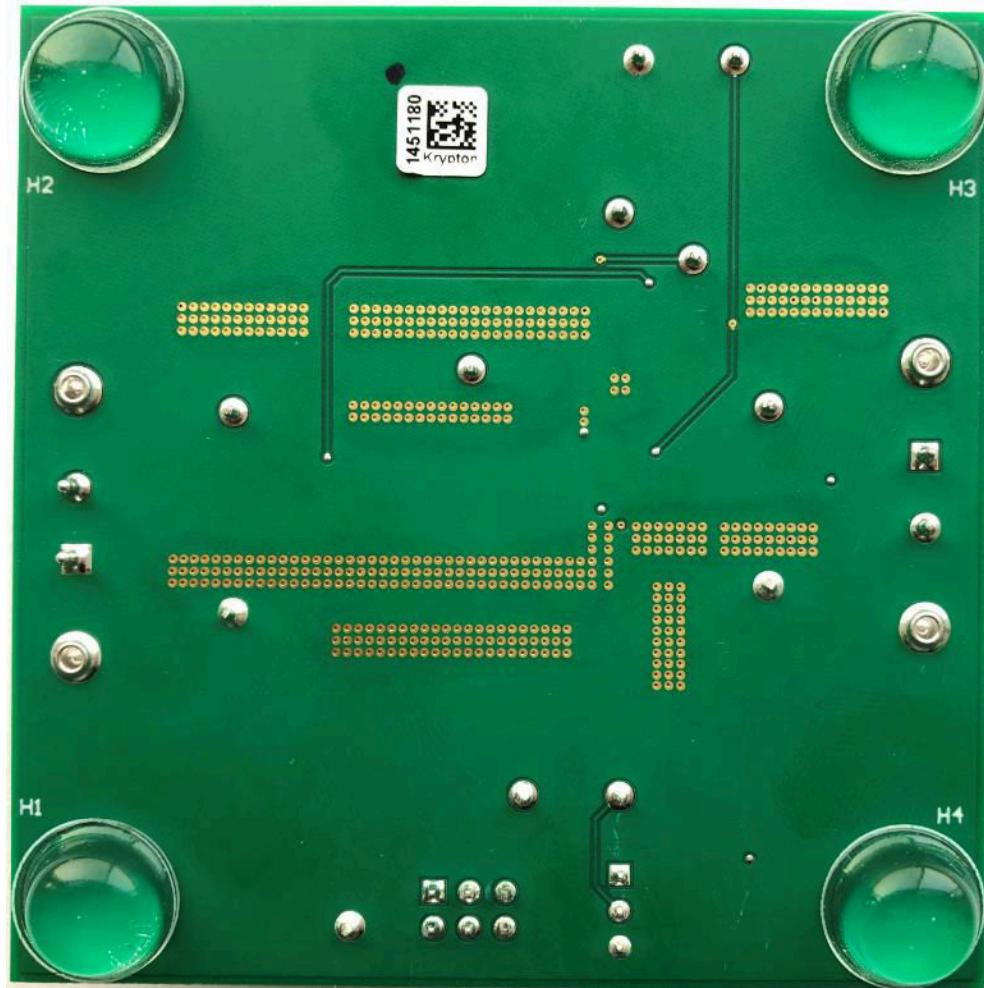
### 5.1 Connectors and Jumpers Description and Placement

TPS566235EVM-036 is provided with input/output connectors and test points as listed in [Table 5-1](#). And [Figure 5-1](#) and [Figure 5-2](#) shows connectors and jumpers placement on TPS566235EVM-036 board.

A power supply capable of supplying greater than 5 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 6 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP2 provides a place to monitor the  $V_{IN}$  input voltages with TP4 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP13 as the ground reference.



**Figure 5-1. Connectors and Jumpers Placement (Top View)**



**Figure 5-2. Connectors and Jumpers Placement (Bottom View)**

**Table 5-1. Connectors and Test Points Description**

DESIGNATOR	FUNCTION	DESCRIPTION
J1	$V_{IN}$ connector	Connect input power supply
J2	$V_{OUT}$ connector	Connect output load
J3	MODE selection	Refer to <a href="#">Table 3-1</a> for operation mode selection
JP1	Enable/disable control	Middle pin is IC's EN pin. Floating EN or shunting to GND will disable IC; Shunting EN to the other side will enable IC
TP1, TP2	$V_{IN}$ test point	Test input voltage
TP3, TP4, TP8, TP13, TP14, TP16	GND test point	Ground reference
TP5	SW test point	Test switching node
TP6, TP7	$V_{OUT}$ test point	Test output voltage
TP9	EN test point	Test enable signal
TP10	VCC test point	Test VCC
TP11	MODE test point	Test MODE
TP12	Loop test point	Test point between voltage divider network and output, used for loop response measurement
TP15	PG test point	Test power good signal

## 5.2 Start-up Procedure

Start-up with dedicated enable signal:

1. Select operation mode at J3.
2. Apply 4.5-V~18-V power supply to J1.
3. Apply 1.6-V~5.5-V enable signal to JP1 middle pin (EN pin).
4. Apply load to J2 output connector.
5. Check the  $V_{OUT}$ .

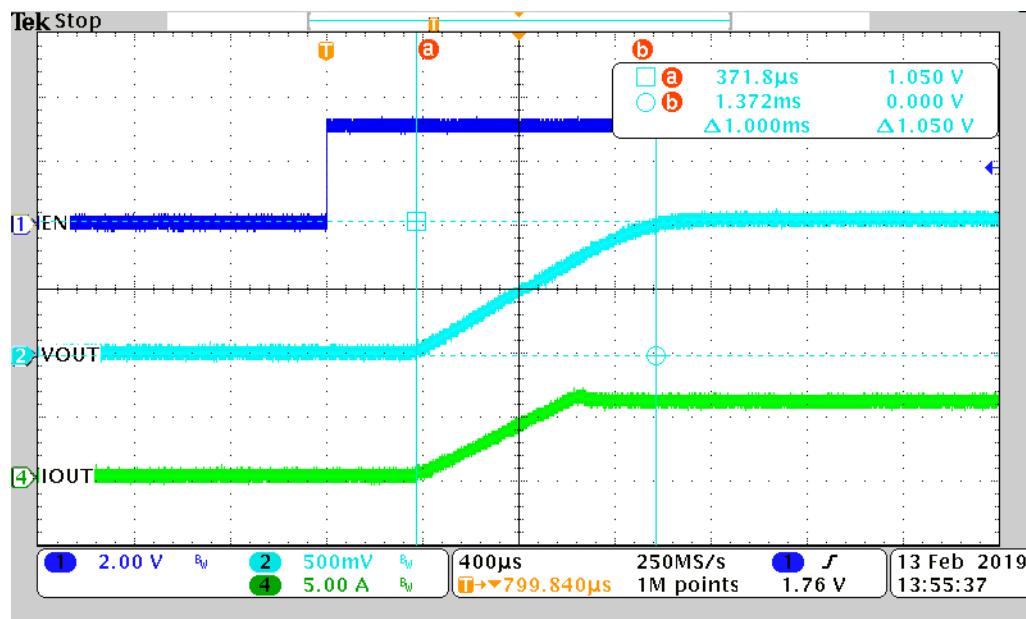
Start-up with VIN control enable signal:

1. Select operation mode at J3.
2. Connect JP1-1 pin to JP1-2 pin with jumper cap.
3. Apply 4.5-V - 18-V power supply to J1.
4. Apply load to J2 output connector.
5. Check the  $V_{OUT}$ .

## 6 Test Waveforms

### 6.1 Power Up

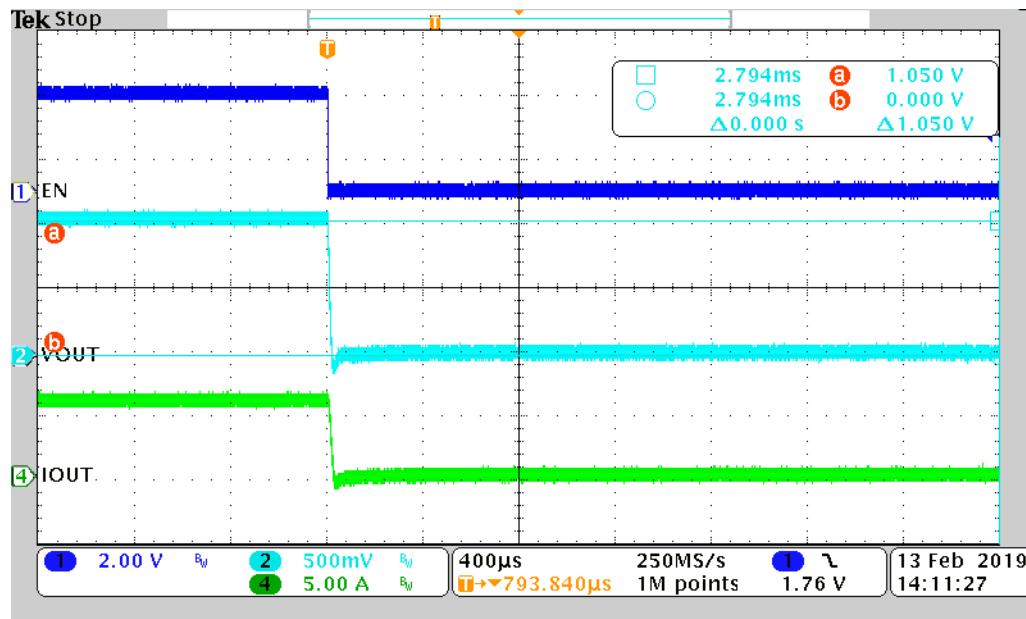
Figure 6-1 shows the power up waveform at 12-V input and 1.05-V output. Once the EN signal is high, V<sub>OUT</sub> starts to ramp up.



**Figure 6-1. Power up with 6 A loading controlled by EN pin**

### 6.2 Power Down

Figure 6-2 shows the power down waveform at 12-V input and 1.05-V output. Once the EN signal is low, V<sub>OUT</sub> starts to ramp down.



**Figure 6-2. Power Down with 6-A Loading Controlled by EN Pin**

## 6.3 Output Voltage Ripple

Figure 6-3 and Figure 6-4 show the  $V_{OUT}$  ripple at 12-V input and 1.05-V output.

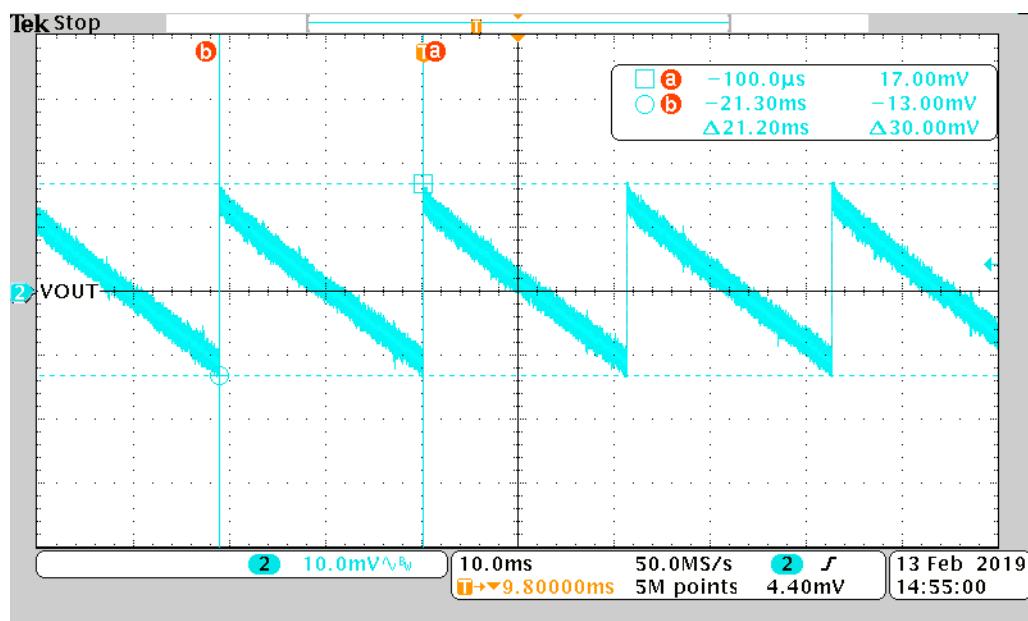


Figure 6-3.  $V_{OUT}$  Ripple with 0-A Loading

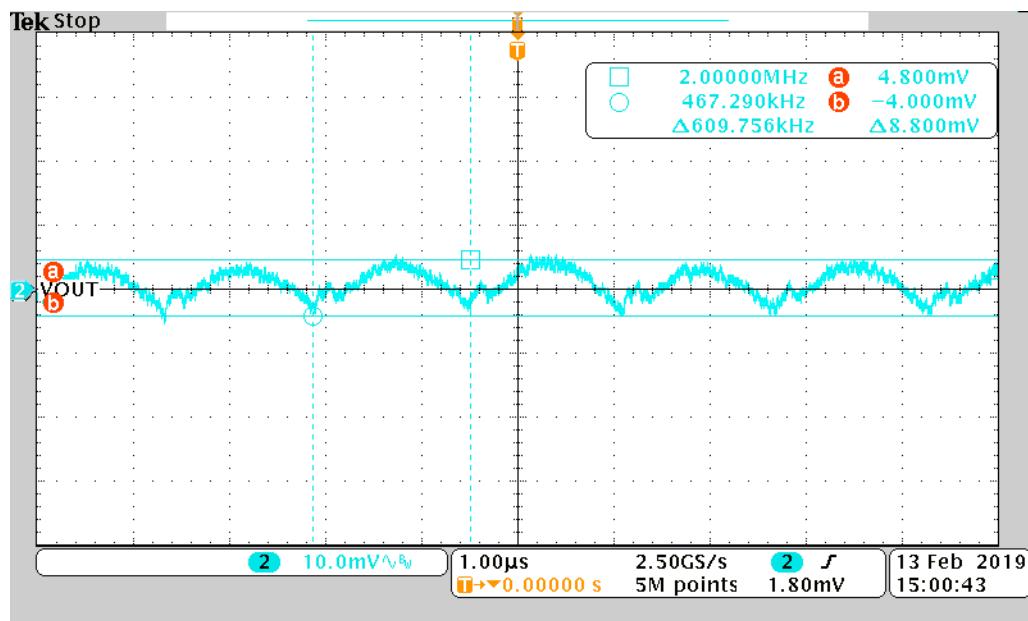


Figure 6-4.  $V_{OUT}$  Ripple with 6-A Loading

## 6.4 Load Transient Response

Figure 6-5 and Figure 6-6 show load transient response at 12-V input and 1.05-V output. The loading step slew rate is 2.5 A/uS.

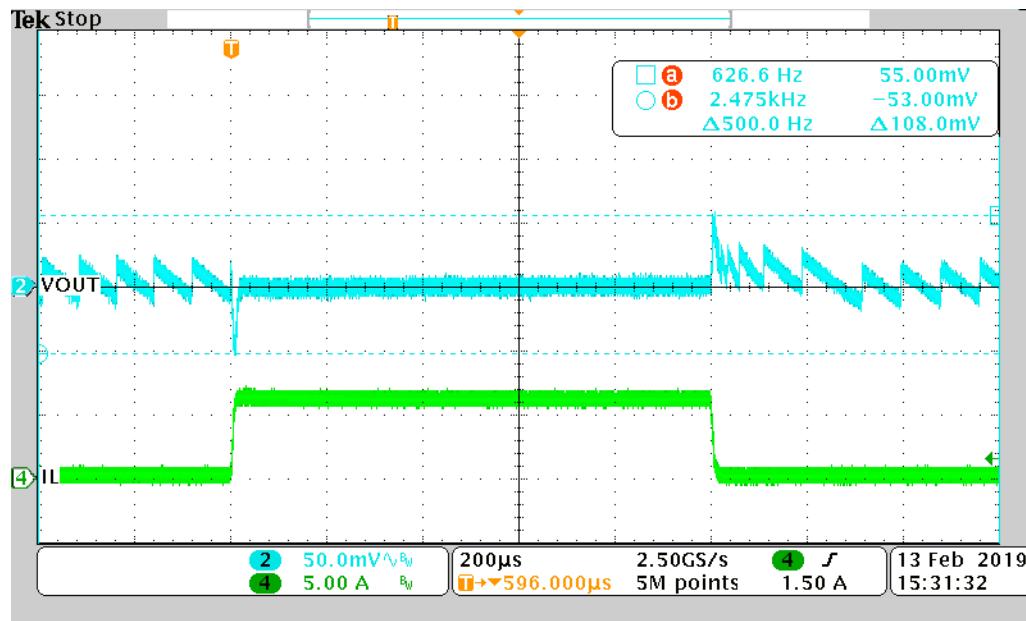


Figure 6-5. Load Transient Response from 0 A to 6 A with  $R_6 = 0 \Omega$  and  $C_{13} = 100 \text{ pF}$

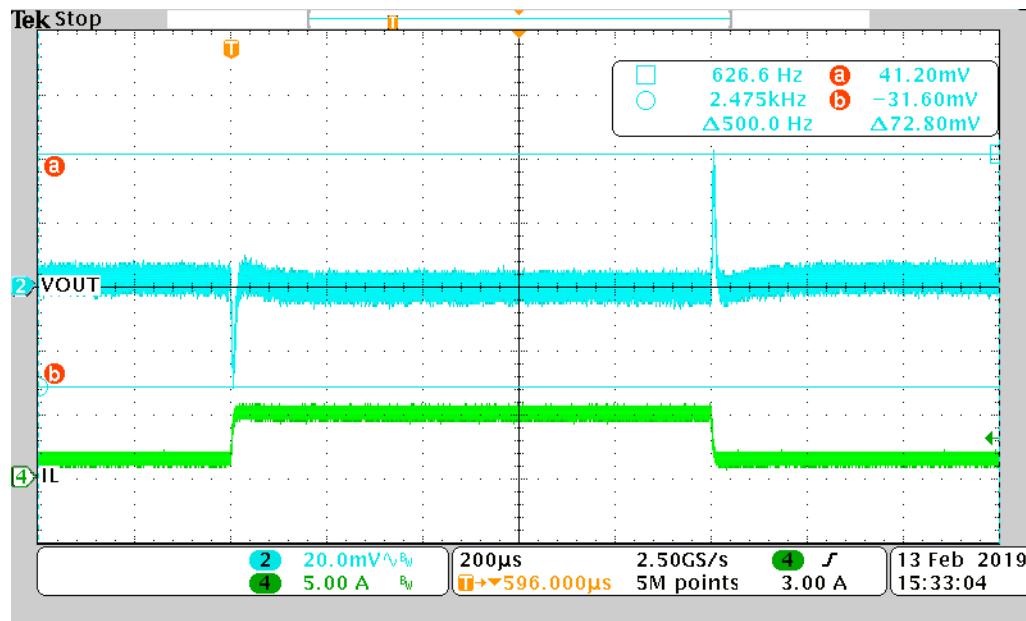
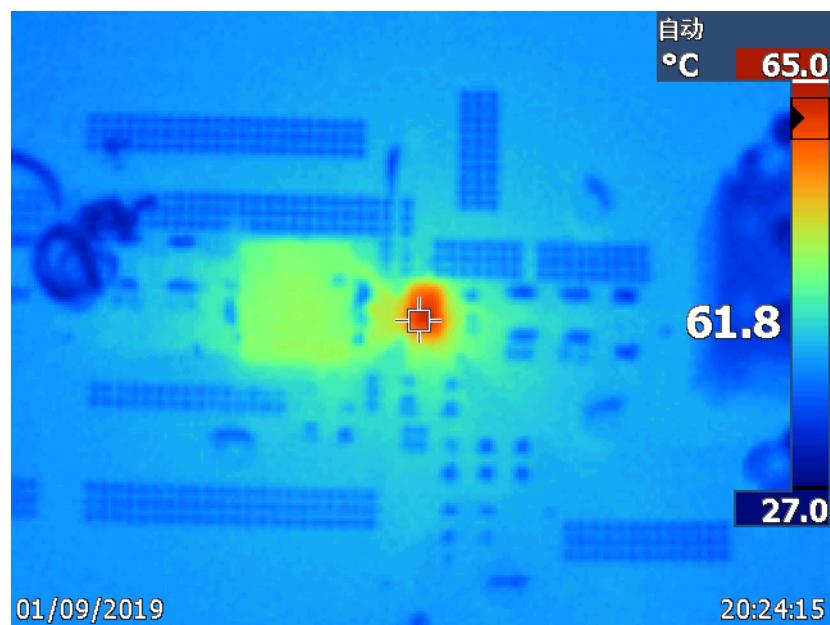


Figure 6-6. Load Transient Response from 1.2 A to 4.8 A with  $R_6 = 0 \Omega$  and  $C_{13} = 100 \text{ pF}$

## 6.5 Thermal

Figure 6-7 shows the thermal information at 12-V input, 1.05-V output, 6-A full loading under room temperature.



**Figure 6-7. Thermal Information at 6-A Full Loading**

## 7 List of Materials and Reference

### 7.1 List of Materials

Table 7-1 presents the List of materials for TPS566235EVM-036.

**Table 7-1. List of Materials**

Designator	Quantity	Description	Part Number	Manufacturer
PCB	1	Printed Circuit Board	BSR036	
C2, C3	2	Capacitor, ceramic, 22 $\mu$ F, 35 V, $\pm$ 20%, X5R, 1206	C3216X5R1V226M160AC	TDK
C4, C5, C11, C14	4	Capacitor, ceramic, 0.1 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0603	C1608X7R1H104K080AA	TDK
C6, C7, C8	3	Capacitor, ceramic, 22 $\mu$ F, 10 V, $\pm$ 10%, X7R, 1206	GRM31CR71A226KE15L	MuRata
C12	1	Capacitor, ceramic, 1 $\mu$ F, 25 V, $\pm$ 10%, X7R, 0603	06033C105KAT2A	AVX
D1	1	Diode, Zener, 5.1 V, 500 mW, SOD-123	MMSZ5231B-7-F	Diodes Inc.
H1, H2, H3, H4	4	Bumper, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2x1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 2.54mm, 3x2, gold, TH	61300621121	Wurth Elektronik
JP1	1	Header, 100mil, 3x1, tin, TH	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, shielded drum core, WE-superflux200, 1 uH, 15 A, 0.0046 $\Omega$ , SMD	744311100	Wurth Elektronik
R1, R9	2	Resistor, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R2	1	Resistor, 49.9, 1%, 0.1 W, 0603	CRCW060349R9FKEA	Vishay-Dale
R3	1	Resistor, 15.0 k, 1%, 0.1 W, 0603	CRCW060315K0FKEA	Vishay-Dale
R4, R5, R7, R10	4	Resistor, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
R8	1	Resistor, 20.0 k, 1%, 0.1 W, 0603	CRCW060320K0FKEA	Vishay-Dale
SH-JP1, SH-JP2	2	Shunt, 100mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP3, TP7, TP14	4	Terminal, turret, TH, triple	1598-2	Keystone
TP2, TP5, TP6, TP9, TP10, TP11, TP12, TP15	8	Test point, miniature, red, TH	5000	Keystone
TP4, TP8, TP13, TP16	4	Test point, miniature, black, TH	5001	Keystone
U1	1	4.5-V to 18-V, 6-A synchronous buck converter	TPS566235RJNR	Texas Instruments
C1	0	Capacitor, ceramic, 22 $\mu$ F, 35 V, $\pm$ 20%, X5R, 1206	C3216X5R1V226M160AC	TDK
C9, C10	0	Capacitor, ceramic, 22 $\mu$ F, 10 V, $\pm$ 10%, X7R, 1206	GRM31CR71A226KE15L	MuRata
C13	0	Capacitor, ceramic, 100 pF, 100 V, $\pm$ 5%, C0G/NP0, 0603	GRM1885C2A101JA01D	MuRata
R6	0	Resistor, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount		

### 7.2 Reference

- TPS566235 4.5-V to 18-V, 6-A synchronous step-down converter data sheet. ([SLVSEW1](#))

## 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2019) to Revision A (December 2022)	Page
• Updated user's guide title.....	<a href="#">2</a>
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	<a href="#">2</a>

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