User's Guide

Using the UCC21520EVM-286, UCC20520EVM-286, UCC21521CEVM-286, and UCC21530EVM-286

ABSTRACT

UCC2x5xxEVM-286 evaluation modules are designed for evaluation of TI's 5.7-kV_{RMS} isolated dual-channel gate driver family with 4-A source and 6-A sink peak current for driving Si MOSFETs, IGBTs and WBG devices such as SiC and GaN transistors. This user's guide covers the UCC21520EVM-286, UCC20520EVM-286, UCC21521CEVM-286, and UCC21530EVM-286 used to evaluate the UCC21520DW, UCC20520DW, UCC21521CDW, and UCC21530DWK, respectively. To evaluate other Iso-Drivers in the UCC2x5xx family, TI recommends that the user read the data sheet thoroughly before switching the part in the EVMs covered by this user guide. In this user guide, the UCC21520EVM-286 evaluation module is shown as the primary example, and the key differences between the UCC21520EVM-286 and the UCC20520EVM-286, UCC21521CEVM-286, and UCC21530EVM-286 will be highlighted accordingly.

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1 Introduction

Developed for high voltage applications where isolation and reliability is required, the UCC2x5xx delivers reinforced isolation of 5.7 kV_{RMS} and a surge immunity tested up to 12.8 kV along with a common-mode transient immunity (CMTI) greater than 100 V/ns. It has the industry's fastest propagation delay of 19 ns and the tightest channel-to-channel delay matching of less than 5 ns to enable high-switching frequency, high-power density, and efficiency.

The flexible, universal capability of the UCC2x5xx with up to 18-V VCCI and 25-V VDDA/VDDB allows the device to be used as a low-side, high-side, high-side/low-side, or half-bridge drivers with dual PWM input or single PWM input. With its integrated components, advanced protection features (UVLO, dead time and enable/disable), and optimized switching performances, the UCC2x5xx enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

2 Description

The UCC2x5xx evaluation board has three independent screw terminal blocks for VCCI, VDDA, and VDDB. The 3-position headers with jumpers for all the key input signals, such as PWM INPUTs (INA, INB or PWM), dead time (DT) programming and enable/disable function (EN/DIS), allow designers to easily evaluate different protection functions. A variety of testing points also support most of the key feature probing of the UCC2x5xx. Moreover, the PCB layout is not only optimized with minimized loop area in each gate driver loop and power supply loop with bypassing capacitors, but the layout also supports high voltage test between the primary side and secondary side with 120-mil PCB board cutout. Importantly, the creepage distance between two output channels are maximized with bootstrap diode in footprint of TO252-2(DPAK), which facilitates high-voltage, half-bridge testing for a wide variety of power converter topologies. For detail device information, refer to UCC21520DW, UCC20520DW, UCC21521CDW and UCC21530DWK data sheets and TI's Isolated gate driver solutions.

3 Features

- Evaluation module for the UCC21520DW, UCC20520DW, and UCC21521CDW in a wide body SOIC-16 (DW), along with the UCC21530DWK in wide body SOIC-14 (DWK) package
- 3-V to 18-V VCCI power supply range, and up to 25-V VDDA/VDDB power supply range
- 4-A and 6-A source/sink current capability
- 5.7-kV_{RMS} Isolation for 1 minute per UL 1577
- TTL/CMOS-compatible inputs
- Onboard trimmer potentiometer for dead-time programming
- 3-position header with for INA, INB, DT and enable/disable
- PCB layout optimized for power supply bypassing cap, gate driver loop
- PCB board cutout that facilitates high voltage isolation test between primary side and secondary side
- Maximized creepage distance between two output channels
- Support for half-bridge test with MOSFETs, IGBTs and SiC MOSFETs with connection to external power stage
- Testing points allows probing all the key pins of the UCC21520DW, UCC20520DW, UCC21521CDW, UCC21530DWK, and other wide-body ISO driver family parts.

3.1 I/O Description

Table 3-1. Jumpers Setting

PINS	DESCRIPTION
J1–VCCI	VCCI positive
J1-INA	INA/PWM signal
J1–GND	VCCI ground
J2–VCCI	VCCI positive
J2-INB	INB signal
J2–GND	VCCI ground
J3-VCCI	VCCI positive
J3-EN/DIS	Enable/Disable signal
J3–GND	VCCI ground
J4–VCCI	VCCI positive
J4-DT	Dead-time programming pin
J4-R2	Connects to trimmer potentiometer
TP1	Primary VCC input
TP2/TP4/TP6/TP8/TP10	Primary Ground input
TP3	INA/PWM signal input
TP5	INB signal input
TP7	EN/DIS signal input
TP9	Dead-time programing
TP17	VDDA secondary side supply
TP18	OUTA driver output
TP19	VSSA secondary side ground
TP20	VDDB secondary side supply
TP21	OUTB driver output
TP22	VSSB secondary side ground

3.2 Jumpers (Shunt) Setting

Table 3-2. Jumpers Setting

JACK	Jumper Setting Options		FACTORY SETTING
J-INA	Option A:	Jumper not installed, INA/PWM signal provided by external signal and this pin is default low if left open	Option A
	Option B:	Jumper on J1-INA and J1-GND set INA low	
	Option C:	Jumper on J1-INA and J1-VCCI set INA high	
J-INB	Option A:	Jumper not installed, INB signal provided by external signal and this pin is default low if left open	Option A for UCC21520EVM-286, UCC21521CEM-286 and UCC21530EVM-286; Option D for UCC20520EVM-286
	Option B:	Jumper on J2-INB and J2-GND set INB low	
	Option C:	Jumper on J2-INB and J2-VCCI set INB high	
	Option D:	Header J2-INB is not installed, and no connection on the device under test	
J-DIS or J-DIS/EN	Option A:	Jumper not installed, the devices under test are enabled when left open on enable/disable pin	Option C for UCC21520EVM-286 and UCC20520EVM-286; Option B for UCC21521CEVM-286 and UCC21530EVM-286
	Option B:	Jumper on J3-EN/DIS and J3-GND	
	Option C:	Jumper on J3-EN/DIS and J3-VCCI	
J-DT	Option A:	Jumper not installed, interlock with 8-ns dead time	Option B
	Option B:	Jumper on J4-DT and J4-VCCI allows driver output overlap or driver output follows PWM input for UCC21520EVM and UCC21521CEVM. The dead time will be around 0 ns in this option for UCC20520EVM	
	Option C:	Jumper on J4-DT and J4-R2 set the dead time by DT (in ns) = R_{DT} (in kΩ) × 10. For better noise immunity and dead-time matching, TI recommends to parallel a 2.2-nF or above bypassing capacitor from DT pin to GND.	

4 Electrical Specifications

Table 4-1. UCC2x5xxEVM-286 Electrical Specifications

DESCRIPTION		MIN	TYP	MAX	UNIT
V_{CCI}	Primary-side power supply	3		18	V
V_{DDA}, V_{DDB}	Driver output power supply for UCC21520EVM-286 and UCC20520EVM-286	9.2		25	V
	Driver output power supply for UCC21521CEM-286 and UCC21530EVM	14.7		25	V
F_S	Switching frequency	0		5	MHz
T_J	Operating junction temperature range	–40		125	°C

5 Test Summary

The UCC21520EVM-286 is used as the primary example for this section. Different Jumper settings, PWM signal input options and voltage source settings can be found in Section 2 and Section 4

5.1 Definitions

This procedure details how to configure the UCC2x5xx evaluation board. Within this test procedure the following naming conventions are followed. Refer to the UCC21520EVM-286 Schematic in Figure 8-1 for details.

V_{XX}	External voltage supply name
$V_{(TPxx)}$	Voltage at test point TPxx. For example, V(TP12) means the voltage at TP12
$V_{(Jxx)}$	Voltage at jack terminal Jxx
$J_{xx(yy)}$	Terminal or pin yy of jack xx
DMM	Digital multi-meters
UUT	Unit under test
EVM	Evaluation module assembly, in this case the UUT assembly drawings have location for jumpers, test points and individual components

5.2 Equipment

5.2.1 Power Supplies

Three DC power supply with voltage/current above 25 V/1 A (for example, Agilent E3634A).

5.2.2 Function Generators

One two-channel function generator over 20 MHz (for example, Tektronics AFG3252).

5.3 Equipment Setup

5.3.1 DC Power Supply Settings

- DC power supply #1
  - Voltage setting: 5 V
  - Current limit: 0.05 A
- DC power supply #2
  - Voltage setting: 12 V for UCC21520EVM and UCC20520EVM
  - Voltage setting: 15 V for UCC21521CEVM and UCC21530EVM
  - Current limit: 0.1 A
- DC power supply #3
  - Voltage setting: 12 V for UCC21520EVM and UCC20520EVM
  - Voltage setting: 15 V for UCC21521CEVM and UCC21530EVM
  - Current limit: 0.1 A

5.3.2 Digital Multi-Meter Settings

- Digital multi-meter #1
  - DC current measurement, auto-range.
- Digital multi-meter #2
  - DC current measurement, auto-range.

5.3.3 Two-Channel Function Generator Settings

Table 5-1. Two-Channel Function Generator Settings

	MODE	FREQUENCY	DUTY	DELAY	HIGH	LOW	OUTPUT IMPEDANCE
Channel A	Pulse	DC ~ 5 MHz	50%	0 ns	3.3 V	0 V	High Z
Channel B				100 ns			

5.3.4 Oscilloscope Setting

Table 5-2. Oscilloscope Settings

	BANDWIDTH	COUPLING	TERMINATION	SCALE SETTINGS	INVERTING
Channel A	500 MHz or above	DC	1 MΩ or automatic	10× or automatic	OFF
Channel B					

5.3.5 Jumper (Shunt) Settings

There are two jumpers (shunts) need to be installed before test:

1. Install shunt #1 for header *J3-DIS* on pin EN/DIS-GND for the UCC21520EVM shown in Figure 5-1. For the UCC20520EVM, UCC21521CEVM and the UCC21530EVM, refer to Table 3-1. The UCC20520EVM is set as disable high on the DIS pin while the UCC21521CEM and UCC21530EVM is set as enable high on the EN pin.
2. Install shunt #2 on header *J4-DT* on pin VCCI-DT as shown in Figure 5-1.

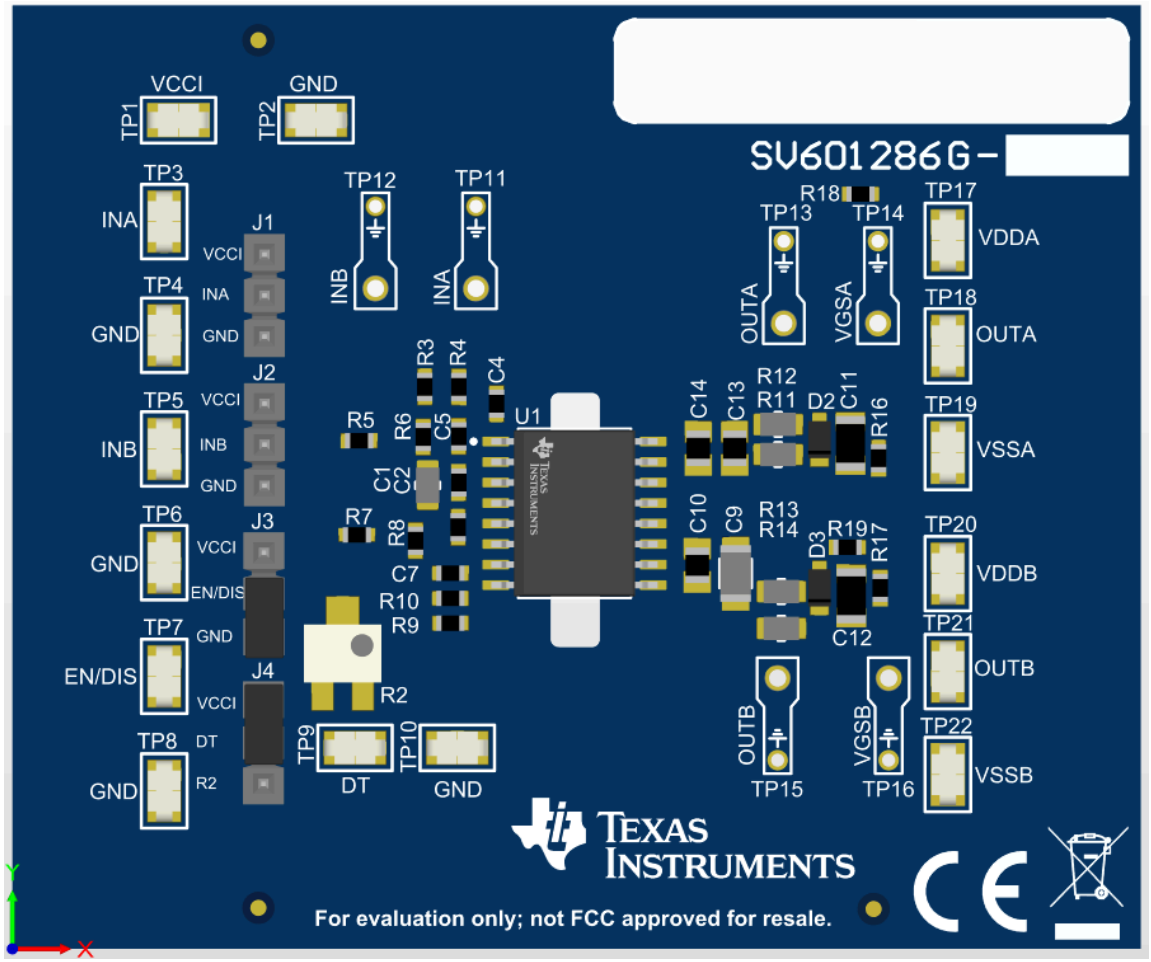

Figure 5-1. Jumpers Installation Position

5.3.6 Bench Setup Diagram

The current bench setup diagram includes the function generator and oscilloscope connections.

Use the following connection procedure and also use Figure 5-2 as a reference:

- Make sure all the output of the function generator, voltage source are disabled before connection;
- Function generator channel-A channel applied on INA (TP3) ⟷ GND (TP14) as seen in Figure 5-2;
- Function generator channel-B channel applied on INB (TP5) ⟷ GND (TP6) as seen in Figure 5-2. For the UCC20520EVM, INB, J-INB and TP15 are not installed because the UCC20520 is a single PWM input, dual-channel output Iso-Driver;
- Power supply #1: positive node applied on VCCI (TP1), and negative node applied on GND (TP2);
- Power supply #2: positive node connected to input of DMM #1 and DMM #1 output connected to VDDA (TP17), negative node connected directly to VSSA (TP19);
- Power supply #3: positive node connected to input of DMM #2 and DMM #2 output connected to VDDB (TP20), negative node connected directly to VSSB (TP22);
- Oscilloscope channel-A probes TP14, smaller measurement loop is preferred;
- Oscilloscope channel-B probes TP16, smaller measurement loop is preferred;

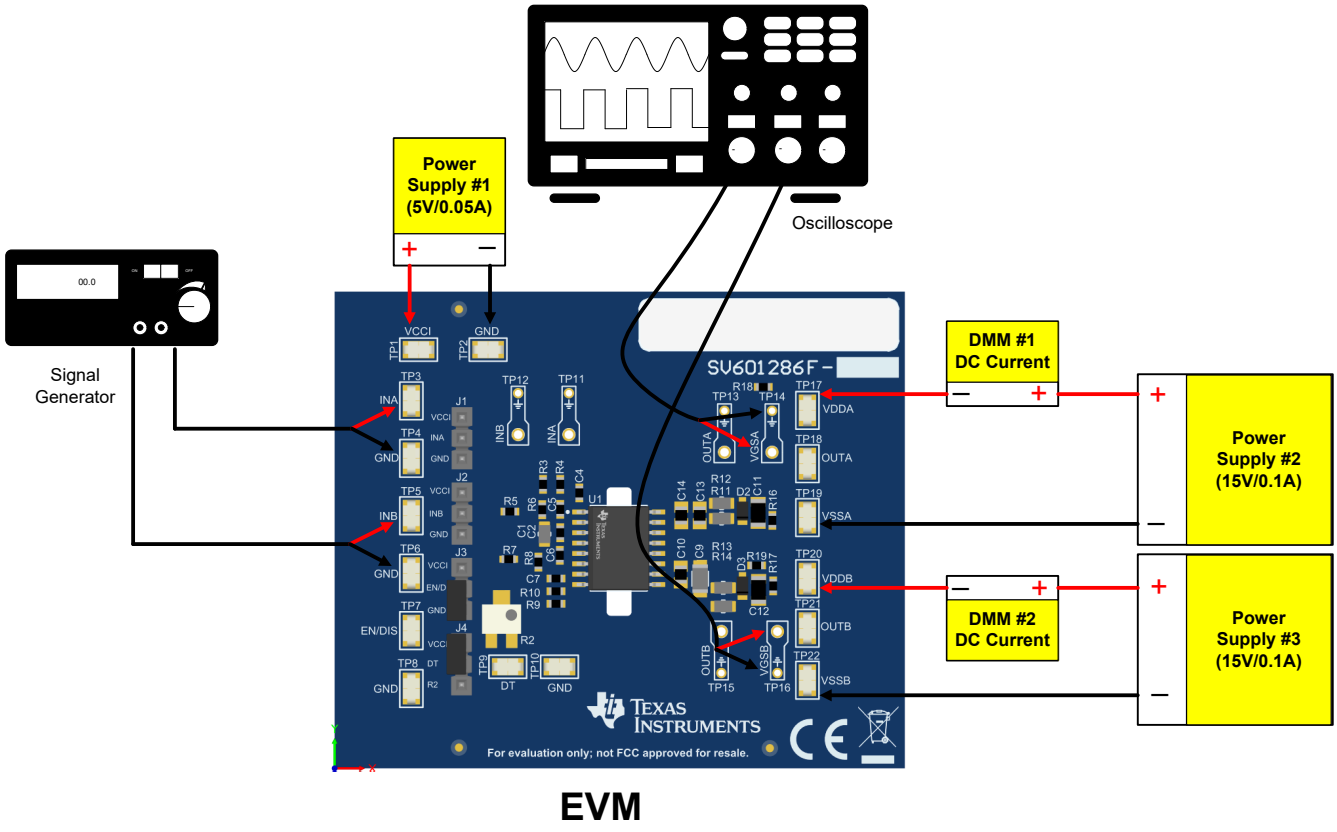

Figure 5-2. Bench Setup Diagram and Configuration

6 Power-Up and Power-Down Procedure

6.1 Power Up

1. Make sure that Section 5.3.6 is implemented for setting up all the equipment before starting the power-up sequence. Figure 6-1 can be used as a reference.
2. Enable supply #1;
3. Enable supply #2 and #3, the quiescent current on DMM1 and DMM2 ranges from 1 mA to approximately 3 mA if everything is set correctly;
4. Enable the function generator, two-channel outputs: channel-A and channel-B;
5. There will be:
   a. Stable pulse output on the channel-A and channel-B in the oscilloscope (refer to Figure 6-1);
   b. Scope frequency measurement is the same with function generator output;
   c. DMM #1 and #2 read measurement results should be around 10 mA, ±2 mA under no load conditions. For more information about operating current, refer to the UCC21520 data sheet.

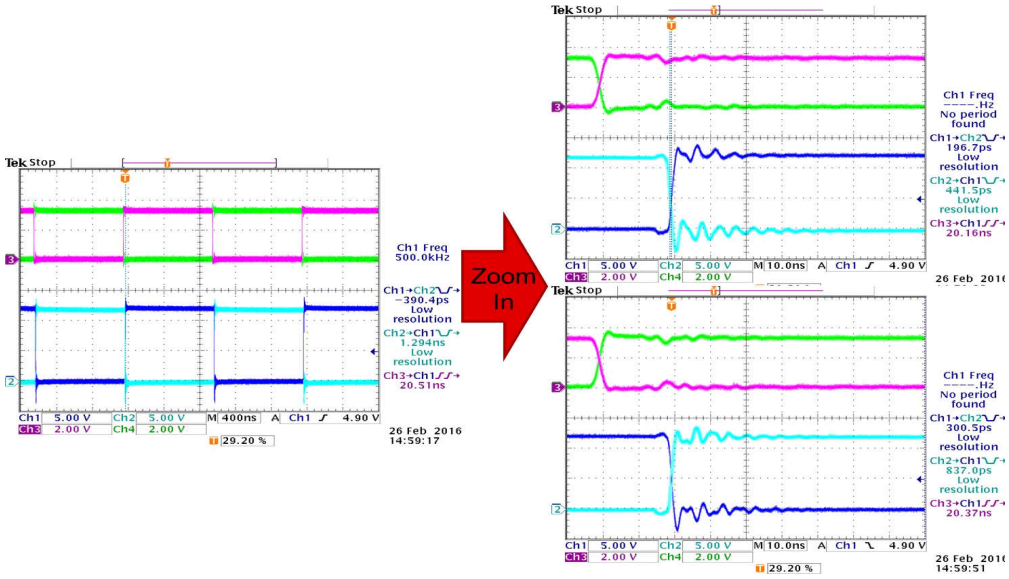

Figure 6-1. Example Input and Output Waveforms (Channels 3 and 4 are PWM Inputs, Channels 1 and 2 are Outputs)

6.2 Power Down

1. Disable function generator;
2. Disable power supply #2 and #3;
3. Disable power supply #1;
4. Disconnect cables and probes;

7 Test Waveforms (C_L=0pF) With Different DT Configurations

7.1 DT Connected to VCCI (J-DT Option B in Table 3-2)

The dead time (DT) between the outputs of the two channels is decided by inputs (see Figure 7-1). Overlap between two output channels is allowed. Figure 7-1 shows a waveform with overlapped operations.

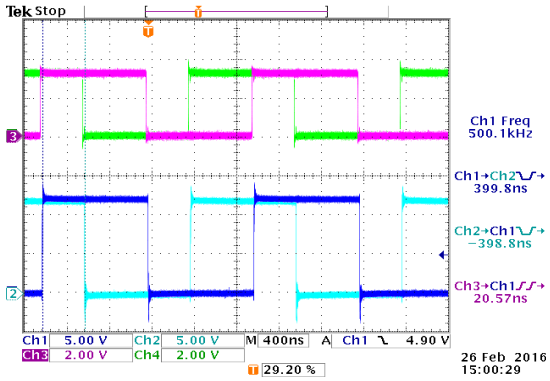

Figure 7-1. Overlap is Allowed When DT Connected to VCCI (Channels 3 and 4 are PWM Inputs, Channels 1 and 2 are Driver Outputs)

7.2 DT Pin Floating or Left Open (J-DT Option A in Table 3-2)

The dead time (DT) between the outputs of the two channels is around 8 ns, which is preset for interlock protections (see Figure 7-2).

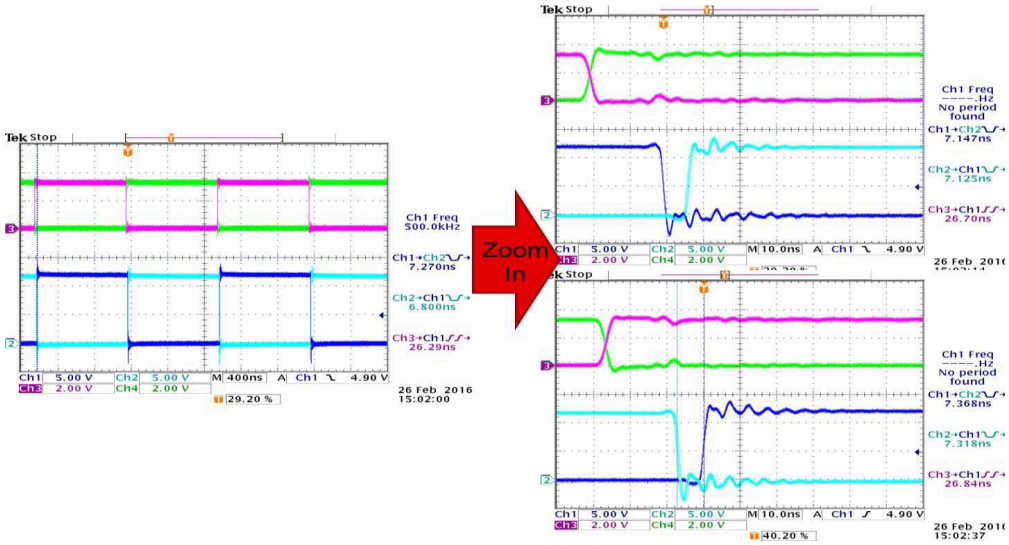

Figure 7-2. Test Waveforms if DT is Left Open (Channel 3 and 4 are PWM Inputs, and Channel 1 and 2 are Driver Outputs)

7.3 DT Pin Connected to RDT (J-DT Option C in Table 3-2)

The dead time (DT) between the outputs of the two channels is set according to: DT (in ns) = 10 × RDT (in kΩ).

The steady-state voltage at DT pin is around 0.8 V, and the DT pin current will be less than 10 µA when R_{DT} = 100 kΩ. Therefore, TI recommends to parallel a ceramic bypass capacitor (2.2 nF or above) with R_{DT} to achieve better noise immunity and better dead-time matching between two channels, especially when the dead time is larger than 300 ns. The major consideration is that the current through the R_{DT} is used to set the dead time, and this current decreases as R_{DT} increases. This bypass capacitor is not installed in the EVM, but the user can easily install it on the bottom layer where the R_{DT} is located.

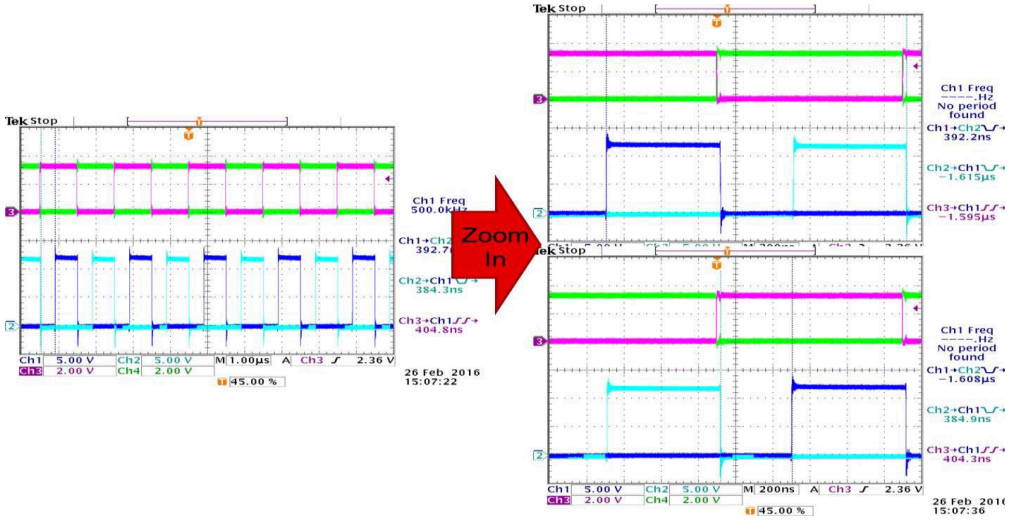

Figure 7-3. Test Waveforms if DT Connected to R_{DT} (Channel 3 and 4 is PWM Inputs, and Channel 1 and 2 is Driver Outputs)

8 Schematic

Figure 8-1 only shows the schematic diagram for UCC21520EVM. The schematic diagrams for the UCC20520EVM, UCC21521CEVM, and UCC21530EVM are similar to Figure 8-1, with the exception that the device under test (U1) could be in one of the following driver ICs: UCC21520DW, UCC20520DW, UCC21521CDW, or UCC21530DWK.

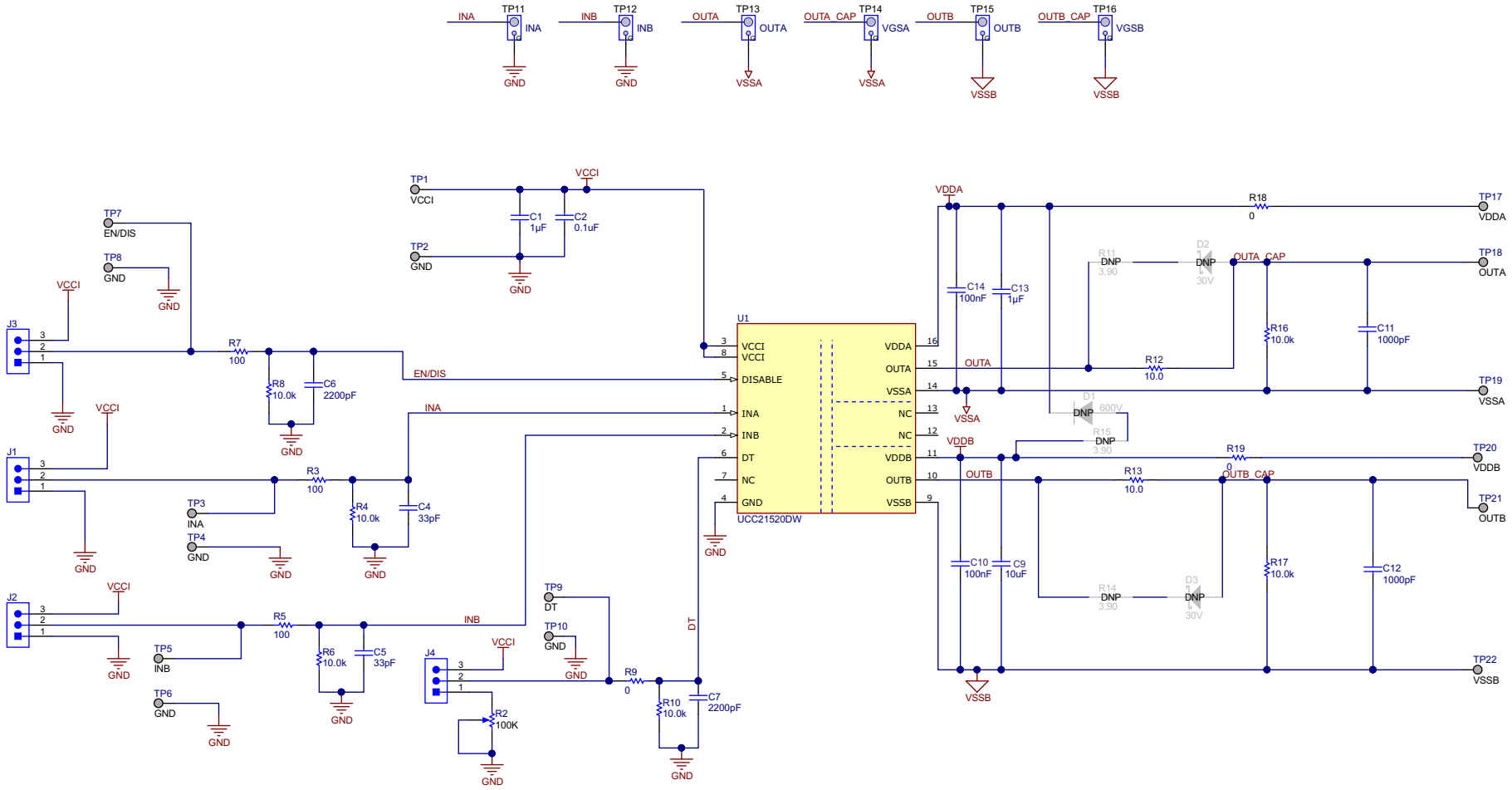

Figure 8-1. UCC21520EVM-286 Schematic

9 Layout Diagrams

The PCB layout information for UCC21520EVM is shown in Figure 9-1, Figure 9-2, Figure 9-3, and Figure 9-4. The layouts are the same for UCC20520EVM, UCC21521CEVM, and UCC21530EVM except for the labels that designate the EVM part number with the device under test.

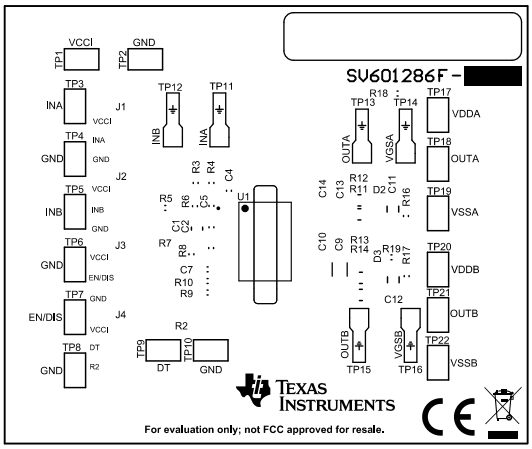

Figure 9-1. Top Overlay

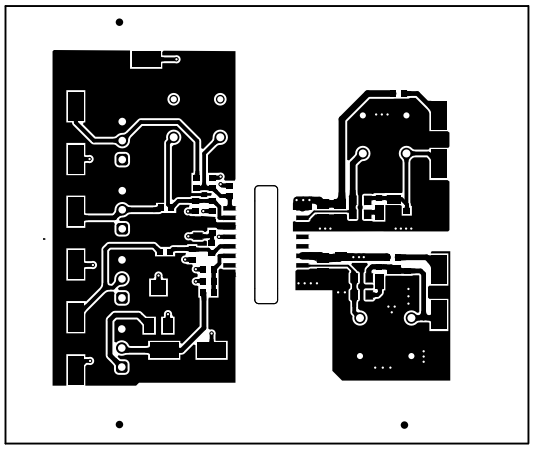

Figure 9-2. Top Layer

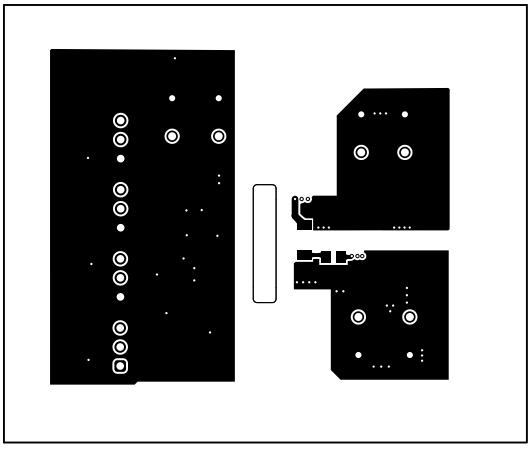

Figure 9-3. Bottom Layer

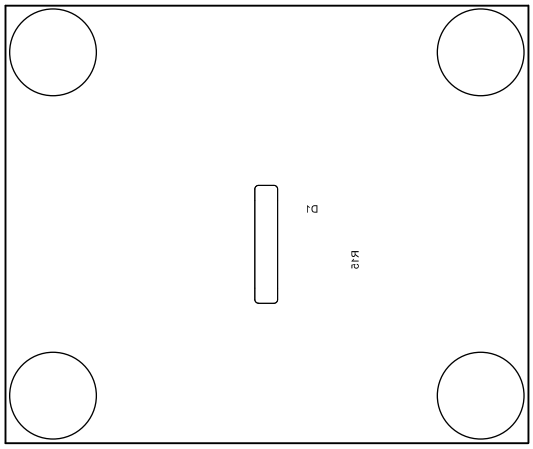

Figure 9-4. Bottom Overlay

10 List of Materials

Table 10-1. UCC2x5xxEVM-286 List of Materials

QTY	DES	DESCRIPTION	MANUFACTURE	PART NUMBER
2	C1, C13	CAP, CERM, 1 µF, 50 V,+/- 10%, X7R, 0805	Std	Std
1	C2	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	Std	Std
2	C4, C5	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0603	Std	Std
2	C6, C7	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	Std	Std
1	C9	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1206	Std	Std
2	C14, C10	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	Std	Std
2	C11, C12	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 1206	Std	Std
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Std	Std
4	J1, J2, J3, J4	Header, 2.54 mm, 3x1, Tin, TH	Std	Std
1	R2	Trimmer, 100 K, 0.25 W, SMD	Std	Std
3	R3, R5, R7	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Std	Std
6	R4, R6, R8, R10, R16, R17	RES, 10.0 k, 1%, 0.1 W, 0603	Std	Std
3	R9, R18, R19	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	Std	Std
2	R12, R13	RES, 10.0, 1%, 0.5 W, AEC-Q200 Grade 0, 0805	Std	Std
2	SH1, SH2	Shunt, 100mil, Flash Gold, Black	Std	Std
16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP17, TP18, TP19, TP20, TP21, TP22	Test Point, Miniature, SMT	Std	Std
0	D1	Diode, Ultrafast, 600 V, 1 A, SMA	Not Populated	Not Populated
0	D2, D3	Diode, Schottky, 30 V, 1 A, AEC-Q101, MicroSMP	Not Populated	Not Populated
0	R11, R14, R15	RES, 3.90, 1%, 0.125 W, 0805	Not Populated	Not Populated
1	U1	UCC21520DW, UCC20520DW, UCC21521CDW and UCC21530DWK, 4-A and 6-A, 5-KV_{RMS} Dual Isolated-channel Universal Gate Driver, DW0016A and DWK0014 for UCC21530DWK	Texas Instruments	UCC21520DW, UCC20520DW, UCC21521CDW, or UCC21530DWK

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2018) to Revision C (October 2021) Page

Changes from Revision A (November 2016) to Revision B (November 2018)	Page
• Added device type to include the UCC21530EVM-286 Evaluation Module	1

Changes from Revision * (June 2016) to Revision A (November 2016)	Page
• Added device type to include the UCC20520EVM-286 and UCC21521CEVM-286 Evaluation Modules	1

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