Using the UCD9224EVM-464

User's Guide



Literature Number: SLUU443 March 2011



UCD9224EVM-464 Digitally Controlled Dual-Rail POL

This user guide describes the evaluation module (EVM) for the UCD9224 Digital PWM System Controller and the UCD7242 Digital Dual Synchronous Buck Power Driver. The UCD9224 is a multi-rail, multi-phase synchronous buck digital PWM controller designed for non-isolated DC/DC power applications. This device combines dedicated circuitry for loop management with a microcontroller, flash memory, and a serial interface to support configurability, monitoring and management. The UCD7242 Dual Synchronous-Buck Power Driver, the foundation of the PTD08D210W Digital PowerTrain™ module, simplifies POL rail development by integrating and optimizing many of the power train components (driver, MOSFETS, current sensing and protection features) needed to realize two voltage phases/rails.

2 Description

The UCD9224EVM-464 includes the Digital Power Controller paired with the UCD7242 driver on the PTD08D210W module to create a power system consisting of two single-phase, point-of-load (POL) power rails, each capable of up to 10 A of output current.

For evaluation purposes, the EVM is supplied pre-configured to operate from a 12-V +/- 10% input voltage source and will produce stepped down voltages of 2.5 V (V_{OUT1}) and 1.2 V (V_{OUT2}) without user intervention once the input voltage has reached the power system's under-voltage lockout that is set within the controller.

The PMBusTM compatible serial data interface included on the EVM allows the user to connect the power system to a Windows based host computer running the Fusion Digital PowerTM Designer software with the USB Interface Adapter EVM (refer to the Section 5: Test Setup for links to the software and adapter website and documentation). The UCD9224EVM-464 output rails can then be monitored and controlled or further configured within the functional limits of the PTD08D210W module (V_{IN} from 4.5 V to 14.0 V and V_{OUT} from 0.7 V to 3.6 V), refer to document SLUU490 - Using the UCD92xx Digital Point of Load Controller for additional information.

For power systems requiring the features found in the UCD9224, (up to 2 rails/4 phases but needing additional phases/rails then), the UCD9246, (up to 4 rails/6 phases), and UCD9248, (up to 4 rails/8 phases), digital controllers are available. Additionally, complex power systems can be implemented with multiple controllers, all sharing the same PMBus ™ interface, and configured to operate as a complete power solution.

2.1 Typical Applications

- Industrial / Automated Test Systems
- Telecom / Networking Equipment
- Servers
- Storage Systems
- FPGA, DSP and Memory Systems



www.ti.com Description

2.2 Features

UCD9224

- Fully Configurable Multi-Output and Multi-Phase Non-Isolated DC/DC PWM Controller
- Controls Up to 2 Voltage Rails and Up to 4 Phases
- Supports Switching Frequencies Up to 2 MHz with 250-ps Duty-Cycle Resolution
- Up To 1-mV Closed Loop Resolution
- Hardware-Accelerated, 3-Pole/3-Zero Compensator with Non-Linear Gain for Improved Transient Performance
- Supports Multiple Soft-Start and Soft-Stop Configurations Including Prebias Start up
- Supports Voltage Tracking, Margining and Sequencing
- Supports Current and Temperature Balancing for Multi-Phase Power Stages
- Supports Phase Adding/Shedding for Multi-Phase Power Stages
- Sync In/Out Pins Align DPWM Clocks Between Multiple UCD92xx Devices
- 12-Bit Digital Monitoring of Power Supply Parameters Including:
 - Input/Output Current and Voltage
 - Temperature at Each Power Stage
- Multiple Levels of Over-current Fault Protection:
 - External Current Fault Inputs
 - Analog Comparators Monitor Current Sense Voltage
 - Current Continually Digitally Monitored
- Over and Under-voltage Fault Protection
- Over-temperature Fault Protection
- Enhanced Nonvolatile Memory with Error Correction Code (ECC)
- Device Operates From a Single Supply with an Internal Regulator Controller That Allows Operation Over a Wide Supply Voltage Range
- Supported by Fusion Digital Power™ (<u>UCD9224 Datasheet</u>) Designer, a Full Featured PC Based Design Tool to Simulate, Configure, and Monitor Power Supply Performance



Description www.ti.com

PTD08D210W Module

- Dual 10-A Outputs
- Programmable Wide-Output Voltage
 - 0.7 V to 3.6 V
- 4.75-V to 14-V Input Voltage
- Efficiencies up to 96%
- Digital I/O
 - PWM input
 - Fault Flag (FF) output
 - Synchronous Rectifier Enable (SRE) input
- Analog I/O
 - Temperature Output
 - Output Current reporting
- Operating Temperature: -40°C to 85°C

UCD7242 Driver

- Fully Integrated Power Switches and Drivers for Dual Synchronous Buck Converters
- Wide Input Voltage Range of 4.75 V to 18 V (operation to 2.2 V with external VGG bias voltage)
- Up to 10-A Output Current Per Channel
- Operational to 2-MHz Switching Frequency
- High-Side Current Limit With Current Limit Flag
- Onboard Regulated 6-V Driver Supply From VIN
- Thermal Protection
- Temperature Sense Output Voltage Proportional to Chip Temperature
- UVLO and OVLO Circuits Ensure Proper Drive Voltage
- Rated From –40°C to 125°C Junction Temperature
- RoHS Compliant
- Accurate On-Die Current Sensing (±5%)



3 Electrical Performance Specifications

Table 1. UCD9224EVM-464 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics		"	"	1	
Voltage range	As configured, EVM input capable of 4.75 V to 14.0 V	10.8 12 13.2		13.2	V
No load input current		135		mA	
Controller turn-on voltage	Input voltage above which outputs become enabled	11.0		V	
Controller turn-off voltage	Input voltage below which outputs become disabled			10.5	
Controller OVP protection	Input voltage above which operation is latched off	13.8			
Output Characteristics					
Output voltage, VOUT1	utput voltage, VOUT1 $I_{OUT1} = 10 \text{ A}$ 2.450		2.5	2.550	V
Output load current, IOUT1				10	
Output voltage regulation	Line regulation: $V_{IN} = 10.8 \text{ V}$ to 13.2 V, $I_{OUT1} = 10 \text{ A}$		<1.0%		
	Load regulation: $I_{OUT1} = 10\%$ to 100%, $V_{IN} = 12 \text{ V}$		<1.0%		
Output voltage ripple	I _{OUT1} = 10 A		30		mVpp
Output over current			12.5		Α
Output voltage, VOUT2	Output current = 10 A	1.750	1.8	1.850	V
Output load current, IOUT2				10	Α
Output voltage regulation	Line regulation: $V_{IN} = 10.8 \text{ V}$ to 13.2 V, $I_{OUT2} = 10 \text{ A}$		<1.0%		
	Load regulation: $I_{OUT2} = 10\%$ to 100%, $V_{IN} = 12 \text{ V}$		<1.0%		
Output voltage ripple	I _{OUT2} = 10 A		25		mV_{PP}
Output over current			12.5		Α
Systems Characteristics					
Switching frequency			750		kHz
Efficiency	2.5 V at 10 A, 1.2 V at 0 A		87.5%		
	1.2 V at 10 A, 2.5 V at 0 A		78.2%		
Operating temperature			25		°C



4 Assembly / Schematic Layouts

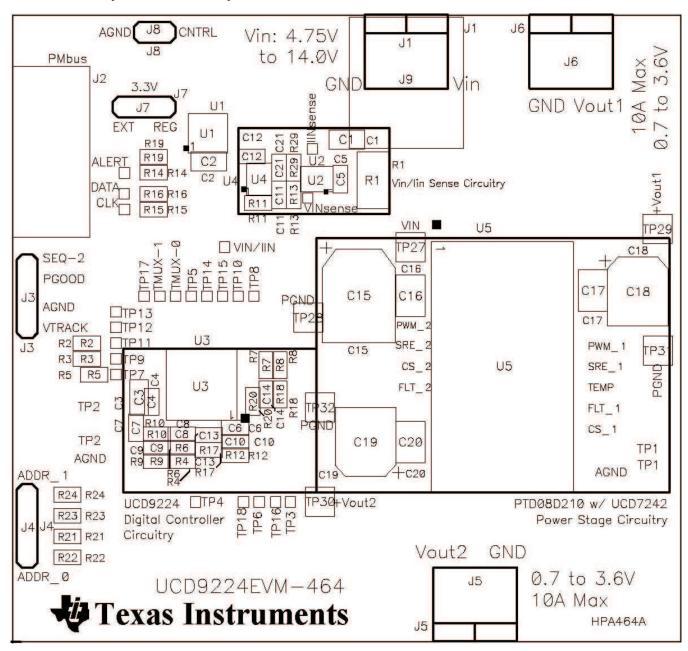


Figure 1. Top Assembly



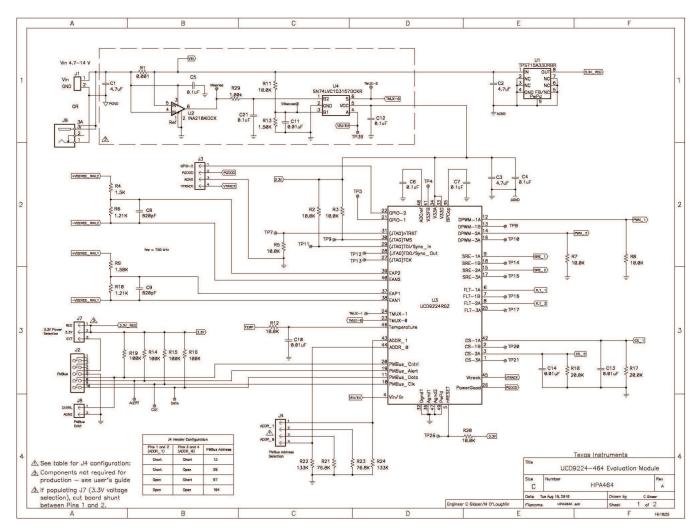


Figure 2. Schematic 1



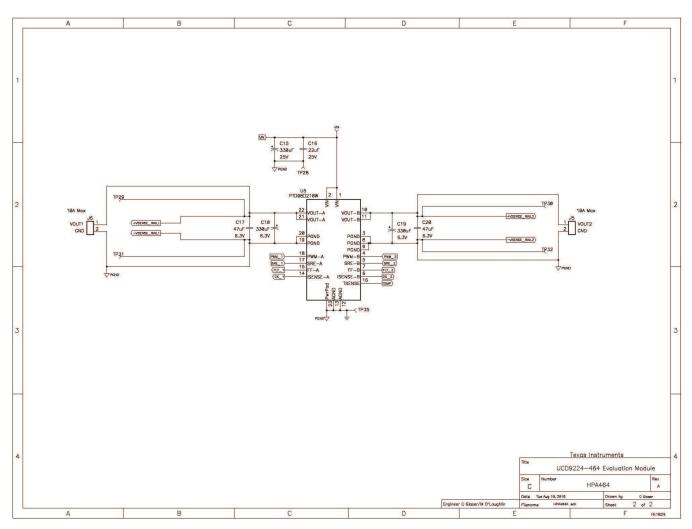


Figure 3. Schematic 2



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5 Test Setup

5.1 Test Equipment

Input Voltage Source: 12-V power supply with at least a 5-A sourcing capability.

Multimeters: Two 5 ½ digit digital multimeters.

Output Load: Two electronic loads capable of sinking 10 A from low voltage (<1 V) sources.

Oscilloscope: Minimum 4-channel, 100-MHz bandwidth with storage capability.

Fan: Not required but may be desirable if testing at full output power.

Recommended Wire Gauge: Input Voltage: 20 AWG min. Output Load: 16 AWG min.

5.1.1 Test configuration, Monitoring and Control Functionality

PC computer running Microsoft OS version:

- XP (32 bit)
- Vista (32 bit)
- Vista (64 bit untested, should be compatible)
- 7 (32 or 64 bit)

Texas Instruments' USB Interface Adapter EVM - P/N USB-to-GPIO, User's Guide - SLLU093

Fusion Digital Power Designer Software Installer Executable File:

fusion digital power designer download for power controllers version 1 8 6.exe or newer



Test Setup www.ti.com

5.2 Recommended Test Setup

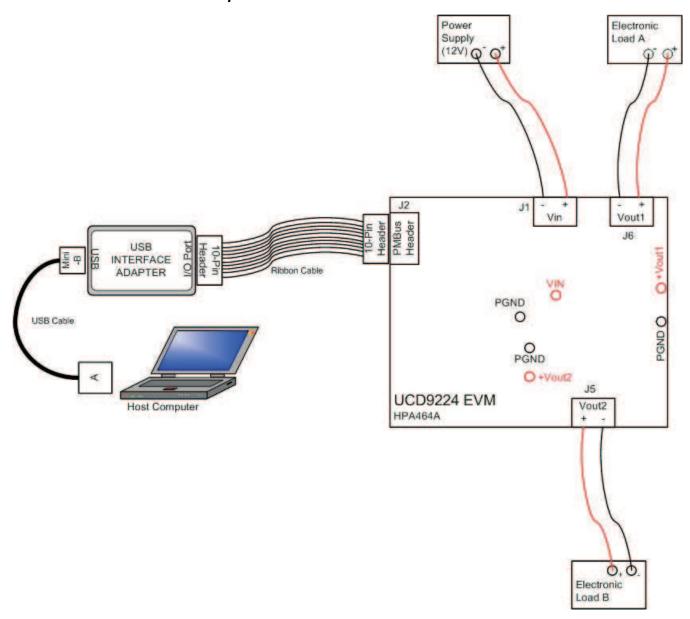


Figure 4. UCD9224EVM-464 Recommended Test Set Up



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5.3 List of Connectors

Table 2. Connector definition

CONNECTORS	PINS	NAME	DESCRIPTION
J1	1	VIN	Input voltage
	2	GND	Input voltage return
J2	1 thru 4	GND	USB interface adapter - unconnected
	5		USB interface adapter – 3.3V 100ma supply (optional)
	6		USB interface adapter – ground
	7	PMBus_CNTRL	USB interface adapter – control line
	8	PMBus_ALERT	USB interface adapter – alert line
	9	PMBus_CLK	USB interface adapter – clock line
	10	PMBus_DATA	USB interface adapter – data line
J3	1	GPIO-1	General purpose input/output – UCD9224 pin 22 (SEQ-2)
	2	PGOOD	Power good – all rails (UCD9224 Pin 26)
	3	AGND	Analog ground reference point for external signals
	4	VTRACK	Input reference for external voltage tracking
J4	2-Jan	ADDR-1	Jumper location to modify ADDR-1 setting
	4-Mar	ADDR-0	Jumper location to modify ADDR-0 setting
J5	1	+V _{OUT2}	Output voltage 2
	2	-V _{OUT2}	Output voltage 2 return
J6	1	+V _{OUT1}	Output voltage 1
	2	-V _{OUT1}	Output voltage 1 return
J7 (optional)	1	REG	3.3 V from onboard regulator U1 (1)
	2	3.3 V	3.3-V supply for UCD9224 controller (1)
	3	EXT	3.3 V from J2-5 (PMBus)
J8	1	CNTRL	Manual control line access
	2	AGND	Ground
J9 (optional)	1	GND	Input voltage return (2)
	2		Unconnected
	3/3 A	VIN	Input voltage (2)

⁽¹⁾ J7 is not populated by default and a shunt trace connects Pins 1 and 2 on the EVM.

⁽²⁾ J9 (DC power jack) replaces J1 to allow use of a standard 5.5mm/2.5mm power adapter plug.



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5.4 List of Test Points

Table 3. Test Point Functions

TEST POINTS	NAME	DESCRIPTION	
TMUX0	TMUX0	Output low bit to drive multiplexor for temperature and V_{IN}/I_{IN}	
TMUX1	TMUX1	Output high bit to drive multiplexor for temperature	
VIN/IIN	Vin/lin	Input supply sense (after multiplexor) – alternates between V _{IN} /I _{IN}	
VIN	Vin	Input voltage referenced to PGND	
+Vout1	+V _{OUT}	Output voltage for rail #1 referenced to PGND	
+Vout2	+V _{OUT2}	Output voltage for rail #2 referenced to PGND	
PGND	Power Ground	Power ground reference	
VINsense	Vinsense	V _{IN} sense (prior to multiplexor)	
IINsense	linsense	I _{IN} sense (prior to multiplexor)	
PWM_1	DPWM-1A	Digital pulse width modulator output 1A	
PWM_2	DPWM-2A	Digital pulse width modulator output 2A	
SRE_1	SRE-1A	Synchronous rectifier enable output 1A	
SRE_2	SRE-2A	Synchronous rectifier enable output 2A	
FLT_1	FLT-1A	External fault input 1A	
FLT_2	FLT-2A	External fault input 2A	
CS_1	CS-1A	Power stage 1A current sense input and input to analog comparator 1	
CS_2	CS-2A	Power stage 2A current sense input and input to analog comparator 2	
TP1	AGND	Analog ground reference	
TP2	AGND	Analog ground reference	
TP3	nRESET	Reset pin – active low	
TP4	V33FB	Base drive control for 3.3-V linear regulator transistor (no connect if using an external 3.3-V LDO regulator)	
TP5	SEQ-1	Sequencing input/output (GPIO)	
TP6	CS-1B	Power stage 1B current sense input	
TP7	nTRST	JTAG test reset (pull-down to ground using 10-kΩ resistor)	
TP8	DPWM-1B		
TP9	TMS	JTAG test mode select (pull-up to 3.3 V with 10-kΩ resister)	
TP10	DPWM-3A		
TP11	TDI/Sync_In	JTAG test data in (multiplexed with Sync_In for synchronizing switching frequency across multiple devices) – Pull-up to 3.3 V with 10-kΩ resistor	
TP12	TDO/Sync_Out	JTAG test data out (multiplexed with Sync_Out for synchronizing switching frequency across multiple devices)	
TP13	TCK	JTAG test clock	
TP14	SRE-1B	Synchronous rectifier enable output 1B	
TP15	SRE-3A	Synchronous rectifier enable output 3A	
TP16	FLT-1B	External fault input 1B	
TP17	FLT-3A	External fault input 3A	
TP18	CS-3A	Power stage 3A current sense input and input to analog comparator 4	



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6 Software Setup

Accessing the UCD9224EVM-464's configuration, control and monitoring capabilities with the Fusion Digital Power Designer software tool requires a one-time software setup per host system.

6.1 Fusion Digital Power Designer Software (Fusion GUI) Installation

Place the Fusion Digital Power Designer Software (Fusion GUI) Installer zip file (UCD9224EVM-464 Software Files) in a known location on the host computer to be used for EVM configuration/test. Unzip the installation files for the Fusion Digital Power Designer Software by double clicking the zip file.

Double click the unzipped TI-Fusion-Digital-Power-Designer-1.8.6.exe file and proceed through the installation by accepting the installer prompts and the license agreement. Use the Fusion GUI installer's suggested default installation locations to complete the install.

When the Fusion GUI installation reaches the finished window, uncheck the launch application check box and close the window.

7 Test Procedure

The UCD9224EVM-464 is provided with a default configuration that will allow the user to immediately power up the EVM and begin testing as either a stand-alone power solution or as a "networked" power system when accessing the PMBus[™] interface.

7.1 Test Setup

- 1. Set the external input power supply's output voltage to 12 V +/-0.5 V and current limit the supply at 5.0 A. Ensure the output voltage is disabled.
- 2. Attach supply connection leads (AWG 20 minimum) between the external power supply and the input voltage connector (J1) on the EVM following the polarity settings shown in the Recommended Test Setup (Figure 4).
- 3. Set both Electronic Load A and B to constant current loading and adjust their loading currents to 10.0 A +/- 0.1 A each.
- 4. Attach leads (AWG 16 minimum) between the Electronic Load A inputs and the target EVM's V_{OUT1} (J6) connector following the polarity settings shown in the Recommended Test Setup (Figure 4).
- 5. Attach leads (AWG 16 minimum) between the Electronic Load B inputs and the target EVM's V_{OUT2} (J5) connector following the polarity settings shown in the Recommended Test Setup (Figure 4).
- 6. Ensure that both electronic loads have their loads enabled.



Test Procedure www.ti.com

7.2 Output Voltage

- 1. Attach the DMMs to both output voltage test points, +V_{OUT1} to PGND and +V_{OUT2} to PGND.
- 2. Enable the external input voltage supply.
- 3. Measure V_{OUT1} and V_{OUT2} Output Voltages.

7.3 V_{IN} UVLO Settings and OVP Setpoint

- 1. Remove the DMM from V_{OUT2} and connect to the input voltage test points, V_{IN} and PGND.
- 2. Slowly reduce the external input voltage supply until V_{OUT1} is disabled then confirm V_{IN} voltage level.
- 3. Slowly increase the external input voltage supply until V_{OUT1} is enabled and confirm V_{IN} voltage level.
- 4. Slowly increase the external input voltage supply until V_{OUT1} is disabled and confirm V_{IN} voltage level.
- 5. Return the input supply to 12.0 V, confirm operation is still disabled.
- 6. Disable the external input voltage source.

7.4 Turn-On Timing / Power Good

Testing the currently configured settings for Turn-On Timing and Power Good

- 1. Attach Channel 1 of the oscilloscope between V_{OUT1} and PGND test points and Channel 2 between V_{OUT2} and PGND test points.
- 2. Set the oscilloscope to 1.0 V/div. vertical scale on both channels and set the time scale to 1 ms/div. Set the Trigger source to Channel 1 with a single-shot acquisition.
- 3. Remove DMM from V_{IN} and connect between the PGOOD (J2-2) and AGND (J2-3).
- 4. Enable the external input power supply.
- 5. Review captured waveform and active high PGOOD signal.

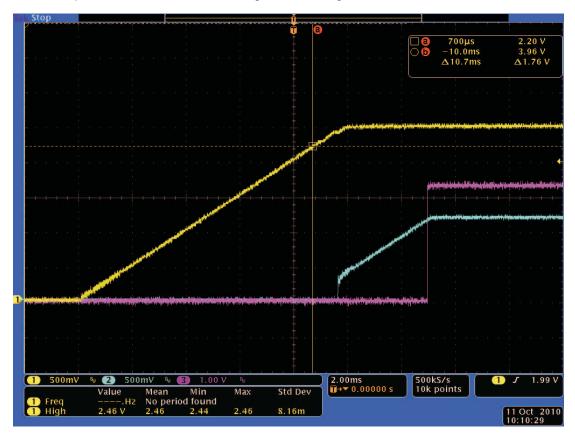


Figure 5. V_{OUT1} (Yellow), V_{OUT2} (Blue) and PGOOD (Red) Start-Up Timing



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7.5 Fusion GUI Monitoring and Control Example

 Attach the USB Interface Adapter to the computer hosting the Fusion GUI software with the supplied USB A-to-MiniB cable then to the UCD9224 with the supplied 10-pin ribbon cable. The USB Interface Adapter will be recognized as an HID device by the host system with no additional drivers needed. The green LED will illuminate when the adapter has been connected with the system.

2. With the UCD9224EVM-464 still powered, launch the Fusion GUI by double clicking the desktop icon or, alternately, navigating to the application icon in the program folder through the Windows Start Menu (default location: Start\All Programs\Texas Instruments Fusion Digital Power Designer\Fusion Digital Power Designer).

NOTE: The Offline Mode version of the GUI is for project file development only and will not be able to access an operating power system.

3. The GUI will scan the bus for available devices and after this discovery process is successful the GUI will open to its main Configuration Page (Figure 6). Navigation through the GUI is controlled with the Page and Tab selections which are highlighted in red.

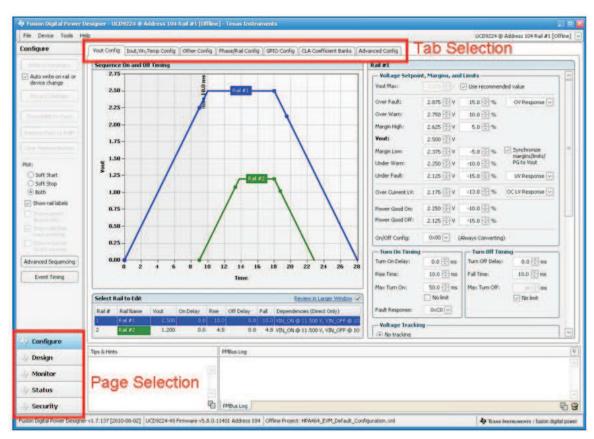


Figure 6. Default Fusion Digital Power Designer GUI Start Page



Test Procedure www.ti.com

4. Select the Monitor Page and the window in Figure 7 will be displayed. The operating status of the output voltage and other parameters for Rail #1 can be reviewed from this window, by default Rail #1 is always presented at the Fusion GUI startup. Rail #2 can be monitored by using the dropdown selection in the upper right corner of the monitoring window and selecting UCD9224 @ Address xxx Rail #2. The red horizontal lines that are present in most of the plots indicate the fault limits for this parameter and the yellow lines are the warning levels.

In the V_{OUT} Rail #1 plot shown in Figure 7, the voltage can be seen to shift down slightly and then up slightly when referenced to the earlier section of the plot. This reflects the application of margining to the output voltage with the Margin High setting still visible at the bottom of the column just to the left of the plots.



Figure 7. Fusion Digital Power Designer Software – Monitor Page – Rail #1

NOTE: A Low V_{IN} alert may be present when monitoring is first accessed but it does not affect the operation of the system. This is a typical alert condition during initial voltage application, as V_{IN} ramps above the voltage necessary to power the UCD9224 but has not reached the Turn Controller On threshold before the first V_{IN} sample is taken by the controller. This contrasts to a V_{IN} Under Voltage Warning which occurs when the unit is operating and the input voltage falls below the V_{IN} UV Warning level.



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5. There are configuration value boxes in many of the plot windows, ex. OT Fault and OT Warn boxes exist within the Temp Rail #1 plot. These are the numerical values for the fault and warning limits and reflect the same values found on the Configuration page of the GUI.

Change the OT Warn level from the pre-configured 85°C to 20°C and click the Write button, observe in the Status Registers/Lines section of the Monitor page that the Temp Status has been updated from OK to OT Warn and the SMBALERT# changes from Not Asserted to Asserted.

PMBus[™] digital controllers are considered slave devices on the SMBus and as such they cannot initiate communication with the system controller directly, but instead need to ask for assistance by activating the SMBus Alert line, SMBALERT#. If the SMB Alert line is pulled low then the system controller, the Fusion GUI for this example, will send an inquiry across the PMBus[™] to determine which controller requires assistance and why. Once the system controller has determined the issue (and possibly initiated a response), then the faults can be cleared. Return the OT Warn level to 85°C and click the Clear Faults button.

Now change the OT Fault level to 20°C and click the Write button, observe that several items changed state within the Status Registers/Lines section. The Temp Status and Logged Faults both indicate OT Fault, Misc Status indicates POWER_GOOD#, and the SMBALERT# is Asserted again. POWER_GOOD# is an indication that one or both rails have violated either the Power_Good_ON or _OFF thresholds in the configuration. In this case, it is the Power_Good_Off threshold because the configured response for an OT Fault on Rail#1 had been set to Shut Down Immediately.

Warnings and faults are stored in RAM and will be cleared when power to the controller is cycled or the Clear Faults button is exercised. Logged faults are stored in Flash and they are persistent after a power cycle. Logged faults can be cleared with the Clear Logged Faults button.

Power cycle the UCD9224 EVM and the configuration will be returned to the original state before the above changes were implemented.



Test Procedure www.ti.com

7.6 Restoring the UCD9224 EVM's Original Configuration

The file HPA464_EVM_Default_Configuration.XML can be found on the TI website and is provided to allow the user to return the EVM to its originally configured state. Simply open the Fusion GUI while the powered EVM is connected to the computer with the USB Interface Adapter. At the default Configuration Screen select File → Import Project from the dropdown menu at the top of the window and the Select Project File window will open. Click the Select File button and navigate to the location of and highlight the HPA464_EVM_Default_Configuration.xml file and click the Open button. Click the Next > button and the Select Project Items to Import window will open, set the check boxes as shown in Figure 8 and click the Next > button. In the Review Parameters to Import window, click the Select All button and then click the Write Checked button. The Fusion GUI will download the default configuration settings (it may generate two warnings about NACK of SYNC_OFFSET command, this is OK, the controller NACKs this command if the value is already zero). When the download is complete, click the Next > button then the OK button to complete the project file import. The Fusion GUI will perform a device reset after which the UCD9224EVM-464 should be restored to its original configuration settings.

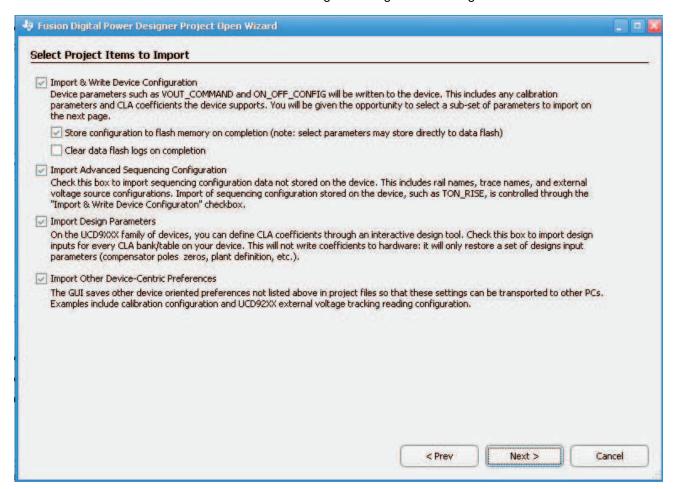


Figure 8. Configuration File Import Settings



8 Performance Data and Typical Characteristic Curves

Figure 9 through Figure 12 present typical performance curves for UCD9224EVM-464.

8.1 Efficiency

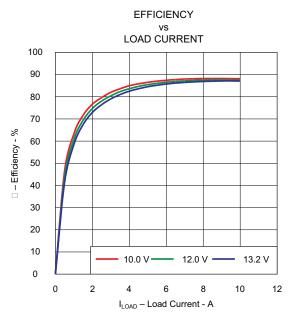


Figure 9. 2.5-V Efficiency (1.2-V no load)

8.2 Output Ripple

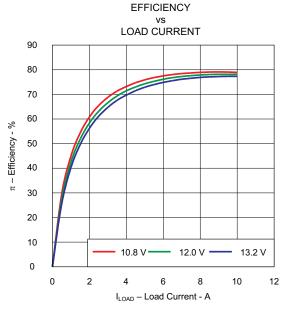


Figure 10. 1.2-V Efficiency (2.5-V no load)



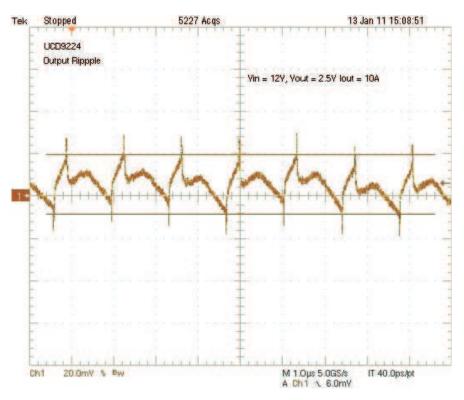


Figure 11. 2.5-V Output Ripple

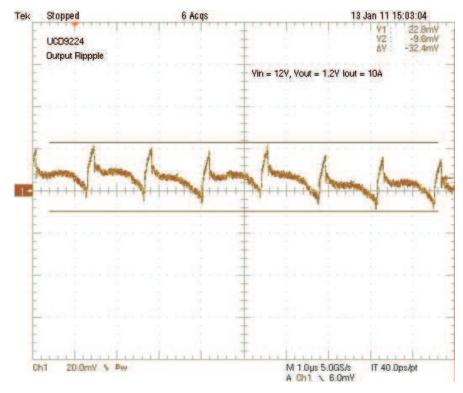


Figure 12. 1.2-V Output Ripple



9 EVM Assembly Drawing and PCB layout

The following figures (Figure 13 through Figure 17) show the design of the UCD9224EVM-464 printed circuit board.

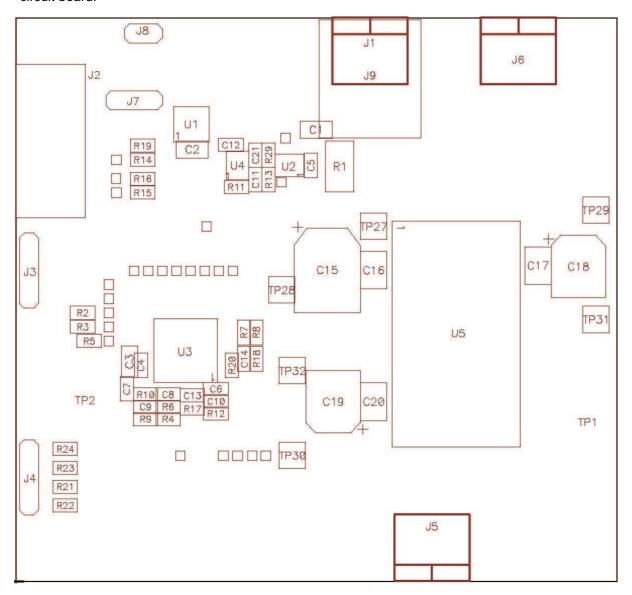


Figure 13. Top Layer Assembly Drawing (top view)



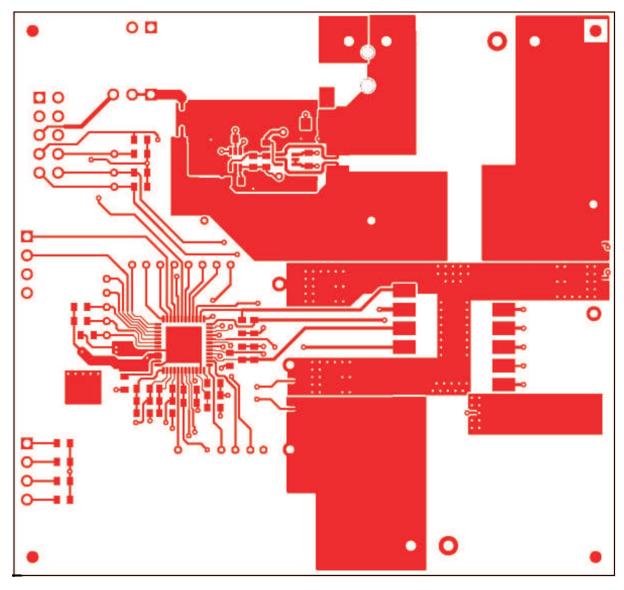


Figure 14. Top Copper (top view)



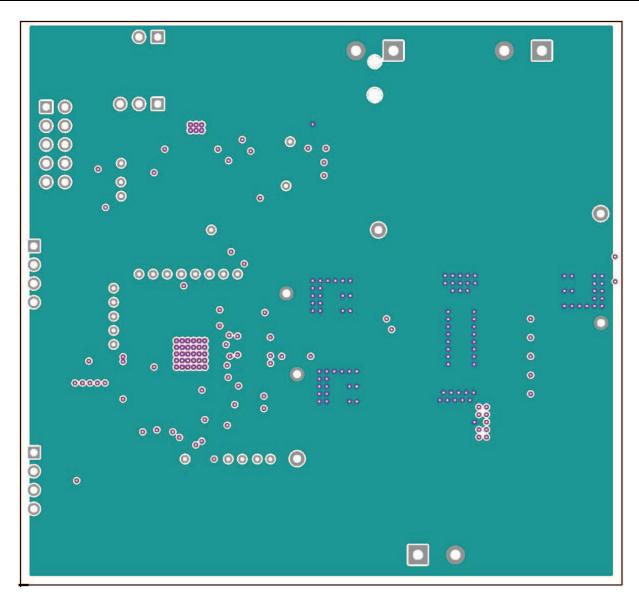


Figure 15. Internal Layer 1 (top view)



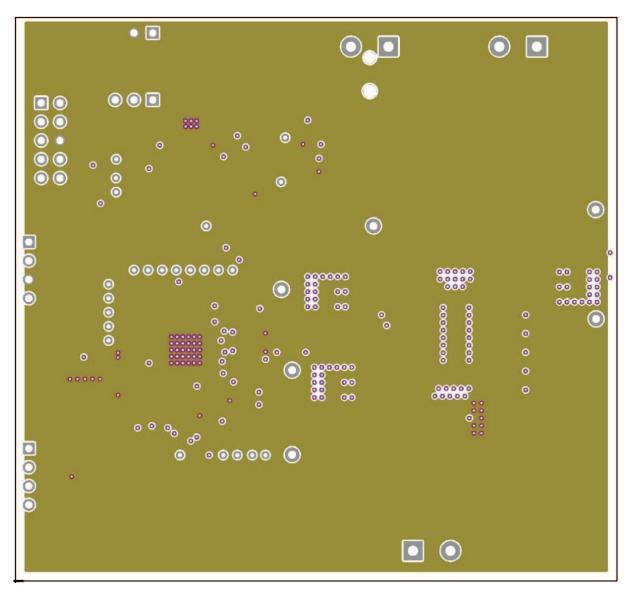


Figure 16. Internal Layer 2 (top view)



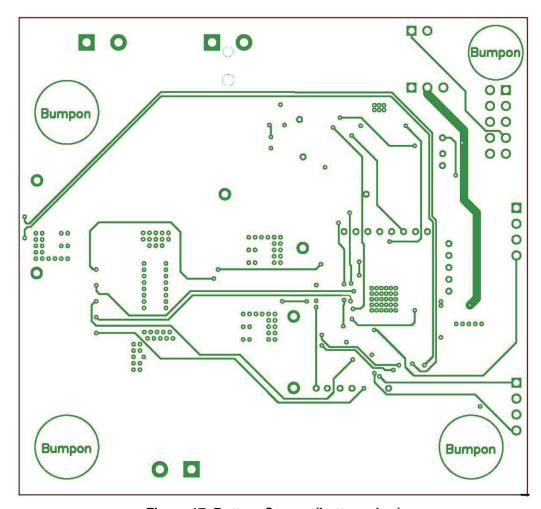


Figure 17. Bottom Copper (bottom view)



List of Materials www.ti.com

10 List of Materials

The EVM components list according to the schematic shown in Figure 2 and Figure 3.

Table 4. UCD9224EVM-464 List of Materials

QTY	REFERE NCE	DESCRIPTION	MANUFACTURER	PART NUMBER
3	C1, C2, C3	Capacitor, ceramic, 4.7 µF, 25 V, X5R, 0805	Murata Electronics (VA)	GRM21BR61E475KA1 2L
4	C10, C11, C13, C14	Capacitor, ceramic, 10000 PF, 50V, X7R, 0603	Kemet (VA)	C0603C103K5RACTU
1	C15	Capacitor, elect, 330 µF, 25 V, FK, SMD	Panasonic - ECG (VA)	EEE-FK1E331P
1	C16	Capacitor, ceramic, 22 µF, 25 V, X5R, 1210	Taiyo YUDEN (VA)	TMK325BJ226MM-T
2	C17, C20	Capacitor, ceramic, 47 µF, 16 V, X5R, 1210	Taiyo YUDEN (VA)	EMK325BJ476MM-T
2	C18, C19	Capacitor, elect, 330 µF, 6.3 V, FK, SMD	Panasonic - ECG (VA)	EEE-FK0J331XP
6	C4, C5, C6, C7, C12, C21	Capacitor, ceramic, 0.100 μF, 50V, X7R, 0603	Kemet (VA)	C0603C104K5RACTU
2	C8, C9	Capacitor, ceramic, 820 PF, 50 V, X7R, 0603	Kemet (VA)	C0603C821K5RACTU
3	J1, J5, J6	Terminal block, 5.08 MM, vertical, 2 pos	On Shore Technology Inc	ED120/2DS
1	J2	Conn header, low-pro, 10 pos, gold	Assmann Electronics Inc	AWHW10G-0202-T-R
2	J3, J4	Conn, header 0.100, single, STR, 4 pos	SULLINS CONNECTOR SOLUTIONS (VA)	PEC04SAAN
1	J8	Conn, header, 0.100, single, STR, 2 pos	Sullins Connector Solutions (VA)	PEC02SAAN
1	R1	Resistor, 0 .001 Ω, 1/2 W, 1%, 2010, SMD	Vishay/Dale (VA)	WSL20101L000FEA
4	R14, R15, R16, R19	Resistor, 100 kΩ, OHM 1/10 W, 1%, 0603, SMD	Vishay/Dale (VA)	CRCW0603100KFKEA
2	R17, R18	Resistor, 20.0 kΩ, 1/10 W, 1%, 0603, SMD	Vishay/Dale (VA)	CRCW060320K0FKEA
8	R2, R3, R5, R7, R8, R11, R12, R20	Resistor, 10.0 kΩ, 1/10 W, 1%, 0603, SMD	Vishay/Dale (VA)	CRCW060310K0FKEA
2	R21, R23	Resistor, 76.8 kΩ, 1/10 W, 1%, 0603, SMD	Panasonic - ECG (VA)	ERJ-3EKF7682V
2	R22, R24	Resistor, 133 kΩ, 1/10 W, 1%, 0603, SMD	Vishay/Dale (VA)	CRCW0603133KFKEA
1	R29	Resistor, 1.00 kΩ, 1/10 W, 1%, 0603, SMD	Panasonic - ECG (VA)	ERJ-3EKF1001V
3	R4, R9, R13	Resistor, 1.50 kΩ, 1/10 W, 1%, 0603, SMD	Panasonic - ECG (VA)	ERJ-3EKF1501V
2	R6, R10	Resistor, 1.21 kΩ, 1/10 W, 1%, 0603, SMD	Vishay/Dale (VA)	CRCW06031K21FKEA
2	TP1, TP2	PC test point compact SMT	Keystone Electronics (VA)	5016
3	TP27, TP29, TP30	Test point, PC mini, 0.040", RED	Keystone Electronics	5000
3	TP28, TP31, TP32	Test point, PC mini, 0.040", BLACK	Keystone Electronics	5001
1	U1	3.3-V hi-in, LDO reg, 8-SON	Texas Instruments (VA)	TPS715A33DRBT
1	U2	Current monitor, 1%, SC70-6	Texas Instruments (VA)	INA210AIDCKT
1	U3	DGTL PWM system, CTRLR, 48 V, QFN	Texas Instruments (VA)	UCD9224RGZT
1	U4	Switch SPDT SC70-6	Texas Instruments (VA)	SN74LVC1G3157DCK R
1	U5	Module DGTL Powertrain, 10 A, 22 dip	Texas Instruments	PTD08D210WAC

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It is important to operate this EVM within the input voltage range of 4.75 V to 12 V and the output voltage range of 0.7 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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