User's Guide

SLUU416A–May 2010–Revised September 2010

CSD86350Q5DEVM-604

The CSD86350Q5DEVM-604 evaluation module (EVM) is a synchronous buck converter featuring TI's NexFET™ Power Block technology to provide a high current, ultra-high density power supply solution. The EVM provides a 1.2V output at 25A from a 12V nominal input bus at over 92% efficiency. The EVM is designed to operate from a single supply, so no additional bias voltage is required. The EVM uses the TPS51218 high performance, mid-input voltage, synchronous buck controller and TI's NexFET™ Power Block to optimize the efficiency and power density of the total solution.

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1 Description

The CSD86350Q5DEVM-604 is designed to use a regulated 12V (8V – 13V) bus voltage to provide a regulated 1.2V output at up to 25A of load current. The CSD86350Q5DEVM-604 is designed to demonstrate the CSD86350Q5D NexFET™ Power Block in a typical 12V bus to low-voltage application, while providing a number of non-invasive test points to evaluate the performance of the CSD86350Q5D NexFET™ Power Block in a given application.

1.1 Applications

- Synchronous Buck Converters
  - High Frequency Applications
  - High Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters

1.2 Features

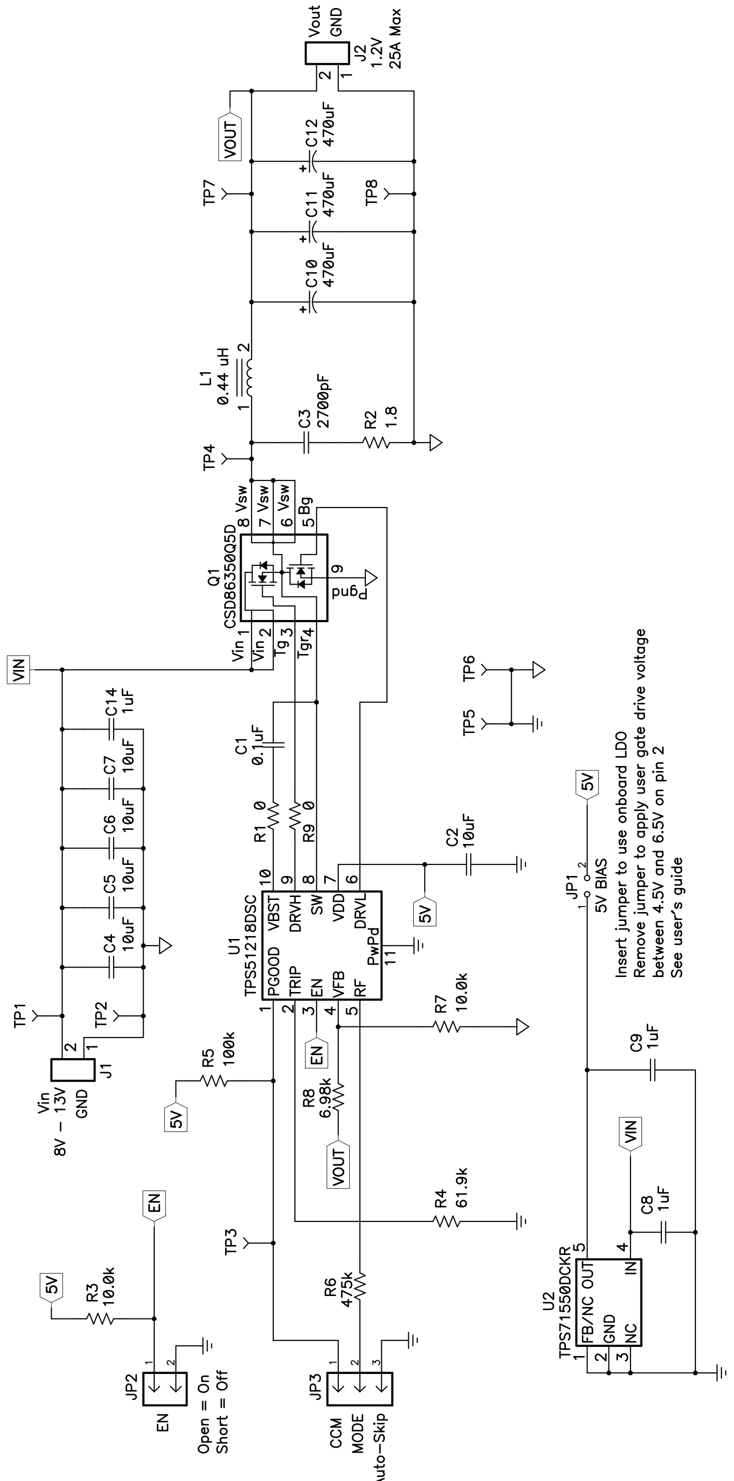
- 8V to 13V input voltage rating
- 1.2V output voltage
- 25A steady state load current
- 290 kHz switching frequency
- Simple access to IC features including enable, power good, and switching node
- Convenient test points for simple, non-invasive measurements of converter performance including input ripple, output ripple, and switching node

2 CSD86350Q5DEVM-604 Electrical Performance Specifications

Table 1. CSD86350Q5DEVM-604 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IN}	Input voltage		8	12	13	V
I_{IN}	Input current	V_{IN} = 12V, I_{OUT} = 25A	-	2.8	-	A
	No load input current	V_{IN} = 12V, I_{OUT} = 0A, MODE = GND	-	0.35	-	mA
V_{bias}	External bias voltage	JP1 open, Bias applied on pin 2 of JP1	4.5	5.0	6.5	V
I_{bias}	External bias current	JP1 open, Bias applied on pin 2 of JP1	15			mA
Output Characteristics						
V_{OUT}	Output voltage	V_{IN} = 12V, I_{OUT} = 25A	1.18	1.2	1.22	V
V_{OUT_ripple}	Output voltage ripple	V_{IN} = 12V, I_{OUT} = 25A, measured across output capacitor C12	-	16	-	mV_{p-p}
I_{OUT}	Output current	V_{IN} = 8V to 13V	0		25	A
System Characteristics						
F_{SW}	Switching frequency		266	290	314	kHz
η_{pk}	Peak efficiency	V_{IN} = 12V	-	92.6	-	%
η	Full load efficiency	V_{IN} = 12V, I_{OUT} = 25A	-	90.0	-	%

3 CSD86350Q5DEVM-604 Schematic



For reference only. See Section 9 for specific values.

Figure 1. CSD86350Q5DEVM-604 Schematic

4 Connector, Jumper, and Test Point Descriptions

4.1 Input Power (J1)

12V input power connection to the CSD86350Q5DEVM-604. Connect the positive voltage to pin 2 and the return connection to pin 1. See Section 5.1.5 for the appropriate sizing of the wire.

4.2 Output Power (J2)

1.2V output power connection from the CSD86350Q5DEVM-604. Connect the positive LOAD connection to pin 2 and the return LOAD connection to pin 1. See Section 5.1.5 for the appropriate sizing of the wire.

4.3 5V Bias Jumper (JP1)

The CSD86350Q5DEVM-604 contains an onboard 5V bias regulator (a TPS71550 linear regulator) to power the TPS51218 controller. This allows the EVM to run off of a single 12V input source. Insert the shunt in JP1 to use the onboard regulator. Removing the shunt allows the user to apply a different bias voltage to the EVM on pin 2 of JP1. This external bias voltage should be between 4.5V and 6.5V and be able to supply 15 mA to properly power the TPS51218. The ground reference of this external source should be TP5.

4.4 Disable Jumper (JP2)

The CSD86350Q5DEVM-604 contains a disable jumper header (JP2). Installing the shunt in JP2 shuts down the TPS51218 and disables the power supply. Removing the shunt allows the EN pin on the TPS51218 to be pulled up to 5V and enables the TPS51218.

4.5 MODE Jumper (JP3)

The CSD86350Q5DEVM-604 contains a MODE jumper to select the mode of operation of the TPS51218. Installing the shunt in the 'Auto-Skip' position in JP3 (between pins 2 and 3) connects the RF pin to GND through R6 to increase efficiency at light loads. Installing the shunt in the 'CCM' position in JP3 (between pins 1 and 2) connects the RF pin to PGOOD through R6 in order to maintain a constant switching frequency over the entire load range.

4.6 Test Point Descriptions

Table 2. Test Point Description

Test Point	Label	Use	Section
TP1	VIN	Measurement test point for input voltage	Section 4.6.1
TP2	PGND	Measurement test point for input voltage return	Section 4.6.1
TP3	PGOOD	Measurement test point for power good	Section 4.6.4
TP4	SW	Measurement test point for switch node voltage	Section 4.6.3
TP5	AGND	Reference test point for PGOOD and return connection for an external bias voltage applied to pin 2 of JP1	Section 4.6.4
TP6	PGND	Measurement test point for switch node voltage return	Section 4.6.3
TP7	VOUT	Measurement test point for output voltage	Section 4.6.2
TP8	PGND	Measurement test point for output voltage return	Section 4.6.2

4.6.1 Input Voltage Monitoring (TP1 and TP2)

The CSD86350Q5DEVM-604 provides two test points for measuring the input voltage applied to the module. This allows the user to measure the actual input voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive input to TP1 and negative input to TP2. Tip and barrel measurement technique can be used on TP1 and TP2 to measure the input ripple of the EVM. See Figure 3.

4.6.2 Output Voltage Monitoring (TP7 and TP8)

The CSD86350Q5DEVM-604 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual output voltage without losses from output cables and connectors. All output voltage measurements should be made between TP7 and TP8. To use TP7 and TP8, connect a voltmeter positive input to TP7 and negative input to TP8. Tip and barrel measurement technique should not be used on TP7 and TP8 to measure the output ripple of the EVM, as the probe can pick up substantial radiated noise. It is recommended to measure the output voltage ripple as described in Section 5.4.

4.6.3 Switching Node Monitoring (TP4 and TP6)

The CSD86350Q5DEVM-604 provides two test points for measuring the switching node of the module power stage. Tip and barrel measurement technique should be used on TP4 and TP6 to measure the switching node waveform. See Figure 3.

4.6.4 Power Good Voltage Monitoring (TP3 and TP5)

The CSD86350Q5DEVM-604 provides a test point, TP3, and a local ground, TP5, for measuring the power good output voltage. A 100-kΩ resistor pull-up to 5V (R5) is included on the EVM to allow the Power Good signal to be monitored without requiring an external pull-up. TP5 is the ground reference for the power good test point.

TP5 also functions as the return connection for an external bias voltage source that may be supplied to pin 2 of JP1.

5 Test Set Up

5.1 Equipment

5.1.1 Voltage Source

V_{IN} — The input voltage source (V_{IN}) should be a 0V – 15V variable DC source capable of supplying 5A

5.1.2 Meters

A1 — Input current meter. 0A – 5A ammeter

V1 — Input voltage meter. 0V – 15V voltmeter

V2 — Output voltage meter. 0V – 2V voltmeter

5.1.3 Load

LOAD — Output load. Electronic load set for constant current or constant resistance capable of 0A – 25A at 1.2V

5.1.4 Oscilloscope

For Output Voltage Ripple — Oscilloscope should be an analog or digital oscilloscope set for AC coupled measurement with 20 MHz bandwidth limiting. Use 20mV/division vertical resolution and 1µs/division horizontal resolution.

For Switch Node Waveform — Oscilloscope should be an analog or digital oscilloscope set for DC coupled measurement with 20 MHz bandwidth limiting. Use 2V/division or 5V/division vertical resolution and 1µs/division horizontal resolution.

5.1.5 Recommended Wire Gauge

V_{IN} to J1 — The connection between the source voltage (V_{IN}) and J1 of the CSD86350Q5DEVM-604 can carry as much as 5A of current. The minimum recommended wire size is AWG #16 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

J2 to LOAD: — The connection between J2 and the LOAD of the CSD86350Q5DEVM-604 can carry as much as 25A of current. The minimum recommended wire size is AWG #12 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

5.1.6 Other

FAN — The CSD86350Q5DEVM-604 evaluation module includes components that can get hot to the touch when operating. Because this evaluation module is not enclosed to allow probing of circuit nodes, a small fan capable of 200lfm – 400lfm is recommended to reduce component temperatures when operating.

5.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the CSD86350Q5DEVM-604. Note that although the return for J1 and J2 are the same ground, the connections should remain separate as shown in Figure 2.

5.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 5A maximum. Make sure V_{IN} is initially set to 0V and connected as shown in Figure 2.
3. Connect V_{IN} to J1 as shown in Figure 2.
4. Connect ammeter A1 between V_{IN} and J1 as shown in Figure 2.
5. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
6. Connect voltmeter V2 to TP7 and TP8 as shown in Figure 2.
7. Connect oscilloscope probes to desired test points per Table 2.
8. Place fan as shown in Figure 2 and turn on making sure to blow air directly across the evaluation module.

5.2.2 Test Setup Diagram

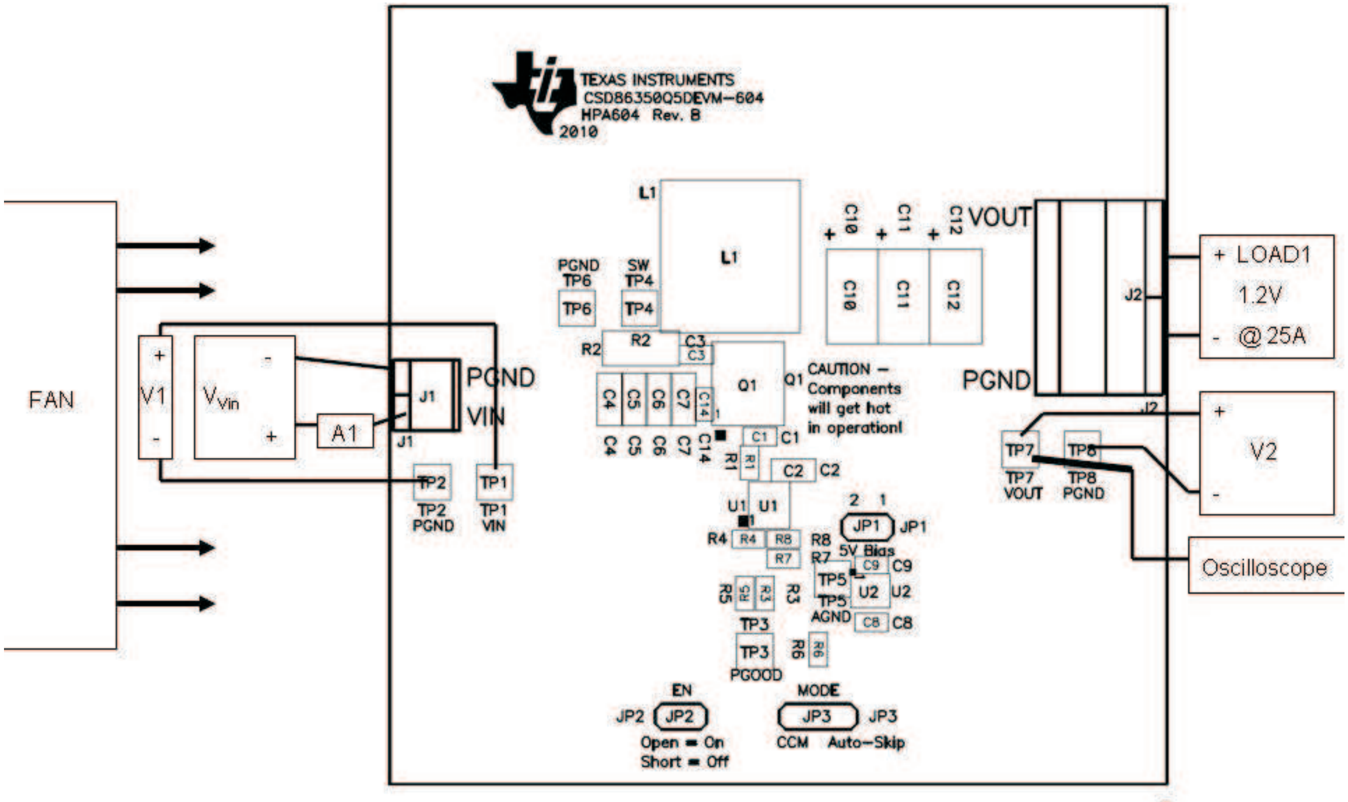


Figure 2. CSD86350Q5DEVM-604 Recommended Test Set-Up

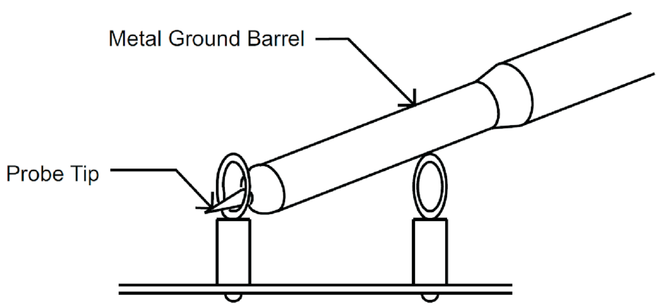


Figure 3. Tip and Barrel Technique

5.3 *Start Up/Shut Down Procedure*

1. Install shunt in JP1
2. Remove shunt from JP2, if present
3. Verify shunt position of JP3 for desired operating MODE per Section 4.5
4. Increase V_{IN} from 0V to 12V
5. Turn on FAN
6. Vary LOAD from 0A to 25A
7. Vary V_{IN} from 8V to 13V
8. Decrease LOAD to 0A
9. Decrease V_{IN} to 0V

5.4 Output Ripple Voltage Measurement Procedure

1. Solder a bus wire onto the ground of output capacitor C12
2. Follow Section 5.3 (Start Up / Shut Down Procedure) steps 1 – 7 to set V_{IN} and LOAD to the desired operating condition
3. Set oscilloscope for output voltage ripple measurement as described in Section 5.1.4
4. Measure output voltage ripple across C12 using the soldered bus wire wrapped around the exposed oscilloscope probe ground barrel
5. Follow Section 5.3 (Start Up / Shut Down Procedure) steps 8 and 9 to power down

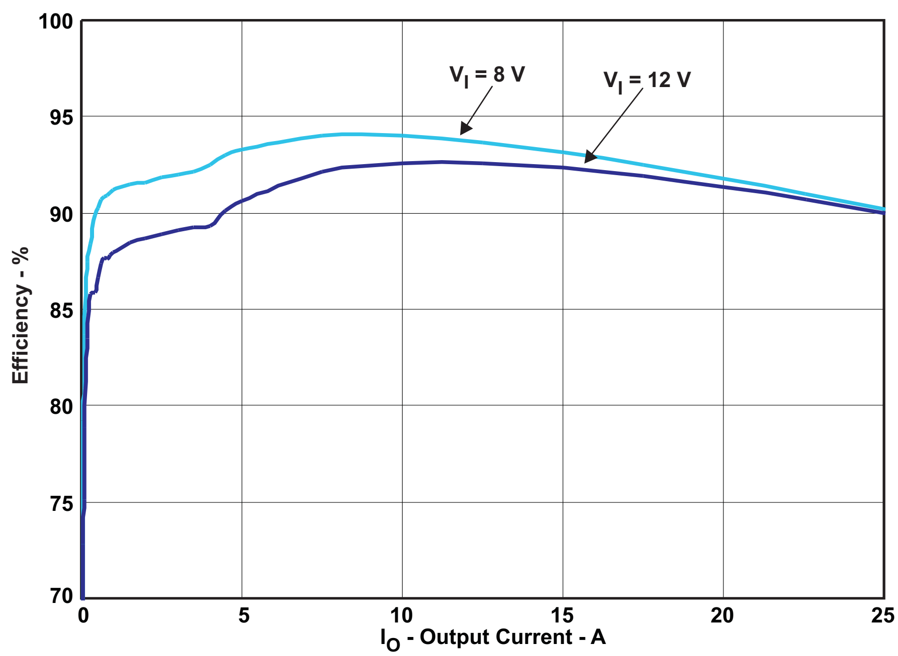
5.5 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down LOAD
3. Shut down V_{IN}
4. Shut down FAN

6 CSD86350Q5DEVM-604 Test Data

Figure 4 through Figure 12 present typical performance curves for the CSD86350Q5DEVM-604. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

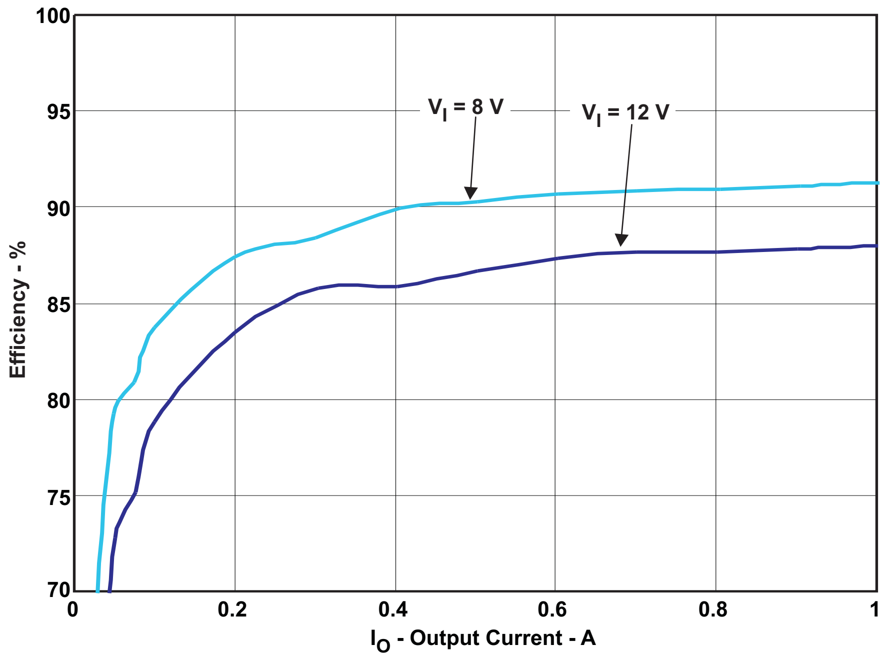
6.1 Efficiency



V_{IN} = 8V & 12V, V_{OUT} = 1.2V, MODE = GND, no airflow

Figure 4. CSD86350Q5DEVM-604 Efficiency vs Load Current

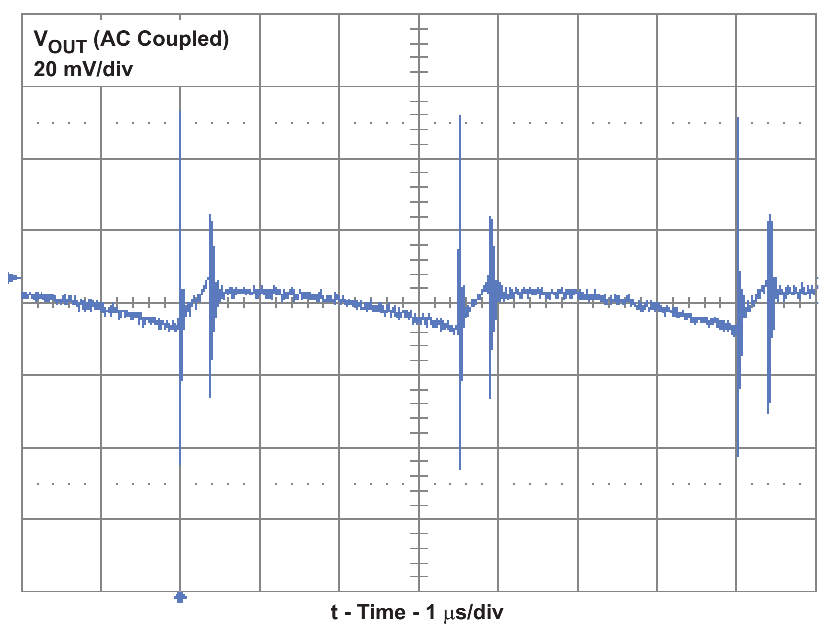
6.2 *Efficiency (Low Load)*



V_{IN} = 8V & 12V, V_{OUT} = 1.2V, MODE = GND, no airflow

Figure 5. CSD86350Q5DEVM-604 Low Load Efficiency vs Load Current

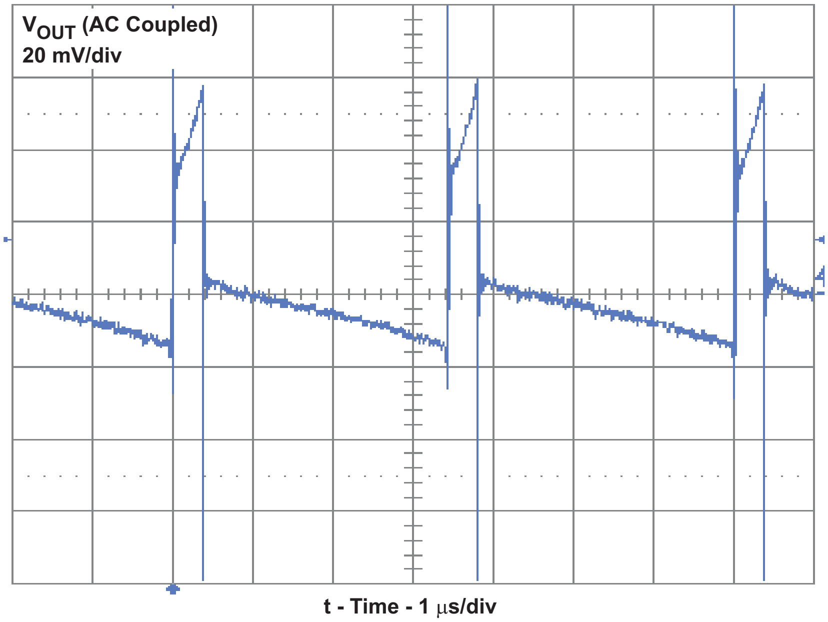
6.3 *Output Voltage Ripple*



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A, measured across output capacitor C12 using a bus wire wrapped around exposed oscilloscope probe ground barrel

Figure 6. CSD86350Q5DEVM-604 Output Voltage Ripple

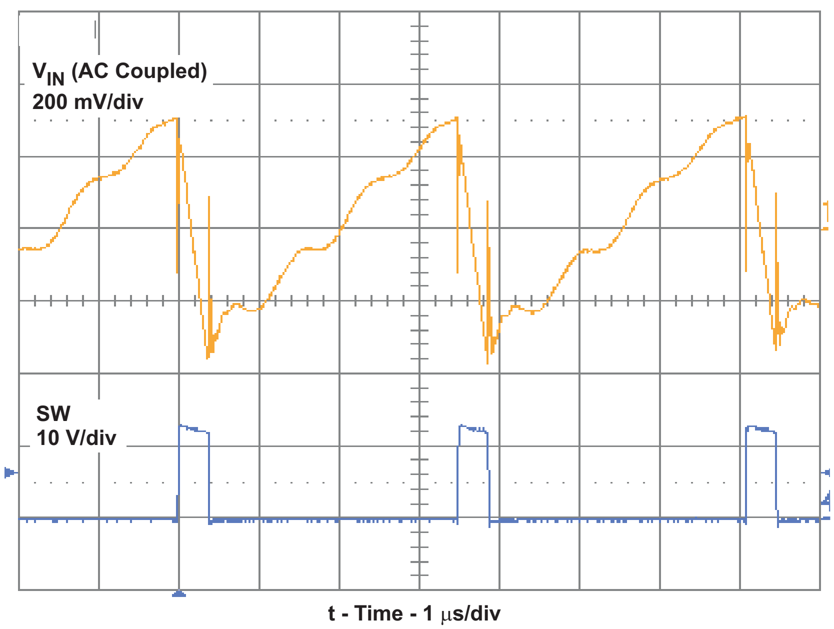
6.4 Output Voltage Ripple



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A, measured at TP7 and TP8 using the tip and barrel measurement technique shown in Figure 3. Since the probe picks up substantial radiated noise, this method is not recommended to measure the output voltage ripple.

Figure 7. CSD86350Q5DEVM-604 Output Voltage Ripple

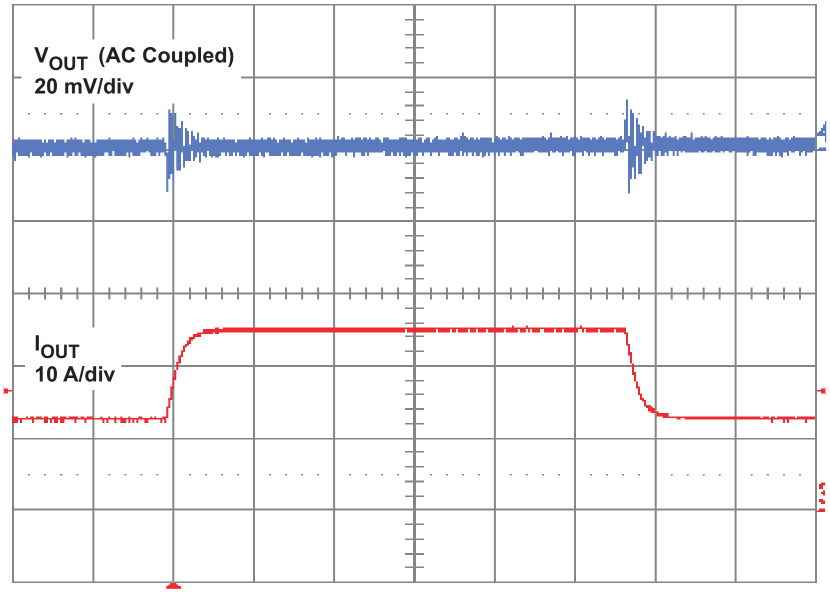
6.5 Input Voltage Ripple



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A

Figure 8. CSD86350Q5DEVM-604 Input Voltage Ripple

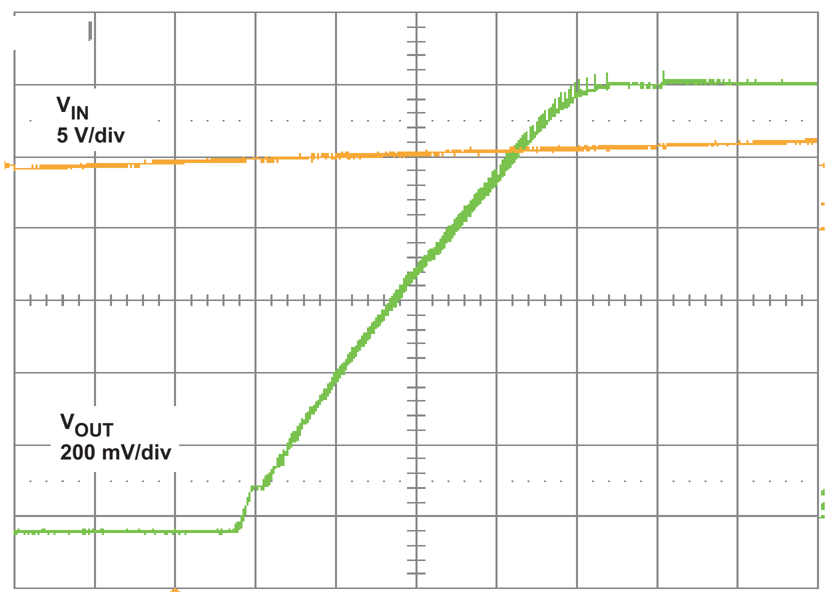
6.6 Load Transient Response



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12.5A to 25A, measured across output capacitor C12 using a bus wire wrapped around exposed oscilloscope probe ground barrel

Figure 9. CSD86350Q5DEVM-604 Step Response

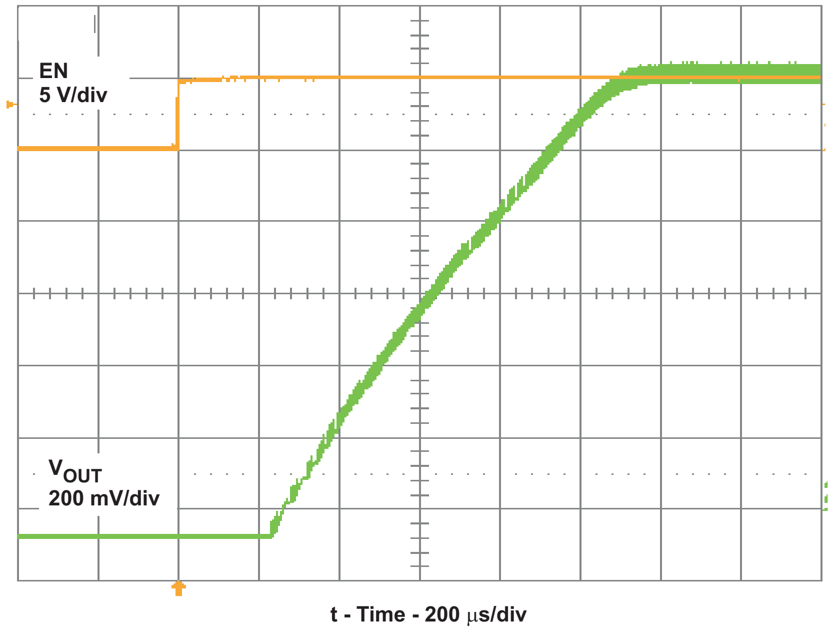
6.7 Start Up on V_{IN}



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A

Figure 10. CSD86350Q5DEVM-604 Start-Up on V_{IN}

6.8 Start Up on EN



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A

Figure 11. CSD86350Q5DEVM-604 Start-Up on EN

6.9 Thermal Image

V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A, no air flow

Figure 12. CSD86350Q5DEVM-604 Thermal Image

7 CSD86350Q5DEVM-604 Modifications

Several modifications can be made to the CSD86350Q5DEVM-604. Making any of these changes will change the EVM's performance data and may require a modification to the inductor value or current limit trip point (R4 value). The design may also change thermally. Consult the TPS51218 datasheet for details on how to pick R4.

7.1 Switching Frequency

The switching frequency of the CSD86350Q5DEVM-604 may be changed by changing the value of R6, per Table 3:

Table 3. R6 and Switching Frequency

R6 Value (kΩ)	Switching Frequency (f_{sw}) (kHz)
470	290
200	340
100	380
39	430

7.2 Output Voltage

The output voltage of the CSD86350Q5DEVM-604 may be changed by changing the value of R8, per Equation 1. $I_{Lripple}$ is found from Equation 2.

CAUTION

The output voltage should not be set higher than 1.9V or else damage may occur to the EVM.

$$R8 = \frac{\frac{V_{OUT} - (I_{Lripple} \times 2m\Omega)}{2} - 0.7}{0.7} \times R7 \qquad (1)$$

$$I_{Lripple} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f_{sw} \times V_{IN}} \qquad (2)$$

7.3 Gate Drive Resistors

The gate drive to the high side MOSFET may be slowed by increasing the value of resistors R1 and/or R9. This will slow down the turn on of the high side MOSFET and result in less ringing on the SW node. This will also result in slightly lower efficiency and higher operating temperatures.

8 CSD86350Q5DEVM-604 Assembly Drawings and Layout

The following figures (Figure 13 through Figure 16) show the design of the CSD86350Q5DEVM-604 printed circuit board. The EVM has been designed using a 4-layer, 2oz. copper circuit board measuring 3" × 3" with all populated components on the top to allow the user to easily view, probe and evaluate the CSD86350Q5D solution. Moving components to both sides of the PCB can offer additional size reduction for space constrained systems.

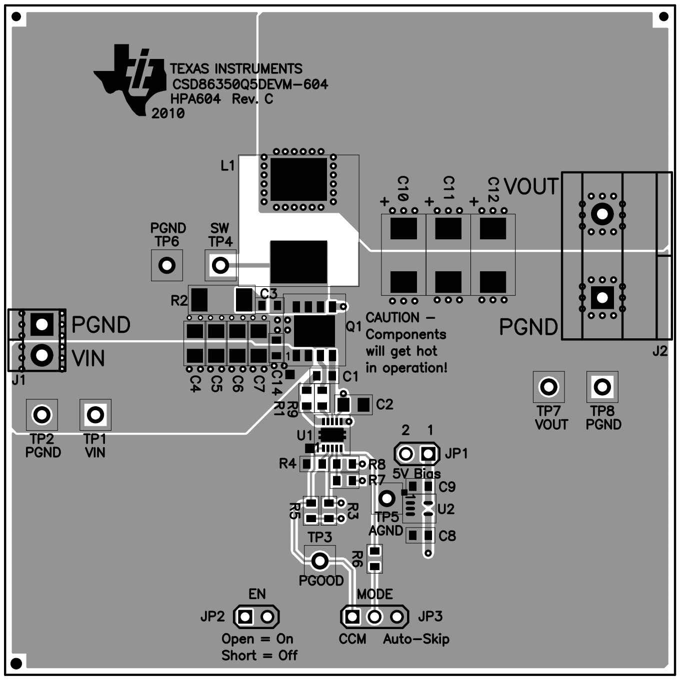


Figure 13. CSD86350Q5DEVM-604 Top Component Placement (Top View)

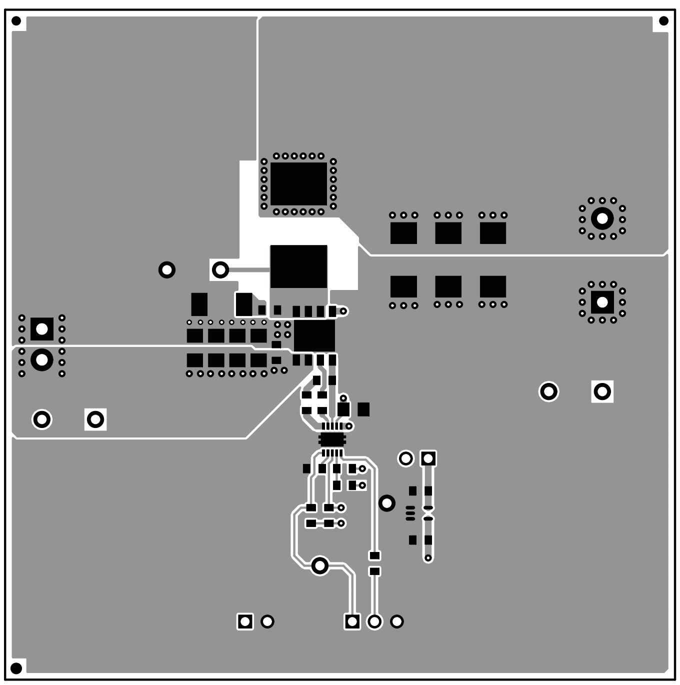


Figure 14. CSD86350Q5DEVM-604 Top Copper (Top View)

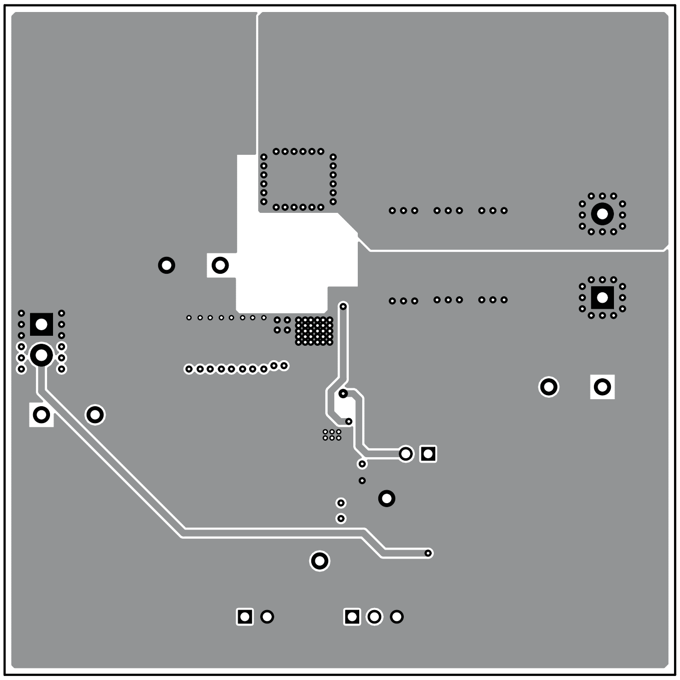


Figure 15. CSD86350Q5DEVM-604 Internal Copper Layer 1 (X-Ray Top View)

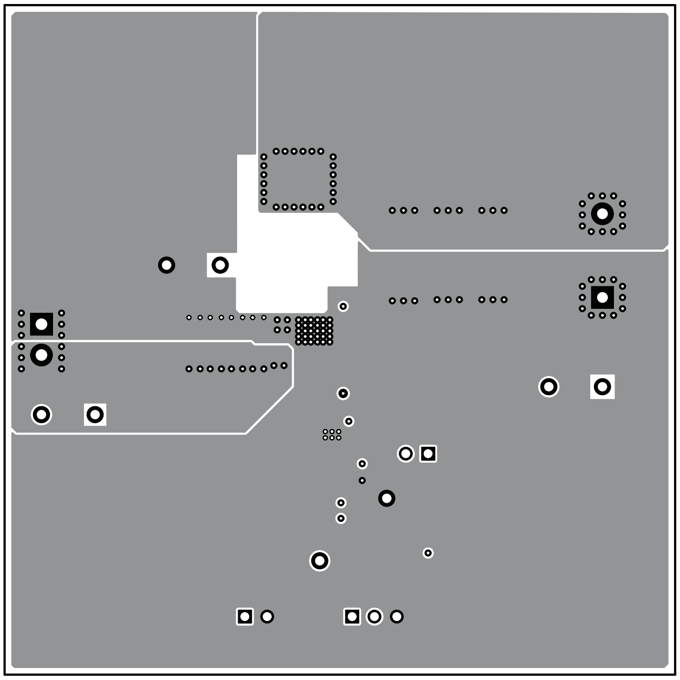


Figure 16. CSD86350Q5DEVM-604 Internal Copper Layer 2 (X-Ray Top View)

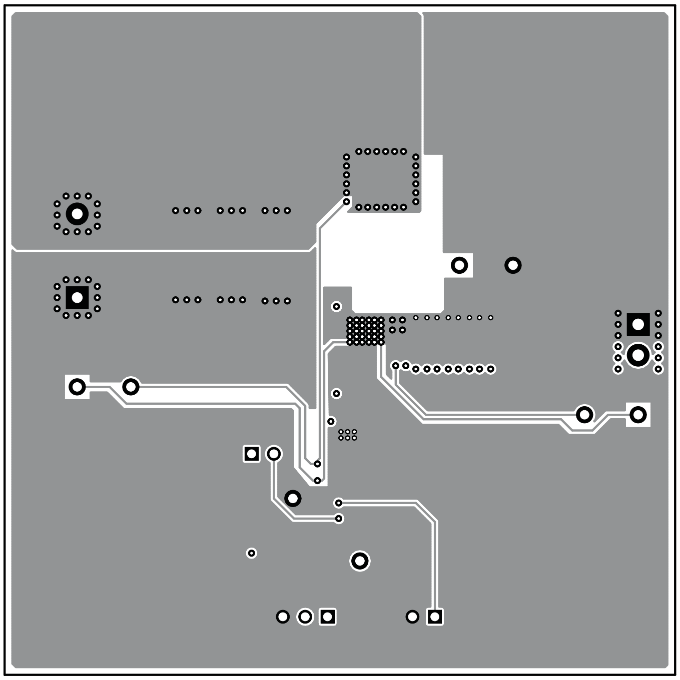


Figure 17. CSD86350Q5DEVM-604 Bottom Copper (Bottom View)

9 CSD86350Q5DEVM-604 Bill of Materials

Table 4. CSD86350Q5DEVM-604 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	0.1µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
3	C10, C11, C12	470µF	Capacitor, Polymer Aluminum, 2V, 20%	7343	EEFSX0D471XE	Panasonic
1	C2	10µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	Std	Std
1	C3	2700pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
4	C4, C5, C6, C7	10µF	Capacitor, Ceramic, 25V, X5R, 20%	1206	Std	Std
3	C8, C9, C14	1µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
1	L1	0.44µH	Inductor, SMT Power, 35A, ±20%	0.510 x 0.530 inch	SLC1480-441ML	Coilcraft
1	Q1	CSD86350Q5D	MOSFET, Dual N-Chan, 25V, 25A	QFN-8 POWER	CSD86350Q5D	TI
2	R1, R9	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	1.8	Resistor, Metal Film, 1/2W, 1%	2010	Std	Std
2	R3, R7	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	61.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	475k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	6.98k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS51218DSC	IC, Single Synchronous Step-Down Controller	DSC-10	TPS51218DSC	TI
1	U2	TPS71550DCKR	IC, High Input Voltage, Micropower, 3.2 µA at 50 mA LDO, 5V	SC70-5	TPS71550DCKR	TI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8V to 13V and the output voltage range of no greater than 1.9V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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