*User's Guide*

# *TPS51020 Buck Controller Evaluation Module User's Guide*

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## Trademarks

# 1 Introduction

The TPS51020 is a multi-function dual-synchronous step-down controller. The part is specifically designed for high performance, high-efficiency applications where the loss associated with a current sense resistor is unacceptable. The TPS51020 uses feedforward voltage mode control to improve the line response. Efficiency at light load conditions can be maintained high as well by incorporating auto-skip operation. The TPS51020 can be used in the following:

- Notebook computer system bus and I/O, DDR I, or DDR II termination applications
- Distributed power and point-of-load regulation for DSPs, FPGAs, ASICs, and so forth
- Servers
- Base stations
- Broadband, networking or optical communications systems

The TPS51020EVM−001 evaluation module (EVM) is a high-efficiency, dual synchronous buck converter providing 5 V at 6.0 A and 3.3 V at 6.0 A from an 8.0-V to 20-V input. The TPS51020 operates at 300 kHz with a peak efficiency of 94.8% with both channels enabled. This user's guide describes the TPS51020EVM−001 performance in dual mode.

# 2 Electrical Performance Specifications

A summary of performance specifications for the TPS51020EVM−001 is provided in Table 2-1.

## 2.1 Performance Specification Summary

**Table 2-1. Performance Specification Summary**

| SPECIFICATION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| Input voltage range, $V_{IN}$ (DC) | | 8 | 12 | 20 | V |
| Operating frequency | | | 300 | | kHz |
| Input ripple voltage (RMS value) | $V_{IN}$ = 12 V, $I_{OUT1}$ = 6 A, $I_{OUT2}$ = 6 A | | 194 | | mV |
| **CHANNEL1(VO1, GND)** | | | | | |
| Maximum output current | 8 V ≤ $V_{IN}$ ≤ 20 V | 6 | | | A |
| Output voltage | | 4.85 | 5.00 | 5.13 | V |
| Line regulation | $I_{OUT1}$ = 6 A, 8 V ≤ $V_{IN}$ ≤ 20 V | | | 0.1% | |
| Load regulation | $V_{IN}$ = 12 V, 0 A ≤ $I_{OUT1}$ ≤ 6 A | | | 0.1% | |
| Load transient response voltage change | $I_{OUT1}$ rising from 0 A to 5 A | | 30 | | $mV_{P-P}$ |
| | $I_{OUT1}$ falling from 5 A to 0 A | | 60 | | |
| Load transient response recovery time | $I_{OUT1}$ rising from 0 A to 5 A | | | 500 | ms |
| | $I_{OUT1}$ falling from 5 A to 0 A | | | 500 | |
| Loop bandwidth | $I_{OUT1}$ = 6 A, $V_{IN}$ = 12 V | | 14 | | kHz |
| Phase margin | $I_{OUT1}$ = 6 A, $V_{IN}$ = 12 V | | 32 | | |
| Output ripple voltage | $I_{OUT1}$ = 6 A, $V_{IN}$ = 12 V | | 36 | 60 | $mV_{P-P}$ |
| Output rise time | $I_{OUT1}$ = 6 A, $V_{IN}$ = 12 V, VO1 = 5 V | | 4.6 | | ms |
| Full load efficiency | $I_{OUT1}$ = 6 A, VO1 = 5 V, $I_{OUT2}$ = 0 A, $V_{IN}$ = 12 V | | 93.9% | | |
| **CHANNEL2(VO2, GND)** | | | | | |
| Maximum output current | 8 V ≤ $V_{IN}$ ≤ 20V | 6 | | | A |
| Output voltage | | 3.21 | 3.30 | 3.38 | V |
| Line regulation | $I_{OUT2}$ = 6 A, 8 V ≤ $V_{IN}$ ≤ 20 V | | | 0.1% | |
| Load regulation | $V_{IN}$ = 12 V, 0 A ≤ $I_{OUT2}$ ≤ 6 A | | | 0.2% | |
| Load transient response voltage change | $I_{OUT2}$ rising from 0 A to 5 A | | 50 | | $mV_{P-P}$ |
| | $I_{OUT2}$ falling from 5 A to 0 A | | 50 | | |
| Load transient response recovery time | $I_{OUT2}$ rising from 0 A to 5 A | | | 500 | ms |
| | $I_{OUT2}$ falling from 5 A to 0 A | | | 500 | |
| Loop bandwidth | $I_{OUT2}$ = 6 A, $V_{IN}$ = 12 V | | 15 | | kHz |

**Table 2-1. Performance Specification Summary (continued)**

| SPECIFICATION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Phase margin | $I_{OUT2}$ = 6 A, $V_{IN}$ = 12 V | | 41 | | |
| Output ripple voltage | $I_{OUT2}$ = 6 A, $V_{IN}$ = 12 V | | 34 | 60 | $mV_{P-P}$ |
| Output rise time | $I_{OUT2}$ = 6 A, $V_{IN}$ = 12 V, VO2 = 3.3 V | | 4.72 | | ms |
| Full load efficiency | $I_{OUT1}$ = 0 A, VO2 = 3.3 V, $I_{OUT2}$ = 6 A, $V_{IN}$ = 12 V | | 91.3% | | |

# 3 TPS51020EVM-001 Circuit Module Schematic

Figure 3-1 shows the TPS51020EVM−001 circuit module schematic diagram.

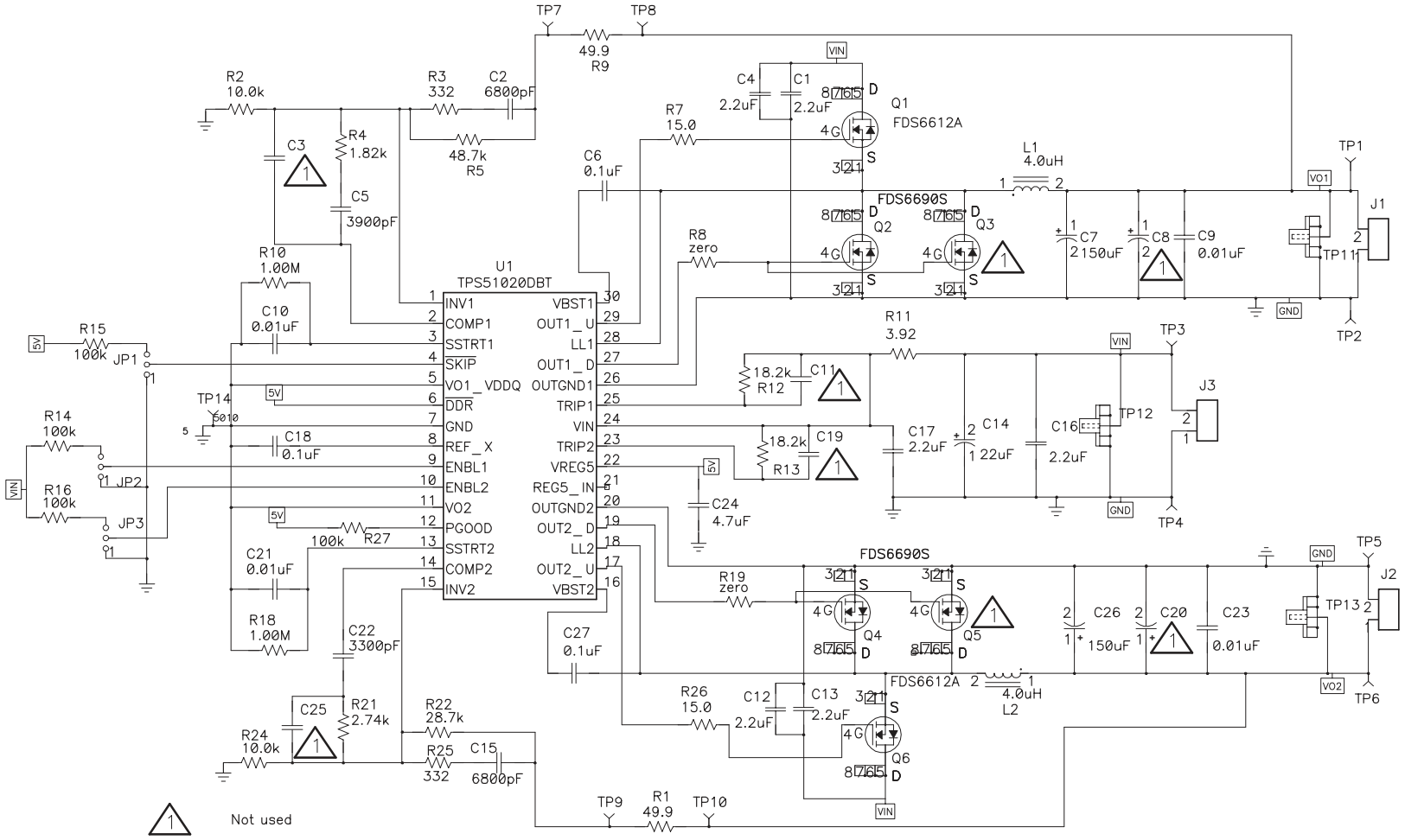


**Figure 3-1. TPS51020EVM-001 Schematic**

# 4 Test Setup and Results

## 4.1 Test Setup

The HPA064 has the following input/output connections: 12-V input through J3 (VIN and GND), 5.0-V output through J1 (VO1 and GND), and 3.3-V output through J2 (VO2 and GND). Figure 4-1 shows the connection points. A power supply capable of supplying 6 A should be connected to VIN and GND through a pair of 16 AWG wires. The 5.0-V and 3.3-V loads should be connected respectively to VO1, GND and VO2, GND2 through pairs of 16 AWG wires. Wire lengths should be minimized to reduce losses in the wires.

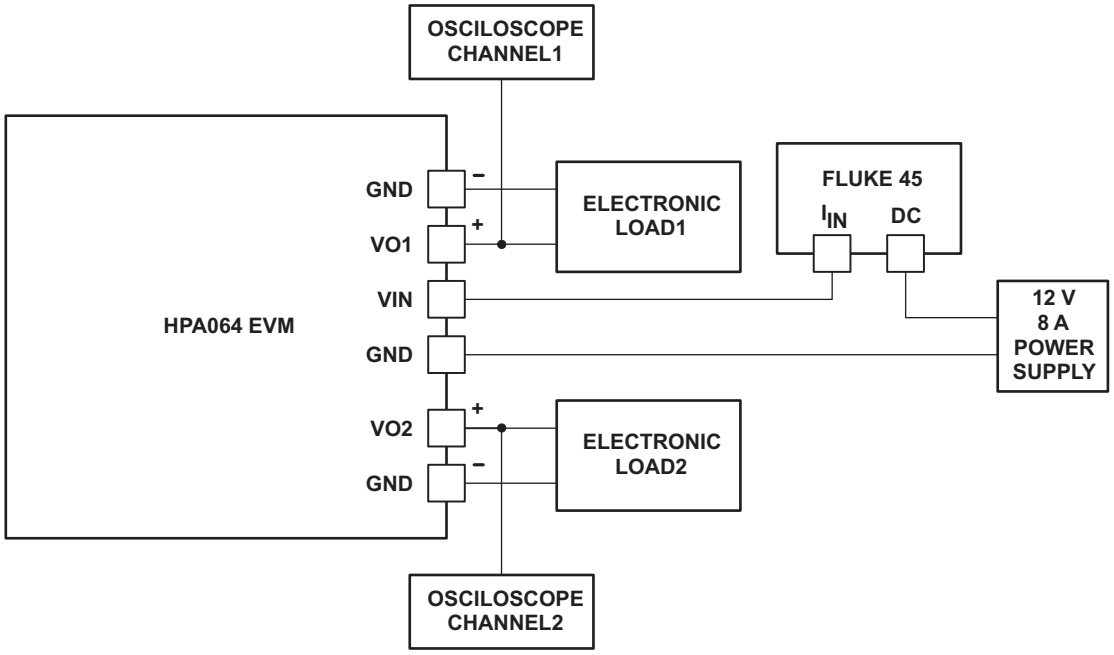


**Figure 4-1. TPS51020EVM-001 Schematic**

## 4.2 Power Up and Power Down

Figure 4-2 and Figure 4-3 show the power-up and power-down waveforms. The power good (PGOOD) pin jumps to high after both outputs have started and have been in regulation for 2048 clock pulses (6.8 ms).

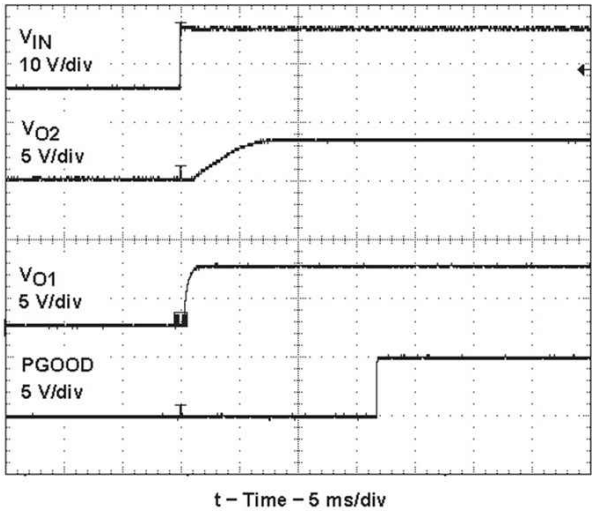


**Figure 4-2. Power-Up Waveform**

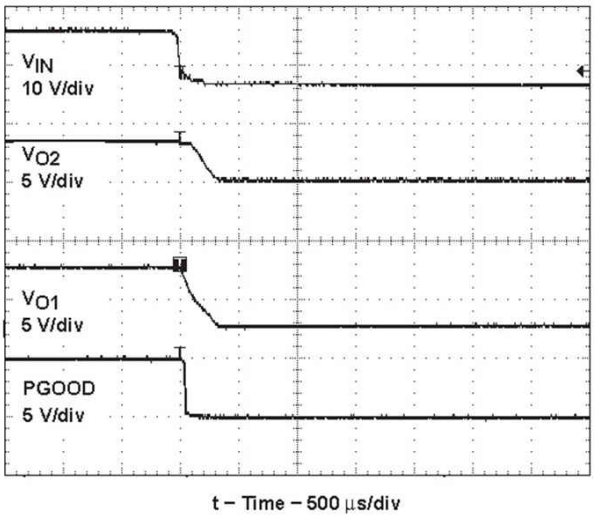


**Figure 4-3. Power-Down Waveform**

## 4.3 Efficiency and Power Loss

Figure 4-4 and Figure 4-5 show the test efficiency and power losses versus load current at different conditions. The maximum efficiency is approximately 94.8% when both channels are enabled. The total power loss is 3.5 W when both channels are on and delivering 6.0 A.

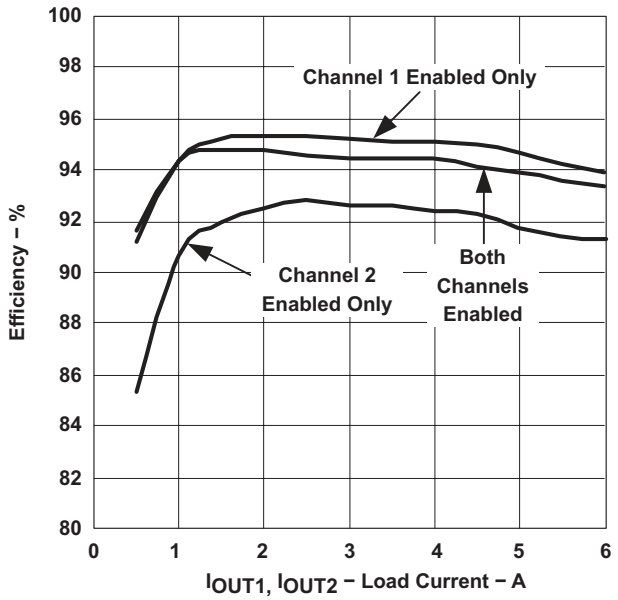


**Figure 4-4. Efficiency vs Load Current**

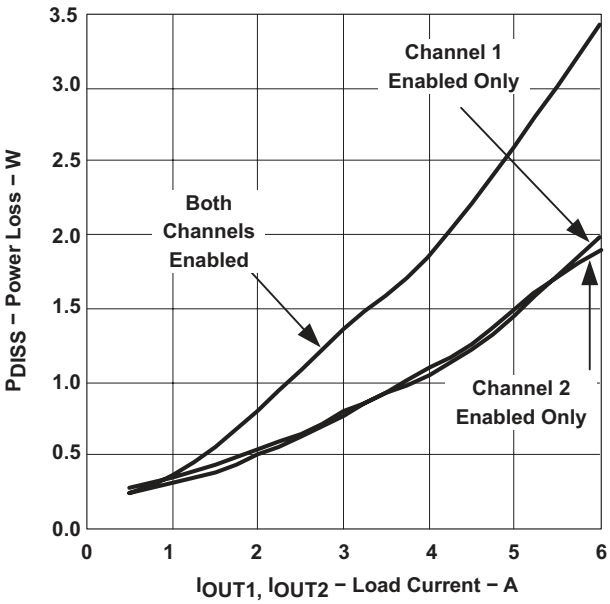


**Figure 4-5. Power Loss vs Current**

## 4.4 Output Ripple

In Figure 4-6, the output ripple waveform shows that two channels are running at 180º phase shift. The peak-to-peak ripple voltage is less than 40 mV in each channel.

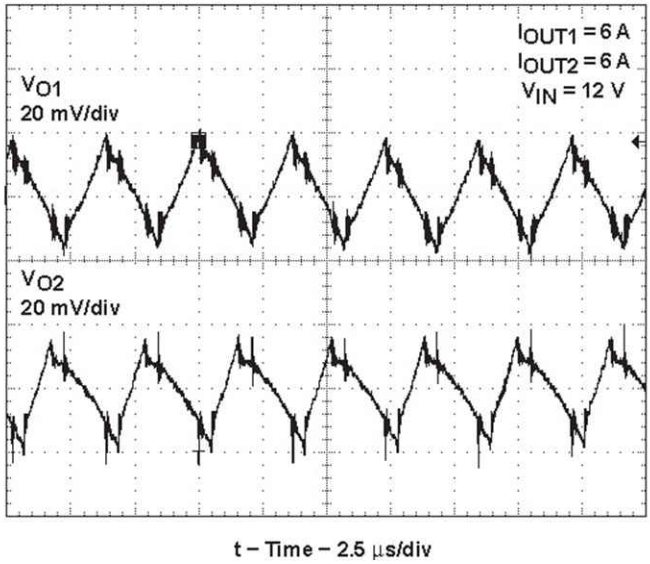


**Figure 4-6. Output Ripple**

## 4.5 Load Transient

Figure 4-7 and Figure 4-8 show the load transient waveforms for each channel. When load is stepped from 0 A to 5 A, the undershoot voltage is less than 60 mV and the settling time is less than 30 µs. When load is stepped down from 5 A to 0 A, the overshoot voltage is less than 50 mV and the settling time is less than 50 µs.

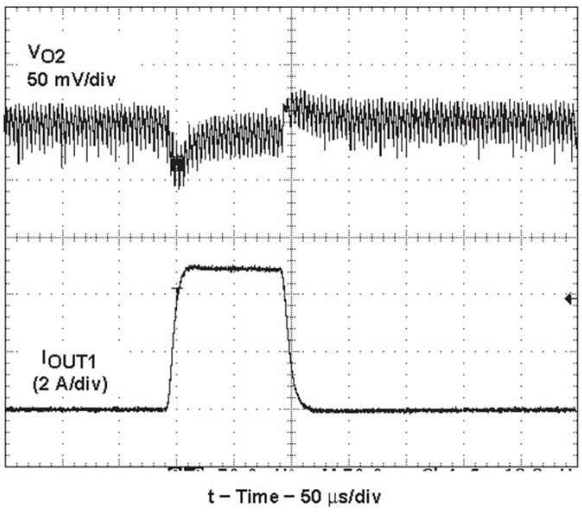


Figure 4-7. Channel 1 Load Transient Waveform

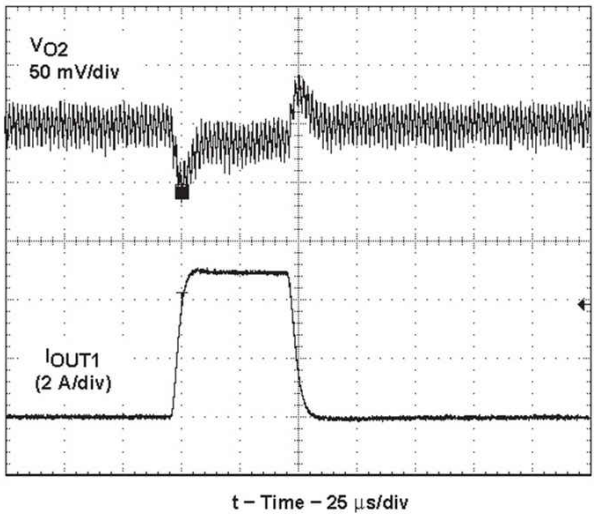


Figure 4-8. Channel 2 Load Transient Waveform

## 4.6 Loop Characteristics

Figure 4-9 and Figure 4-10 show the bode plot of each channel. The crossover frequency is approximately 14 kHz and the phase margin is 32° for Channel 1 when the output is 5 V and 6 A. Channel 2 shows a 15-kHz crossover frequency and a 41° phase margin.

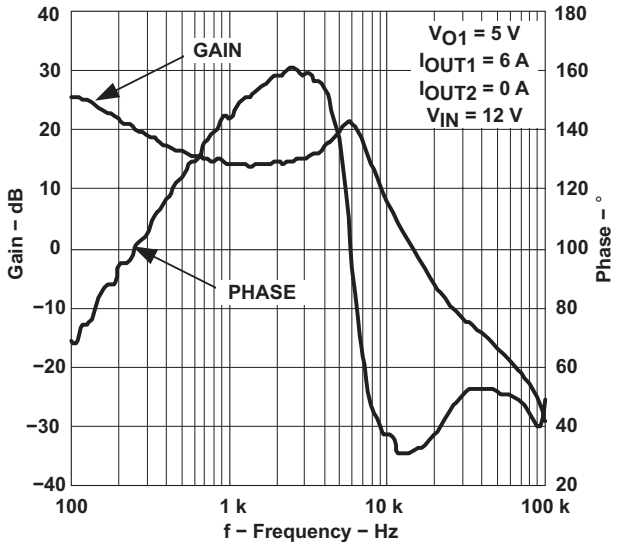


Figure 4-9. Channel 1 Bode Plot

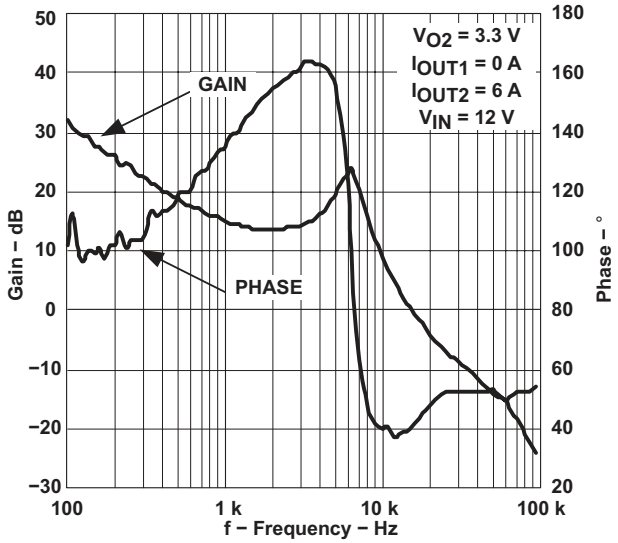


Figure 4-10. Channel 2 Bode Plot

## 5 Assembly Drawing and PCB Layout

Figure 5-1 through Figure 5-5 show the assembly drawing and each layer.

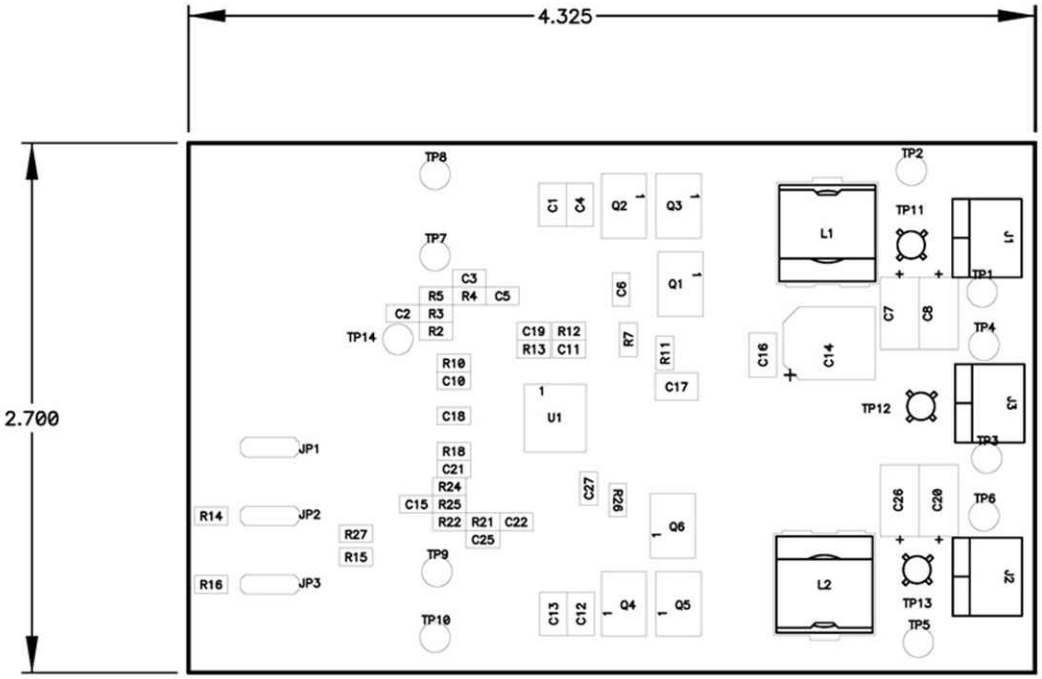


**Figure 5-1. Top Assembly**

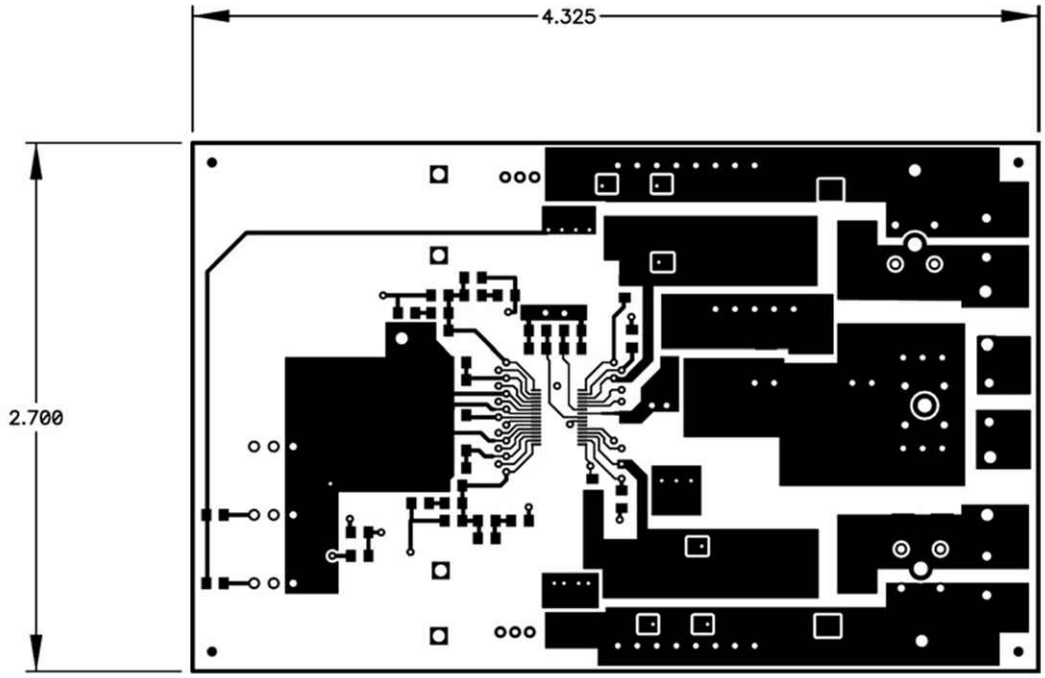


**Figure 5-2. Top Layer**

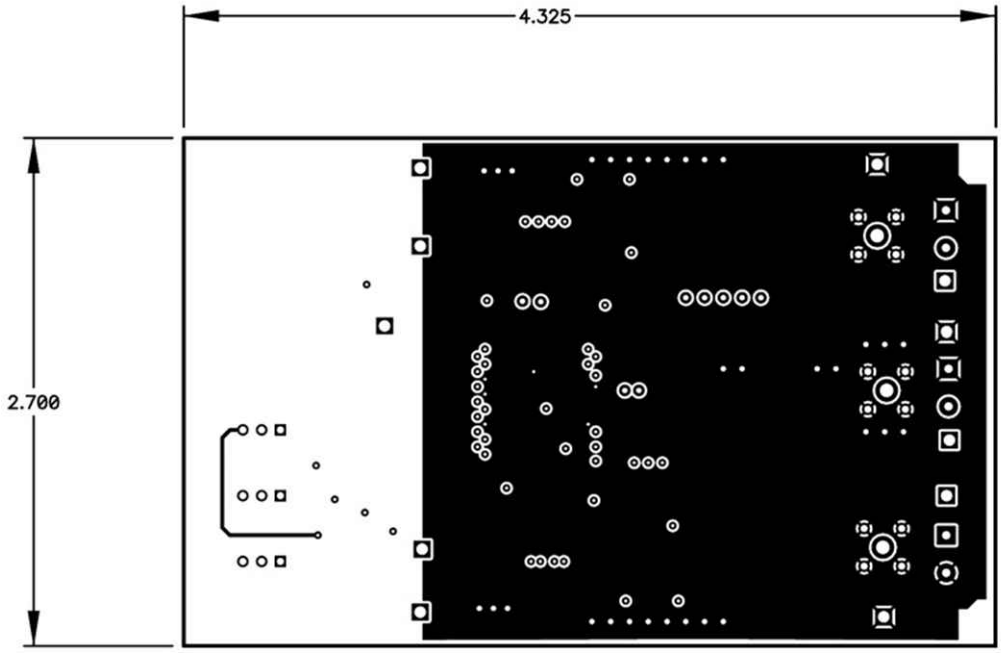


**Figure 5-3. Inner Layer 1**

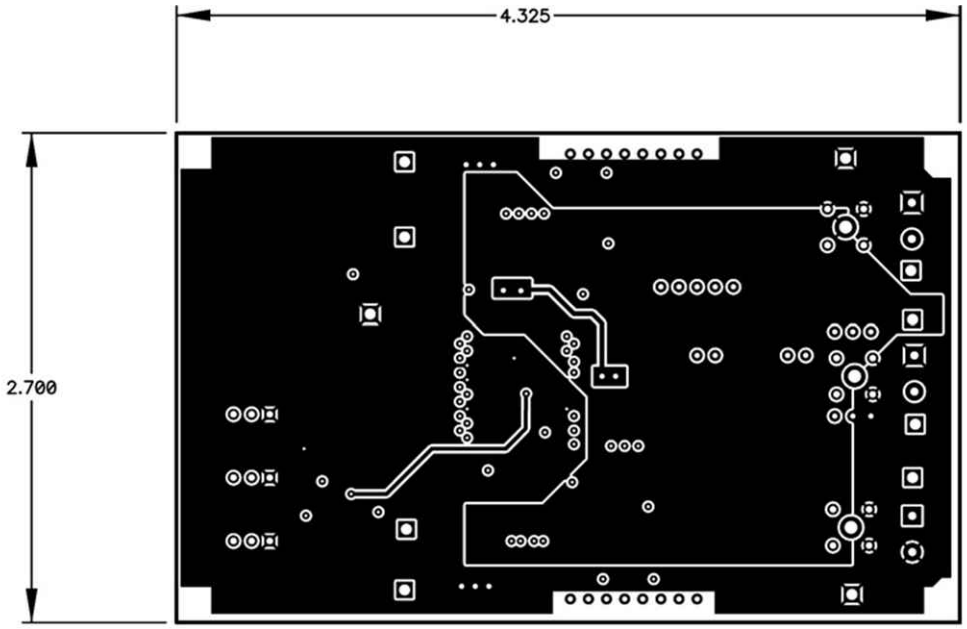


**Figure 5-4. Inner Layer 2**

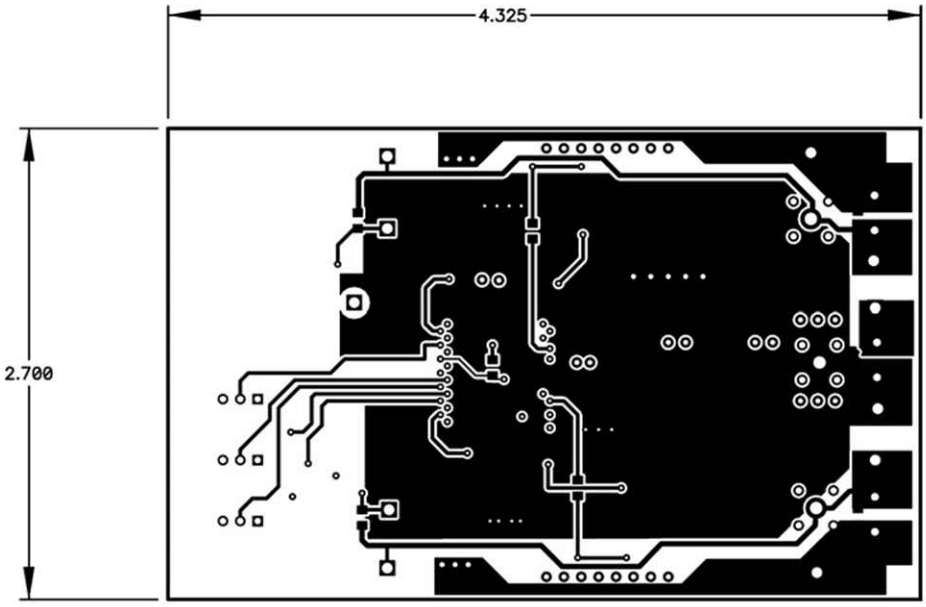


**Figure 5-5. Bottom Layer**

# 6 Circuit Module List of Materials

| RERERENCE DESIGNATOR | QTY | DESCRIPTION | SIZE | MFR | PART NUMBER |
|---|---|---|---|---|---|
| C1, C4, C12, C13, C16, C17 | 6 | Capacitor, ceramic, 2.2 mF, 25 V, X5R, 10% | 1210 | Panasonic | ECJ−4YB1E225K |
| C2, C15 | 2 | Capacitor, ceramic, 6800 pF, 25 V, X7R, 10% | 805 | Std | Std |
| C3, C11, C19, C25 | 0 | Capacitor, ceramic, TBD | 805 | Std | Std |
| C24 | 1 | Capacitor, ceramic, 4.7 mF,25 V, X5R, 10% | 805 | Panasonic | ECJ−2FB1E475M |
| C22 | 1 | Capacitor, ceramic, 3300 pF, 25 V, X7R, 5% | 805 | Std | Std |
| C14 | 1 | Capacitor, aluminum solid cap, with conductive polymer 22 mF, 35 V, 20% | 8.3m (E7) | Sanyo | 35SVPD22M |
| C5 | 1 | Capacitor, ceramic, 3900 pF, 25 V, X7R, 5% | 805 | Std | Std |
| C6, C18, C27 | 3 | Capacitor, ceramic, 0.1 mF,25 V, X7R, 10% | 805 | Std | Std |
| C7, C26 | 2 | Capacitor, aluminum, 150 mF, 6.3 V, 20% (UE Series) | 7343 | Panasonic | EEF−UE0J151R |
| C8, C20 | 0 | Capacitor, aluminum, 150 mF, 6.3 V, 20% (UE Series) | 7343 | Panasonic | EEF−UE0J151R |
| C9, C10, C21, C23 | 4 | Capacitor, ceramic, 0.01 mF, 25 V, X7R, 10% | 805 | Std | Std |
| L1, L2 | 2 | Inductor, SMT, 4.0 mH,10.3 A, 8.0 mW | 0.492 sq” | Sumida | CEP125(H)−4R0 |
| ShortsJumper | 3 | STC02SYAN | Shorts Jumper | Sullins | N/A |
| JP, JP2, JP3 | 3 | Header, 3 pin, 100-mil spacing (36-pin strip) | 0.100´ 3 | Sullins | PTC36SAAN |
| R1, R9 | 2 | Resistor, chip, 49.9 W,1/10−W, 1% | 805 | Vishay | Std |
| R10, R18 | 2 | Resistor, chip, 1M W,1/10W, 1% | 805 | Vishay | Std |
| R4 | 1 | Resistor,chip, 1.82 kW,1/10W, 1% | 805 | Vishay | Std |
| R21 | 1 | Resistor, chip, 2.74 kW,1/10W, 1% | 805 | Vishay | Std |
| R11 | 1 | Resistor, chip, 3.92 kW,1/10W, 1% | 805 | Vishay | Std |
| R2, R24 | 2 | Resistor, chip, 10.0 kW,1/10W, 1% | 805 | Vishay | Std |
| R7, R26 | 2 | Resistor, chip, 15 W,1/10W, 1% | 805 | Vishay | Std |
| R12, R13 | 2 | Resistor, chip, 18.2 kW,1/10W, 1% | 805 | Vishay | Std |
| R22 | 1 | Resistor, chip, 28.7 kW,1/10W, 1% | 805 | Vishay | Std |
| R5 | 1 | Resistor, chip, 48.7 kWs,1/10W, 1% | 805 | Vishay | Std |
| R14,R15, R16, R27 | 4 | Resistor, chip, 100 kW,1/10W, 1% | 805 | Vishay | Std |
| R3, R25 | 2 | Resistor, chip, 332 W,1/10W, 1% | 805 | Vishay | Std |
| R8, R19 | 2 | Resistor, chip, 0 W,1/10W, 1% | 805 | Vishay | Std |
| J1, J2, J3 | 3 | Terminal block, 2 pin, 15 A, 5.1 mm | 0.40´ 0.35 | OST | ED1609 |
| TP1,TP3, TP6, TP8, TP10 | 5 | Test point, 0.062 hole, red | 0.25 | Keystone | 5011 |
| TP2, TP4, TP5, TP7, TP9, TP14 | 6 | Test point, 0.062 hole, black | 0.25 | Keystone | 5010 |
| U1 | 1 | Dual voltage mode, DDR selectable, synchronous, step-down controller for notebook | TSSOP30 | TI | TPS51020DBT |
| TP11,T12, TP13 | 3 | Adaptor, 3.5-mm probe clip (or 131−5031−00) | 0.2 | Tektronix | 131−4244−00 |
| Q1, Q6 | 2 | Transistor, MOSFET, N-channel, 30 V, 8.4 A, Rds 22 mW | SO−8 | Fairchild | FDS6612A |
| Q2, Q4 | 2 | Transistor, MOSFET, N-channel, 30 V, 10 A, Rds 16 mW | SO−8 | Fairchild | FDS6690S |
| Q3, Q5 | 0 | Transistor, MOSFET, N-channel, 30 V, 10 A, Rds 16 mW | SO−8 | Fairchild | FDS6690S |

# 7 References

Texas Instruments, *TPS51020 Dual, Voltage Mode, DDR Selectable, Synchronous, Step−down Controller for Notebook System*

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (May 2004) to Revision A (March 2022) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 2 |
| • Updated the user's guide title. | 2 |

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