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UC385EVM-207
High-Current, Low-Input Voltage, Low-Dropout Linear Regulator EVM

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.7 V minimum to 7.5 V maximum, bias voltage range of 3.4 V minimum to 7.5 V maximum, and output current of 5 A maximum.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This user's guide describes the characteristics, operation and use of the UC385EVM-207 High-Current, Low-Input Voltage, Low-Dropout Linear Regulator evaluation module (EVM). The user's guide includes a schematic diagram, printed circuit board (PCB) layouts, and bill of materials. Electronic PCB layout files are available upon request.

How to Use This Manual

This document contains the following chapters:

❏ Chapter 1—Introduction

❏ Chapter 2—Test Setup and Results

❏ Chapter 3—Board Layout

❏ Chapter 4—Schematic and BIll of Materials

Related Documentation From Texas Instruments

SLUS317 – UCx82–x data sheet

SLUS212 – UCx85–x data sheet

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Figures

Tables

Introduction

This chapter contains background information for the UCx82-x and UCx85-x regulators and support documentation for the UC385EVM-207 evaluation module. The EVM performance specifications are also given.

1.1   Background

The purpose of the UC385EVM-207 is to facilitate evaluation of the UCx82-x and UCx85-x families of devices. The UC385EVM consists of the SLVP207 PCB, one UC385-ADJ adjustable, 5-A linear regulator in a TO-263 package, and supporting passive components. The adjustable device has been configured to output 1.2 V using a feedback resistor. The SLVP207 PCB is designed to accommodate multiple devices with similar pin-outs in different packages (i.e., TO–220, TO–263, or SOT–223). Specifically, in addition to the UCx82 and UCx85 families, the SLVP207 can be used with the TPS755xx, TPS756xx, TPS757xx, TPS758xx, TPS759xx, TPS725xx, TPS725xx, TPS795xx, TPS796xx, and TPS786xx families as well as any other device in the same package and with the same pinout. Therefore, some component footprints on the PCB are not populated.

The UCx82-x and UCx85-x families of high current LDO linear regulators use a NPN pass element and have very fast transient response, low noise, and high PSRR. In addition, these regulators have separate input and bias voltage pins and low dropout. The bias voltage input powers the internal circuitry of the IC. The input voltage pin needs to be at least 500 mV above the output voltage and provides current only for the NPN pass element; therefore, regulator efficiency can be improved and power dissipation can be reduced compared to typical regulators requiring input voltages of 2.5 V or more. Additional features, as well as detailed specifications, of the UCx82-x and UCx85-x regulator families can be found in the UCx82-x data sheet (SLUS317) or the UCx85-x data sheet (SLUS212).

1.2   Performance Specification Summary

Table 1–1 provides a summary of the performance specifications. All tests performed using V_B = 5.0 V, V_I = 1.8 V, and C_O = 100 µF unless otherwise specified.

Table 1–1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage	Min(V_{IN}–V_{OUT}) = 500 mV	1.7	1.8	7.5	V
Bias voltage	Min(V_B–V_{OUT}) = 2.2 V	3.4	5.0	7.5	V
Output voltage			1.2		V
Output current range		0.01		5	A
Load regulation†			0.5	4	mV
Load transient response	I_O = 10 mA to 5 A, $t_{(rise)}$ = 10 µs		–50		mV_{PK}
			32		µs
	I_O = 10 mA to 5 A, $t_{(fall)}$ = 5 µs		75		mV_{PK}
			40		µs
PSRR	f = 1kHz, I_O = 5 A		80		dB
Noise	V_I = 3.5 V, I_{OUT} = 2.5 A, BW = 200 Hz to 100 kHz, C_{OUT} = 100 µF		35		μV_{RMS}

† Per data sheet

1.3 Modifications

The UC385EVM-207 is designed to allow parts to be easily interchanged. Although the EVM is designed with a UC385-ADJ regulator in a TO-263 package, the SLVP207 EVM board can also accommodate any other member of the UCx82 or UCx85 families in either the TO-263 or TO-220 or any device with the same pinout in a TO-220, TO-263, or SOT-223 package. Passive elements such as the output capacitors (C4, C5) and the input capacitor (C3) can be easily changed. The EVM uses resistors R3 and R4 as the feedback resistors for the adjustable regulators. Capacitor C2 is used to reduce the inductance from long power source input leads and may or may not be necessary depending on the specific test setup.

Test Setup and Results

This chapter describes how to properly connect, setup, and use the UC385EVM-207. It also presents the test results for the more common tests performed using the EVM.
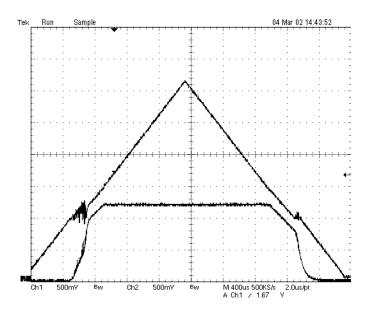
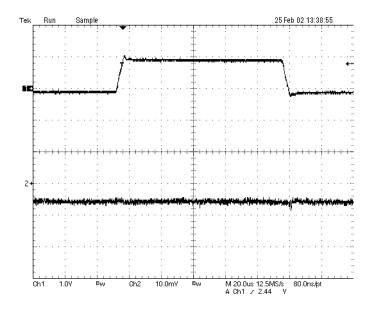## 2.1 Test Setup for DC Testing

Figure 2–1. Test Setup
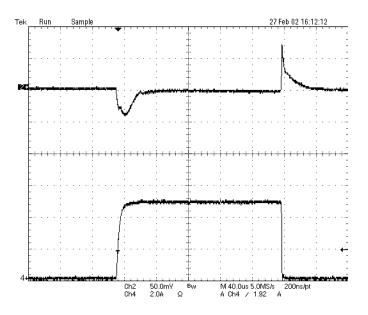
2.2 Test Results

Figure 2–2. Power Up

> Channel 1 is the input voltage and it ramps to 3.3 V. Channel 2 is the output
> voltage. The bias voltage is 5 V and the output current is 2.5 A.
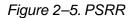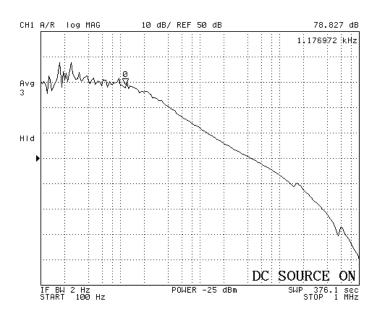
Figure 2–3. Line Transient Response

> Channel 1 is the input voltage stepped from 1.8 V to 2.8 V. Channel 2 is the
> output voltage with a dc offset of 1.2 V. The input bias voltage is 5.0 V. The
> output current is 5 A.

Figure 2–4. Load Transient Response

Channel 2 is the output voltage with a dc offset of 2 V and channel 4 is the output current. The input bias voltage is 5.0 V and the input voltage is 1.8 V.

Figure 2–5. PSRR

The bias voltage is 5 V. The input voltage is 1.8 V and the output voltage is 1.2 V. The output current is 5 A.

Chapter 3

Board Layout

This chapter provides a description of the SLVP207 board layout and layer illustrations used in the UC385EVM–207.

3.1 Layout

The EVM PCB consists of two layers of 1.5 oz. copper. The top side (component) layout of the EVM is shown in Figure 3–1. Large power and ground planes are used to minimize trace resistance. The input capacitor (C3) is located close to the input pin. Proper board layout is critical to ensure the best noise and PSRR performance. The ground side of the output capacitor (C4) is close to the board ground connection for improved transient response. Ground for the bypass capacitor (C5) has a low impedance connection to the ground for the IC. The top and bottom side layouts are shown in Figure 3–2 and Figure 3–3 respectively.
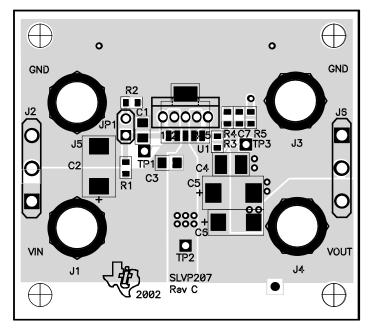
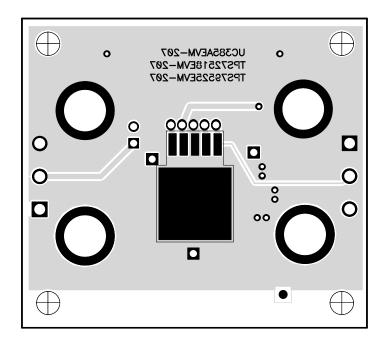*Figure 3–1. Top Side Asembly*

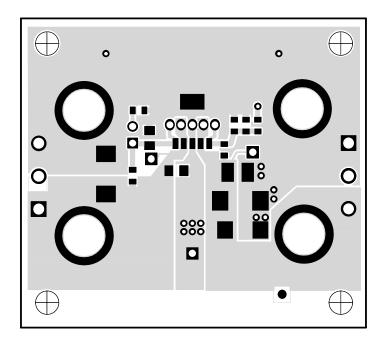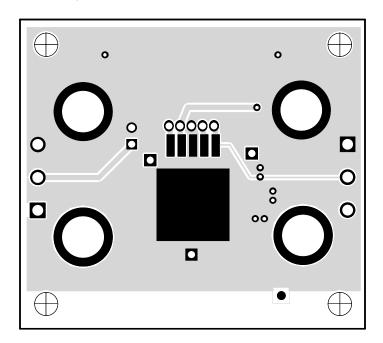*Figure 3–2. Bottom Side Assembly*
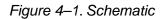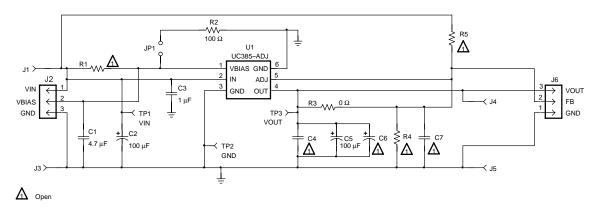

Figure 3–3. Top Side Layout

Figure 3–4. Bottom Side Layout

Schematic and Bill of Materials

The EVM schematic and bill of materials are presented in this chapter.

4.1 Schematic

Figure 4–1. Schematic

4.2 Bill of Materials

Table 4–1. Bill of Materials

COUNT	RefDes	Description	SIZE	MFR	Part Number
1	C1	Capacitor, ceramic, 4.7 µF, 6.3 V, X5R, 20%	805	Murata	GRM21BR60J475KA11
2	C2, C5	Capacitor, POSCAP, 100 µF, 10 V, 55 mΩ, 20%	7343 (D)	Sanyo	10TPB100M
1	C3	Capacitor, ceramic, 1.0 µF, 10 V, X7R, 10%	805	Murata	GRM21BR71C105KA01
1	C4	Open	1210		
1	C6	Open	6032(C)		
1	C7	Open	603		
4	J1, J3, J4, J5	Connector, mini banana jack, uninsulated, 4 mm diameter	0.300 OD	Hirschmann	B0 10
2	J2, J6	Header, 3 pin, 5 mm spacing	0.197 x 3 in	OST	ED1661
1	JP1	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100 x 2 in	Sullins	PTC36SAAN
3	R1, R4, R5	Open	603		
1	R2	Resistor, chip, 100 Ω, 1/16–W, 1%	603	Std	Std
1	R3	Resistor, chip, 0 Ω, 1/16–W, 1%	603	Std	Std
2	TP1, TP3	Test point, red, 1 mm	0.038 in	Farnell	240–345
1	TP2	Test point, black, 1 mm	0.038 in	Farnell	240–333
1	U1	IC, LDO regulator, adj., 5 A	TO–263	TI	UC385–ADJ
1	—	PCB, 2.055 in x 1.85 in x 0.062 in		Any	SLVP207
1	—	Shunt, 100-mil, black	0.100	3M	929950-00