UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller

1 Features

- Ultra-low no-load input power enables < 80-mW standby power at 230 V_{AC} in PFC+LLC system
- Excellent light load efficiency and high efficiency over wide range of load due to multi-mode TM and DCM control
- Enables low system cost through FET drain valley synchronized turn-on which eliminates need for second winding on the boost inductor
- Enables compliance to green power standards without disabling PFC
  - EuP Lot 6 Tier 2, CoC Ver. 5 Tier 2, Energy Star Ver. 6.1, DoE Level VI
- Burst mode with soft-entry and soft-exit periods enables ultra-low audible noise output
- Enhanced error amplifier, responds rapidly to load steps without degrading input current distortion
- User adjustable valley delay ensures valley switching
- Low start-up current consumption (<46 µA)
- Wide VCC range 8.5 V to 34 V
- Cycle-by-cycle current limit
- Second independent output over-voltage protection
- Integrated over-temperature protection
- Create a custom design using the UCC28056 device with the WEBENCH® Power Designer

2 Applications

- Desktop computing and digital TV
- Gaming, set top box and AC adapter front end
- LED drivers and luminaries
- Industrial and medical power supplies, e-bike chargers, power tools chargers

3 Description

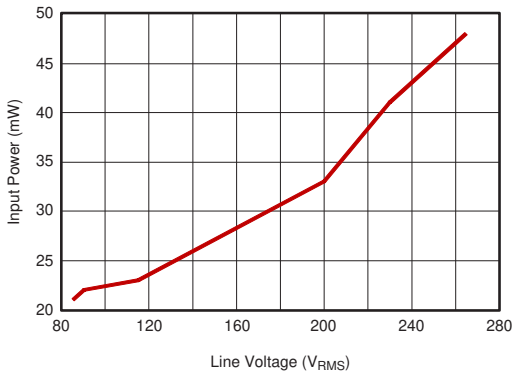
The UCC28056 device drives PFC boost stages based on an innovative mixed mode method that operates in transition mode (TM) at full load and transitions seamlessly into discontinuous conduction mode (DCM) at reduced load, automatically reducing switching frequency. This device incorporates burst mode operation to further improve light load performance, enabling systems to meet challenging energy standards while eliminating the need to switch off the PFC. UCC28056 can drive a PFC power stage up to 300 W, ensuring sinusoidal line input current with low distortion, close to unity power factor. When used with the LLC controller UCC256403/4, and dual synchronous rectifier controller UCC24624 less than 80 mW system standby power can be achieved, enabling PFC always on architecture and eliminating the need for an auxiliary converter. This with FET Drain valley turn-on with simple boost inductor allows fewest component count and reduced system cost.

Device Information(1)

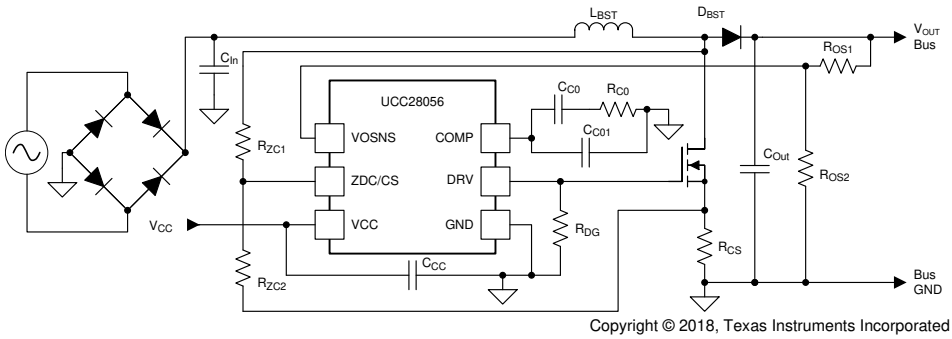
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28056	SOT-23(6)	2.90 mm x 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

No Load Power



Simplified Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April, 2019) to Revision E — **Page**

- Added target market applications. ... 4
- Added explanation for ZCD noise immunity. ... 4
- Changed new variant of LLC controller. ... 14
- Added burst mode modified ... 14
- Added burst mode levels for versions. ... 25
- Added burst modes for different versions ... 25
- Changed boost inductance calculation. ... 30
- Changed inductor requirements. ... 31

Changes from Revision C (February 2018) to Revision D — **Page**

- Added Link to UCC256403/4 LLC controller ... 1
- Added Link to UCC24624 synchronous rectifier controller ... 1
- Updated *Description* section ... 1
- Updated *Description* section ... 1
- Added Device Comparison Table. ... 4
- Changed $V_{BSTFall}$ graph into normalized graph. ... 12
- Changed $V_{BSTRise}$ graph into normalized graph. ... 12
- Changed $V_{OSNSOVP1Rise}$ graph into normalized graph. ... 13
- Changed $V_{OSNSOVP1Fall}$ graph into normalized graph ... 13

Changes from Revision B (January 2018) to Revision C — **Page**

- Updated *Description* section ... 1

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Changes from Revision A (November 2017) to Revision B **Page**

- Updated *Simplified Application* 1
- Changed document status from *Advance Information* to *Production Data* 1

Changes from Original (October 2017) to Revision A **Page**

- Added WEBENCH links to data sheet 1

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5 Device Comparison Tables

DEVICE	UCC28056	UCC28056A	UCC28056B	UCC28056C
Target Applications	**Not recommended for new design**	**PFC Bus output >400VDC**	**Improved audible noise performance**	**Drop in replacement for UCC28056**
OVP2 FEATURE INCLUDED	YES	NO	YES	YES
OVP1 THRESHOLD	110% Vout	108% Vout	110% Vout	110% Vout
BURST MODE THRESHOLD	< 10% Load	< 15% Load	< 15% Load	< 10% Load
ZCD NOISE IMMUNITY	Basic noise immunity	Improved noise immunity	Improved noise immunity	Improved noise immunity

The enhanced noise immunity of UCC28056A, UCC28056B, and UCC28056C provides system robustness advantages and less sensitivity to PCB layout than the UCC28056. For more information on the system level benefits that UCC28056A, UCC28056B and UCC28056C provide, please see UCC28056X Selection Guide SLUA974.

PARAMETER		DEVICE	MIN	TYP	MAX	UNIT
Output Over Voltage Protection						
$V_{OSOvp1Rise}$	VOSNS over-voltage threshold, rising, VCC = 12 V	UCC28056A	2.64	2.7	2.76	V
		UCC28056	2.69	2.75	2.81	
		UCC28056B				
		UCC28056C				
$V_{OSOvp1Fall}$	VOSNS over-voltage threshold, falling, VCC = 12 V	UCC28056A	2.55	2.625	2.68	V
		UCC28056	2.60	2.675	2.73	
		UCC28056B				
		UCC28056C				
$V_{OSOvp1Hyst}$	VOSOovp1Rise - VOSOovp1Fall	All	0.072			V
$T_{Ovp2Blk}$	Ovp2 Comparator output is blanked for this period after falling edge of DRV	UCC28056A	Not Applicable			
		UCC28056	520	620	720	ns
		UCC28056B				
		UCC28056C				
$T_{Ovp2bEn}$	Ovp2b fault is detected if ZCD is detected during this period after falling edge of Ovp2 Comparator output	UCC28056A	Not Applicable			
		UCC28056	620	720	820	ns
		UCC28056B				
		UCC28056C				
V_{Ovp2Th}	Second level output over-voltage fault Threshold	UCC28056A	Not Applicable			
		UCC28056	1.102	1.125	1.148	ns
		UCC28056B				
		UCC28056C				
Burst Mode Operation						
$V_{BSTFall}$	VCOMP Burst Threshold Falling	UCC28056		0.5		V
		UCC28056C				
		UCC28056A		0.75		
		UCC28056B				
$V_{BSTRise}$	VCOMP Burst Threshold Rising	UCC28056		0.625		
		UCC28056C				
		UCC28056A		0.875		
		UCC28056B				

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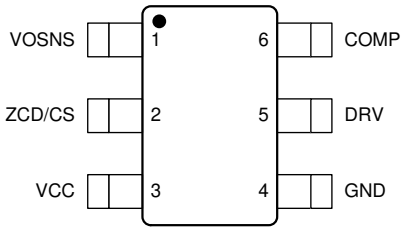
6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	6	I/O	Output of the internal transconductance error amplifier and power demand input. To achieve compensation of the voltage loop, connect a suitable RC network from this pin to GND. The error amplifier output is internally limited to V_{COClmp}. An internal resistor, $R_{CODisch}$, discharges the external compensation network when the controller is in its Stopb state or when the Ovp2 comparator is tripped. Switching stops, and the controller enters a low-power state (BstOffb), when the voltage on the COMP pin drops below $V_{BSTFall}$. Switching resumes when the COMP pin voltage exceeds $V_{BSTRise}$.
DRV	5	I/O	GATE connection to drive the main power MOSFET. This output is internally limited to V_{DRHigh}. This is done to reduce power dissipation in the internal driver and allow controller operation from high VCC voltages. An external resistor connected from DRV to GND adjusts the delay between the Drain waveform falling below V_{In} and the DRV rising edge, allowing the turn on transition to be aligned to the valley minimum accurately over a wide range of idle ring oscillating frequency.
GND	4	G	Controller Ground reference pin. Connect to the power stage at the lower terminal of the current sense resistor, R_{CS}, only.
VCC	3	P	Positive supply voltage. Switching operation can start once VCC exceeds $V_{CCStart}$. Switching operation ceases if VCC drops below V_{CCStop} for longer than $T_{UVLOBlk}$.
ZCD/CS	2	I	This pin is fed by a potential divider connected across the Drain & Source pins of the power MOSFET switch. While the DRV pin is high this pin monitors the voltage across the current sense resistor, R_{CS}. This pin implement over-current protection functions. While the DRV pin in low this pin monitors the Drain voltage waveform. Input voltage applied to the power stage can be obtained by filtering the Drain waveform. Input voltage provides Line voltage feed - forward and Line Brown - In features. Drain voltage waveform is also used to provide ZCD detection, valley synchronization and second level output over - voltage protection features.
VOSNS	1	I	Voltage error amplifier inverting input. The error amplifier non - inverting input connects to internal reference voltage V_{OSReg}. Error amplifier gain increases with error magnitude to improve transient response without compromising Line current distortion. Output over-voltage protection is implemented on this pin. Switching operation halts if the voltage on this pin exceeds $V_{Ovp1Rise}$ and resumes when it drops below $V_{Ovp1Fall}$.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VCC	-0.5	36	V
	ZCD/CS	-0.5	7	
	VOSNS	-0.5	7	
Output voltage	COMP	-0.5	7	V
	DRV	-0.3	20	
Junction temperature range	T_J	-40	150	°C
Storage temperature range, T_{stg}	T_{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Input voltage		12		V
T_A	Operating ambient temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCC28056 SOT23-6 6 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	116.4	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	74.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	36.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{CCStart}$	Turn-on threshold	VCC Rising		10.65	11	V
V_{CCStop}	Turn-off threshold	VCC Falling	8.5	8.85	9.2	V
V_{CCHyst}	UVLO Hysteresis ($V_{CCStart}$ - V_{CCStop}) (1)		1.5			V
$T_{UVLOBlk}$	Turn-OFF Blanking Time		27	35	42	µs
SUPPLY CURRENT						
$I_{CC_Startup}$	Current consumption before startup	VCC = $V_{CCStart}$-200mV, T_A < 110℃			46	µA
I_{CC_FAULT}	Current consumption during fault condition	VCC = 12V			130	µA
I_{CC_BSTOFF}	Current consumption during Burst OFF period	VCC = 12V			132	µA
I_{CC_RUN}	Operating current with DRV pin unloaded	VCC = 12V		1.8	2.2	mA
GATE DRIVE						
V_{DRLow}	DRV output low voltage	I_{DR} = 100mA			0.9	V
V_{DRHigh}	DRV output voltage high level, limited	VCC = 25V, I_{DR} = -10mA	10	13.7	15	V
$V_{DRHighMin}$	DRV minimum high voltage level	VCC = V_{CCStop} + 200 mV, I_{DR} = -8mA	8			V
R_{DRH}	DRV, Pull-up resistance	T_A = -40°C to 125°C, I_{DR} = -8mA, VCC=12V		9.7	16	Ω
R_{DRL}	DRV, Pull-down resistance	T_A = -40°C to 125°C, I_{DR} = 100mA	2.0	4.6	9	Ω
t_R	Rise Time	CLOAD=1nF, DRV=1V to 6V, VCC=12V	10	34	61	ns
t_F	Fall Time	CLOAD=1nF, DRV=6V to 1V, VCC=12V	4	15	40	ns
Isource	Source peak current on DRV Pin (1)			-0.7		A
Isink	Sink peak current on DRV Pin (1)			1		A
R_{DG0}	DRV to GND resistance value to select T_{ZCDR0} (1)		130	200		kΩ
R_{DG1}	DRV to GND resistance value to select T_{ZCDR1} (1)		81.18	82	82.82	kΩ
R_{DG2}	DRV to GND resistance value to select T_{ZCDR2} (1)		61.38	62	62.62	kΩ
R_{DG3}	DRV to GND resistance value to select T_{ZCDR3} (1)		42.57	43	43.43	kΩ
R_{DG4}	DRV to GND resistance value to select T_{ZCDR4} (1)		26.73	27	27.27	kΩ
R_{DG5}	DRV to GND resistance value to select T_{ZCDR5} (1)		17.82	18	18.18	kΩ
R_{DG6}	DRV to GND resistance value to select T_{ZCDR6} (1)		12.87	13	13.13	kΩ
R_{DG7}	DRV to GND resistance value to select T_{ZCDR7} (1)		9	9.1	9.2	kΩ
T_{DGSmpl}	Time needed to detect R_{DG} value.	T_A < 85℃	3.95	4.4	4.95	ms
V_{DGClmp}	Maximum voltage that will be applied on DRV pin while detecting R_{DG} value.		1	1.05	1.1	V
Error Amplifier						
V_{OSReg}	Feedback voltage reference		2.45	2.5	2.55	V
I_{OSBias}	ISNS pin bias current	V_{OS} = V_{OSReg}	-100		100	nA
g_M	Error Amplifier Transconductance Gain	$\lvert V_{OS}-V_{OSReg} \rvert$ < DSuThs		50		µS

(1) Not tested in production. Ensured by design.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
g_{MNL}	Error Amplifier Transconductance Gain for large error	$\lvert V_{OS}-V_{OSReg}\rvert$ > DSuThs		300		µS
DSuThs	Non-Linear Gain Threshold		67			mV
$R_{CODisch}$	Internal COMP to GND resistance when in STOPb state.		4.3	5	5.7	kΩ
V_{COClmp}	COMP pin internal high clamp voltage		5.5	5.6	5.71	V
V_{COSat}	COMP pin internal low clamp voltage (1)			0		V
I_{COMin}	COMP Maximum Source Current			-120		µA
I_{COMax}	COMP Maximum Sink Current			120		µA
Line Voltage Feed-Forward						
$T_{HLinMax}$	Line peak sampling window (1)	While switching	11	12.3	13.6	ms
$V_{FF0Rise}$	Comparator rising threshold switching from G_{FF0} to G_{FF1} (1)			0.348		V
$V_{FF1Rise}$	Comparator rising threshold switching from G_{FF1} to G_{FF2} (1)			0.406		V
$V_{FF2Rise}$	Comparator rising threshold switching from G_{FF2} to G_{FF3} (1)			0.473		V
$V_{FF3Rise}$	Comparator rising threshold switching from G_{FF3} to G_{FF4} (1)			0.552		V
$V_{FF4Rise}$	Comparator rising threshold switching from G_{FF4} to G_{FF5} (1)			0.644		V
$V_{FF5Rise}$	Comparator rising threshold switching from G_{FF5} to G_{FF6} (1)			0.751		V
$V_{FF6Rise}$	Comparator rising threshold switching from G_{FF6} to G_{FF7} (1)			0.875		V
$V_{FF0Fall}$	Comparator falling threshold switching from G_{FF1} to G_{FF0} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.331		V
$V_{FF1Fall}$	Comparator falling threshold switching from G_{FF2} to G_{FF1} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.386		V
$V_{FF2Fall}$	Comparator falling threshold switching from G_{FF3} to G_{FF2} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.45		V
$V_{FF3Fall}$	Comparator falling threshold switching from G_{FF4} to G_{FF3} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.524		V
$V_{FF4Fall}$	Comparator falling threshold switching from G_{FF5} to G_{FF4} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.612		V
$V_{FF5Fall}$	Comparator falling threshold switching from G_{FF6} to G_{FF5} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.713		V
$V_{FF6Fall}$	Comparator falling threshold switching from G_{FF7} to G_{FF6} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.832		V
G_{FF0}	Line Feed-Forward gain level 0 (1)			1		
G_{FF1}	Line Feed-Forward gain level 1 (1)			0.735		
G_{FF2}	Line Feed-Forward gain level 2 (1)			0.541		
G_{FF3}	Line Feed-Forward gain level 3 (1)			0.398		
G_{FF4}	Line Feed-Forward gain level 4 (1)			0.292		
G_{FF5}	Line Feed-Forward gain level 5 (1)			0.215		
G_{FF6}	Line Feed-Forward gain level 6 (1)			0.158		
G_{FF7}	Line Feed-Forward gain level 7 (1)			0.116		
Maximum ON Time						
T_{ONMAX0}	Maximum ON time when $G_{FF} = G_{FF0}$		12.1	12.8	13.2	µs
T_{ONMAX1}	Maximum ON time when $G_{FF} = G_{FF1}$		10.42	10.98	11.28	µs

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ONMAX2}	Maximum ON time when $G_{FF} = G_{FF2}$		8.85	9.41	9.64	µs
T_{ONMAX3}	Maximum ON time when $G_{FF} = G_{FF3}$		7.59	8.07	8.32	µs
T_{ONMAX4}	Maximum ON time when $G_{FF} = G_{FF4}$		6.52	6.92	7.18	µs
T_{ONMAX5}	Maximum ON time when $G_{FF} = G_{FF5}$		5.56	5.93	6.16	µs
T_{ONMAX6}	Maximum ON time when $G_{FF} = G_{FF6}$		4.73	5.09	5.28	µs
T_{ONMAX7}	Maximum ON time when $G_{FF} = G_{FF7}$		4.07	4.36	4.57	µs
Burst Mode Operation See **Device Comparison Table**						
Zero Current Detection and Valley Synch						
$V_{ZcdVinHyst}$	ZcdVin Comparator hysteresis (1)		12	19	26	mV
$T_{DCHVinMin}$	ZcdVin Comparator blanking from DRV falling edge (1)		250	358	467	ns
T_{ZCDTo}	If no negative transitions on Vin comparator for this period then do not wait for valleys		2.035	2.4	3.0	µs
T_{ZCDR0}	Minimum ZCD to DRV delay.	From $V_{ZC} < V_{InSynth}$ to DRV = 6V, C_{DR} = 1nF, Fres = 1.2MHz, $R_{DG} = R_{DG0}$		170	235	ns
ΔT_{ZCDR1}	$T_{ZCDR1} = T_{ZCDR0} + \Delta T_{ZCDR1}$ (1)	$R_{DG} = R_{DG1}$	34.6	45.5	58.5	ns
ΔT_{ZCDR2}	$T_{ZCDR2} = T_{ZCDR0} + \Delta T_{ZCDR2}$ (1)	$R_{DG} = R_{DG2}$	76	90	107	ns
ΔT_{ZCDR3}	$T_{ZCDR3} = T_{ZCDR0} + \Delta T_{ZCDR3}$ (1)	$R_{DG} = R_{DG3}$	114	130	147	ns
ΔT_{ZCDR4}	$T_{ZCDR4} = T_{ZCDR0} + \Delta T_{ZCDR4}$ (1)	$R_{DG} = R_{DG4}$	157	175	193	ns
ΔT_{ZCDR5}	$T_{ZCDR5} = T_{ZCDR0} + \Delta T_{ZCDR5}$ (1)	$R_{DG} = R_{DG5}$	229	255	281	ns
ΔT_{ZCDR6}	$T_{ZCDR6} = T_{ZCDR0} + \Delta T_{ZCDR6}$ (1)	$R_{DG} = R_{DG6}$	301	335	369	ns
ΔT_{ZCDR7}	$T_{ZCDR7} = T_{ZCDR0} + \Delta T_{ZCDR7}$ (1)	$R_{DG} = R_{DG7}$	373	415	457	ns
V_{DDAmpl}	Amplitude of 500 kHz sinewave signal on ZCD/CS pin needed to trigger knee detector		25			mV
$T_{DCHDDMin}$	Knee point detector blanking period (1)	Measured from falling edge of DRV pulse		1.5		µs
Fault Protection						
$T_{LongFlt}$	Long Fault Duration (1)			1		s
Line Brown-In Protection						
$V_{ZCBoRise}$	Brown-out Protection Threshold when in Stopb state	Peak cycle average voltage on ZCD/CS Pin.	0.282	0.3	0.318	V
I_{ZCBias}	ZCD/CS Pin Bias Current (1)	$V_{ZC} = V_{ZCBoFall}$	-100		100	nA
Over-Current Protection						
V_{ZCOcp1}	ZCD/CS First Level over-current protection threshold		450	500	550	mV
V_{ZCOcp2}	ZCD/CS Second Level over-current protection threshold		670	750	825	mV
$T_{Ocp1Blk}$	ZCD/CS blanking time from DRV rising edge to Enable Ocp1 Comparator Output (1)			450		ns
$T_{Ocp2Blk}$	ZCD/CS blanking time from DRV rising edge to Enable Ocp2 Comparator Output (1)			250		ns
$T_{OcpDrvDel}$	ZCD/CS crossing V_{OcpxTh} to DRV falling edge.			56	120	ns
$T_{DCHMax0}$	Max duration of T_{DCHb} state if no ZCD signal detected. After no OCPx Events (1)			250		µS

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{DCHMax1}$	Max duration of T_{DCHb} state if no ZCD signal detected. After one OCPx Events (1)			500		µS
$T_{DCHMax2}$	Max duration of T_{DCHb} state if no ZCD signal detected. After two consecutive OCPx Events (1)			1000		µS
Output Over-Voltage Protection	**See Device Comparison Table**					
Thermal Protection						
$T_{TSDRise}$	Thermal Shutdown Rising Threshold (1)	While switching	135	145	155	°C
$T_{TSDFall}$	Thermal Shutdown Falling Threshold (1)	While not switching	95	105	115	°C
$T_{TSDHyst}$	$T_{TSDRise}$ - $T_{TSDFall}$ (1)		38	40	42	°C

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7.6 Typical Characteristics

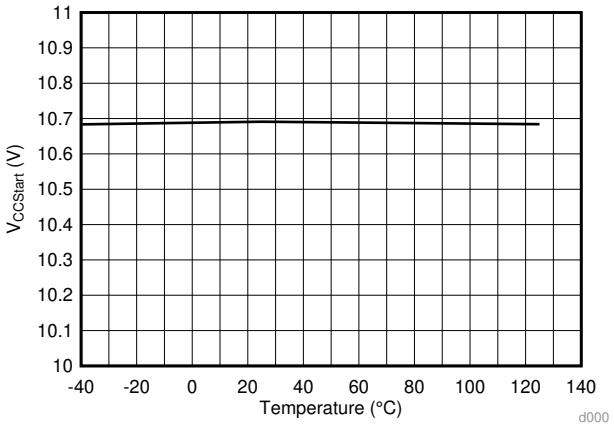


Figure 1. VCCStart Threshold vs Temperature

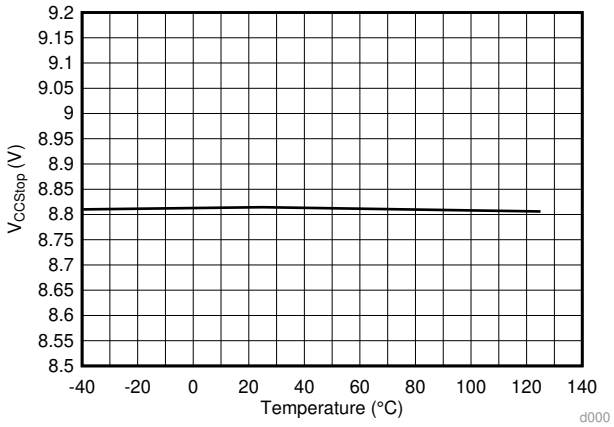


Figure 2. VCCStop Threshold vs Temperature

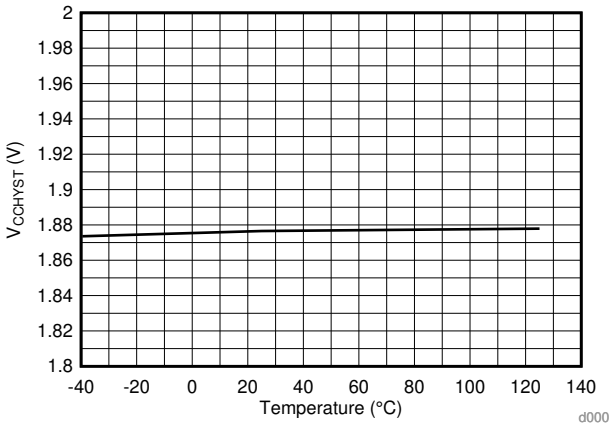


Figure 3. VCC Hysteresis vs Temperature

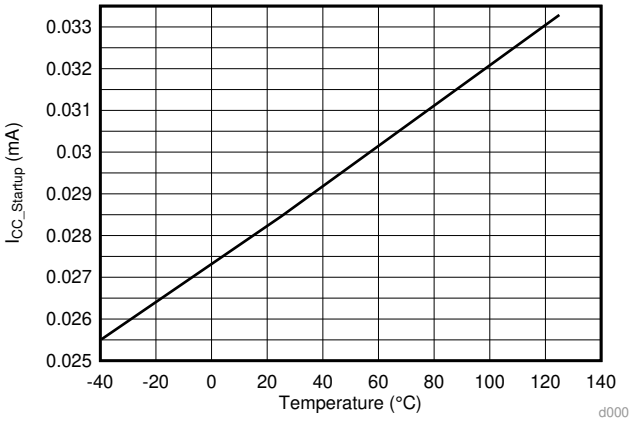


Figure 4. VCC Startup Current vs Temperature

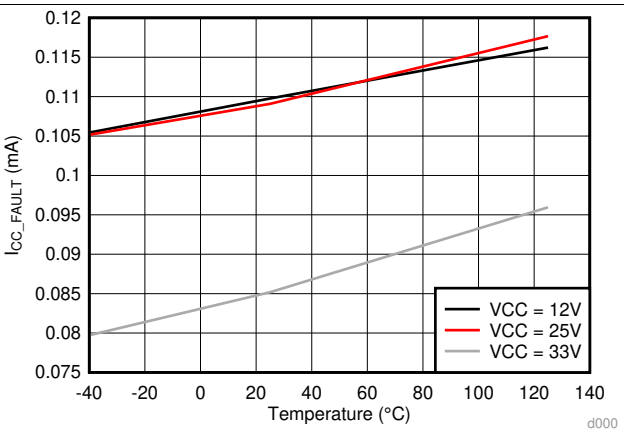


Figure 5. VCC Fault Current vs Temperature

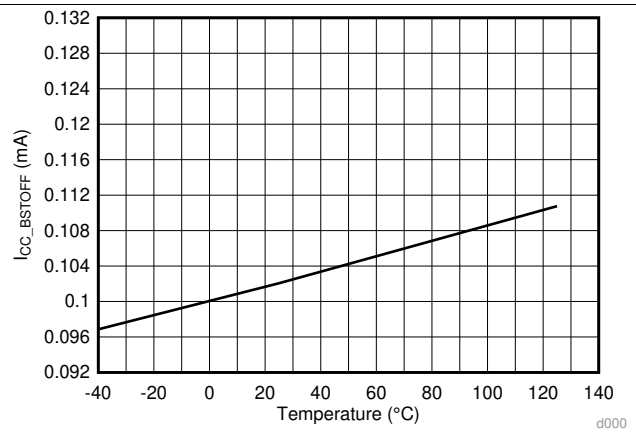


Figure 6. VCC Burst Off Current vs Temperature

Typical Characteristics (continued)

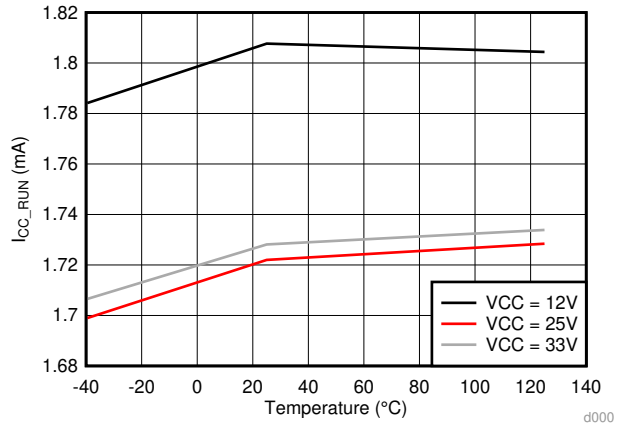


Figure 7. VCC Curent Run Mode vs Temperature

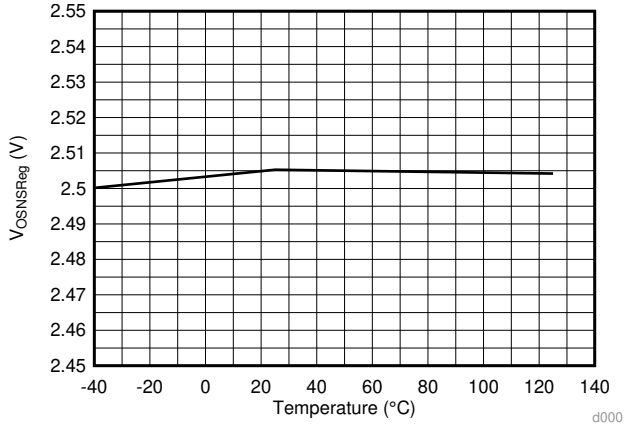


Figure 8. VOSNSReg vs Temperature

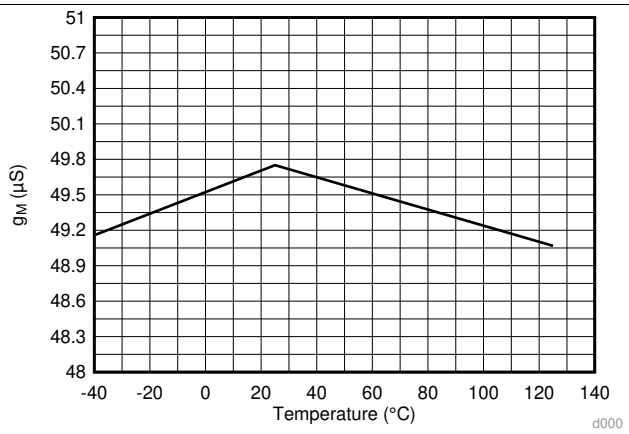


Figure 9. gM vs Temperature

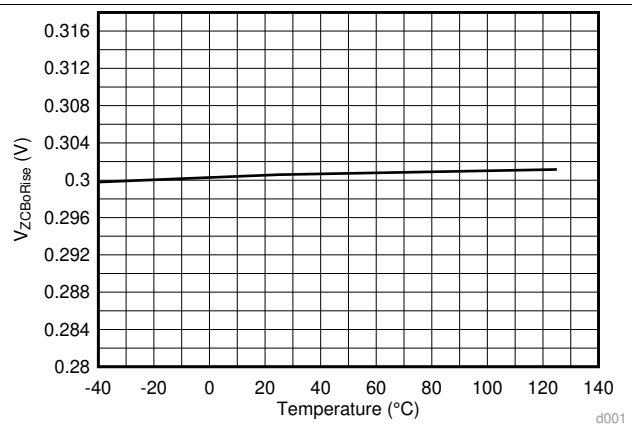


Figure 10. VBoRise vs Temperature

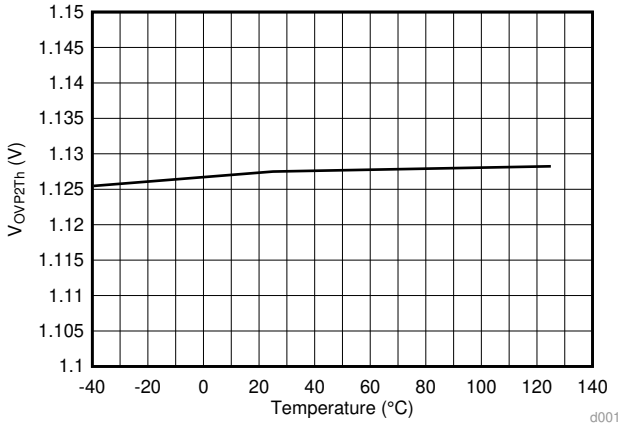
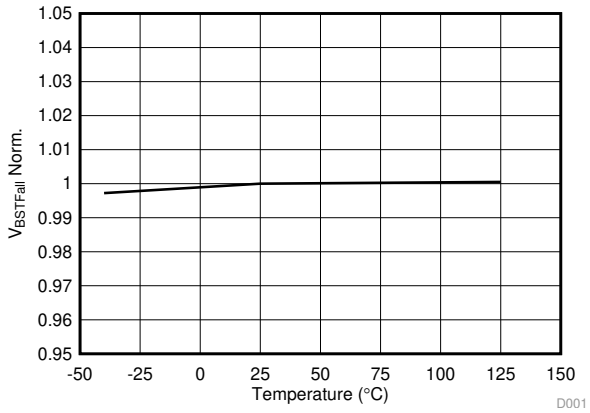


Figure 11. VOVP2 Threshold vs Temperature



It is Normalized respect its value at 25°C

Figure 12. Burst Mode Falling Threshold vs Temperature

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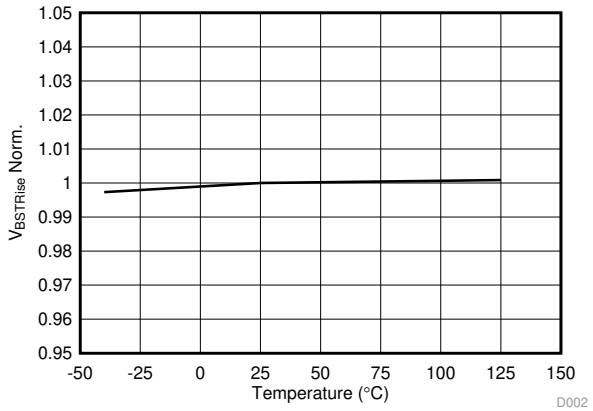
Typical Characteristics (continued)



It is Normalized respect its value at 25°C

Figure 13. Burst Mode Rising Threshold vs Temperature

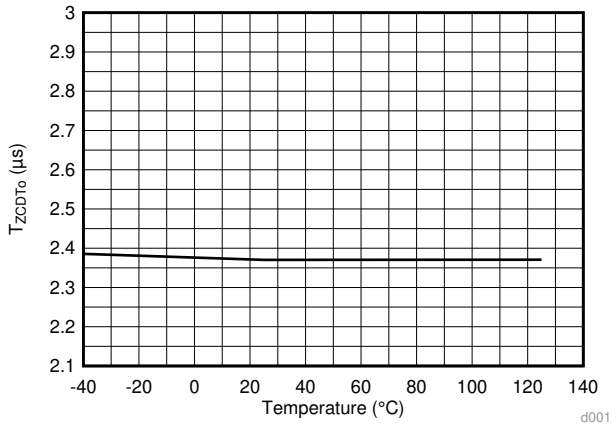
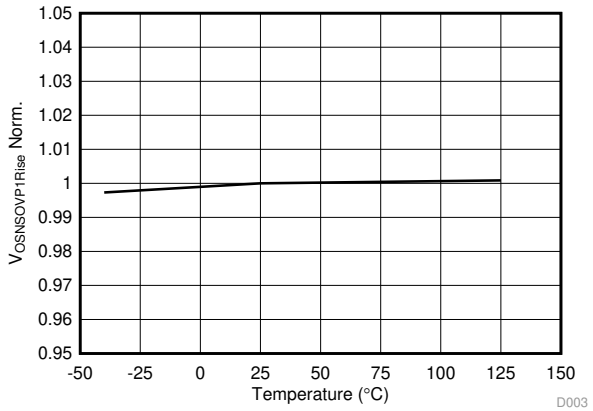
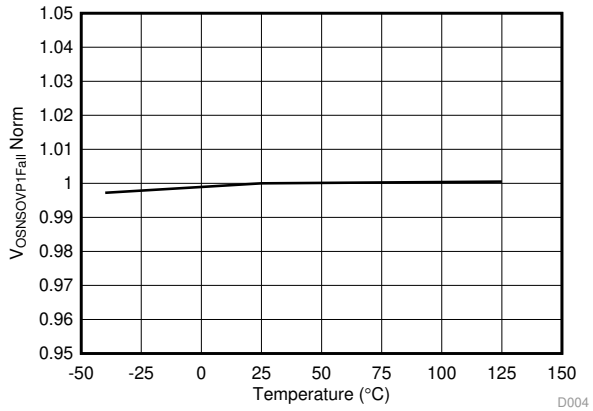


Figure 14. ZCD Timeout vs Temperature



It is Normalized respect its value at 25°C

Figure 15. VOSNS OVP1 Rising Threshold vs Temperature



It is Normalized respect its value at 25°C

Figure 16. VOSNS OVP1 Falling Threshold vs Temperature

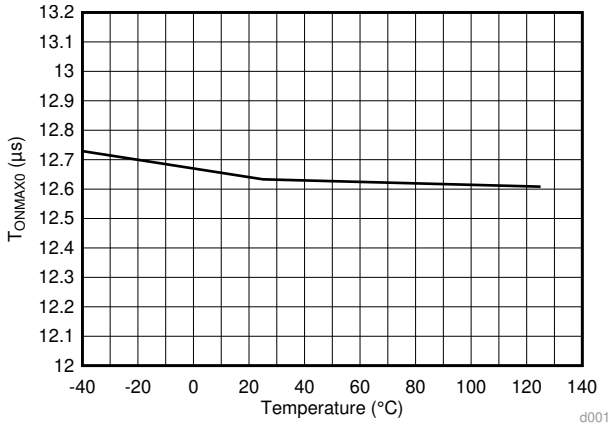


Figure 17. TON Max vs Temperature

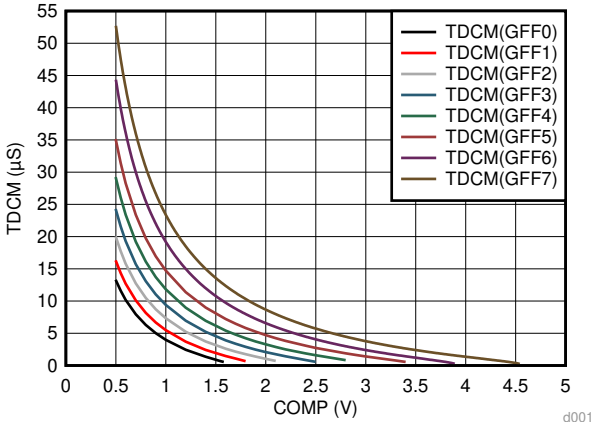


Figure 18. TDCM vs COMP Voltage

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8 Detailed Description

8.1 Overview

The UCC28056 controller followed with the UCC256403/4 LLC controller device to provide a complete PFC and LLC isolated off-Line power supply system. The combined power supply is designed to meet tough efficiency and standby power requirements without the need for an Auxiliary Flyback converter and with no need to switch off the PFC under light load conditions. It allows designers to meet modern green power standards with a simpler and lower system cost of power supply.

The controller contains a number of features designed to maximize operating efficiency across the entire range of Line and Load. A versatile CrM/DCM control algorithm allows UCC28056 to operate in transition mode at full power and then transition seamlessly into DCM at reduced load without compromising Line current harmonics or power factor. The controller operates at maximum frequency (Transition mode) when delivering full load and then automatically reduce switching frequency, moving to DCM operation, when delivering reduced load for maximum efficiency.

Light-load efficiency and standby power are further enhanced by transitioning automatically to a burst mode of operation when delivering less than 10% load for UCC28056C variants and 15% load for UCC28056A/B. During the burst OFF periods, the controller powers down most of its internal circuits to minimize controller power consumption.

The UCC28056 controller includes a comprehensive list of fault protection features such as cycle-by-cycle current limit, over-current protection, dual independent output over-voltage protection, Line Brown-In, Over-temperature protection and supply undervoltage lockout (UVLO).

Quantised 7-level line voltage feed-forward ensures that the loop gain is almost independent of line voltage, to ease design of the output voltage control loop. A non-linear error amplifier greatly improves the response to large steps in load without compromising steady state Line current harmonics.

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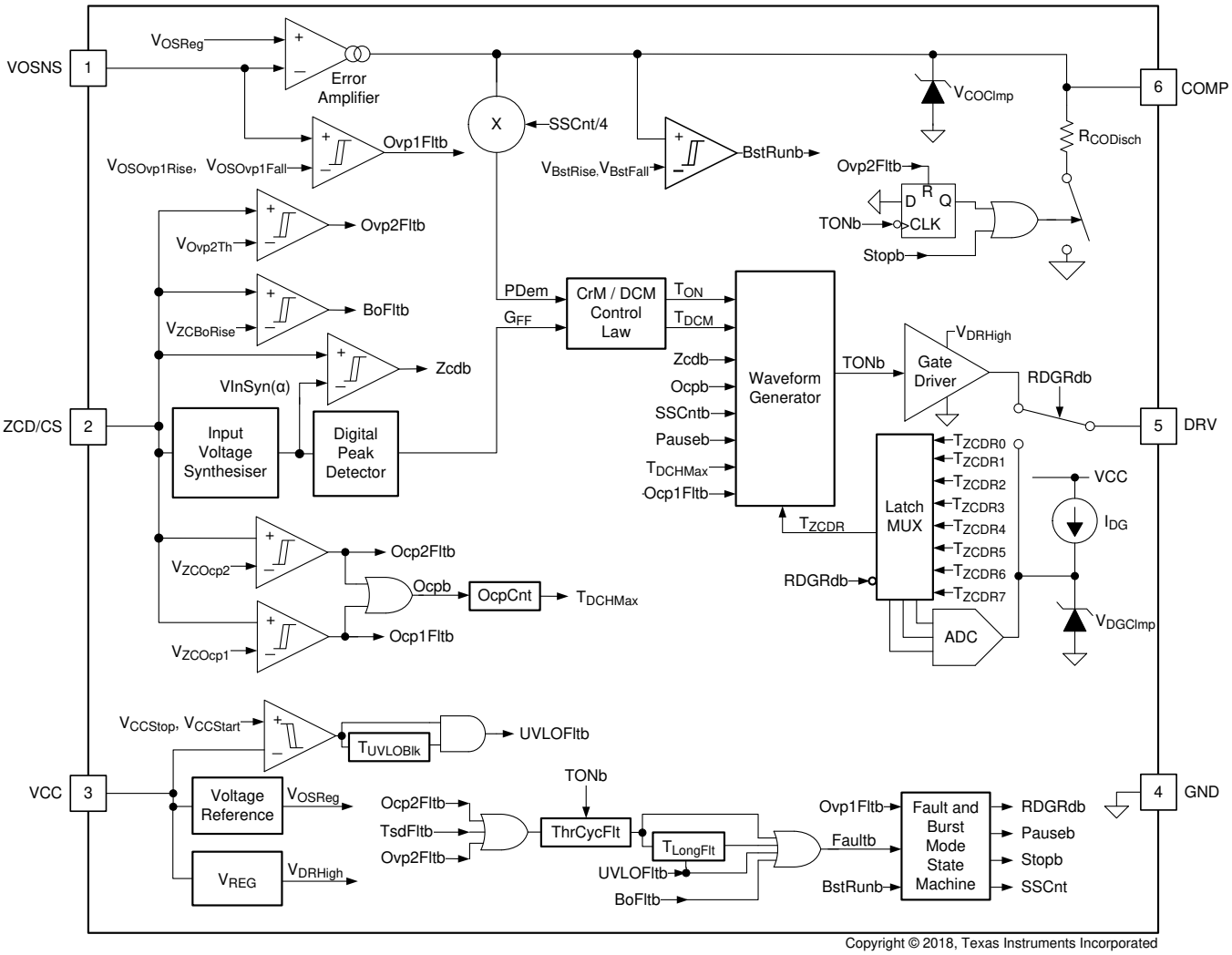
8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 CrM/DCM Control Principle

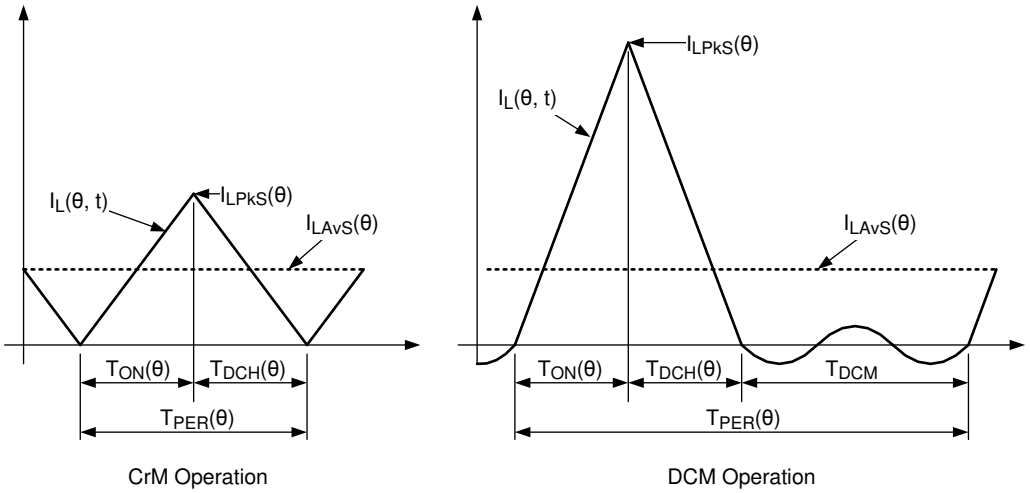

Figure 19. PFC Inductor Current Waveform for CrM and DCM Operation

Consider a single switching cycle that occurs at angle (θ) during the Line Cycle. Assuming ideal CrM operation the average inductor current ($I_{LAvS}(\theta)$) that flows during the switching cycle is given by:

$$I_{LAvS}(\theta) = \frac{I_{LPkS}(\theta)}{2} = V_{In}(\alpha) \times \frac{T_{ON}(\theta)}{2 \times L_{BST}} = \frac{V_{In}(\theta)}{R_{InEq}} \quad (1)$$

A fixed circuit has constant inductance (L_{BST}), so if the switch ON duration ($T_{ON}(\theta)$) holds constant (T_{ON}) , across the Line Cycle, then the average input current remains proportional to the input voltage. In other words, when controlled in this way, the Boost converter behaves as a resistive load (R_{InEq}) connected across the Line.

$$R_{InEq} = \frac{2 \times L_{BST}}{T_{ON}} \quad (2)$$

the next step is to consider DCM operation. Equation 3 describes the average inductor current that flows during the switching cycle.

$$I_{LAvS}(\theta) = \frac{I_{LPkS}(\theta)}{2} \times \frac{T_{ON}(\theta) + T_{DCH}(\theta)}{T_{PER}(\theta)} = V_{In}(\theta) \times \frac{T_{ON}(\theta) \times \delta_{ONDCH}(\theta)}{2 \times L_{BST}} = \frac{V_{In}(\theta)}{R_{InEq}} \quad (3)$$

To ensure average input current proportional to input voltage it is necessary for the on-time product $T_{ON}(\theta)$ x $\delta_{ONDCH}(\theta)$ is kept constant across the Line Cycle. Equation 4 shows the equivalent input resistance.

$$R_{InEq} = \frac{2 \times L_{BST}}{T_{ON} \times \delta_{ONDCH}} \quad (4)$$

The minimum effective input resistance ($R_{InEqMin}$) is needed to draw maximum power (P_{InMax}) from minimum Line voltage ($V_{InMinPkL}$):

$$P_{InMax} = \frac{V_{InMinPkL}}{2 \times R_{InEqMin}} \quad (5)$$

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Feature Description (continued)

Assume that full power operation at minimum Line operation is in CrM mode. Use Equation 6 to calculate the PFC inductor value required to deliver maximum power from minimum Line.

$$R_{InEqMin} = \frac{2 \times L_{BST}}{T_{ONMAX0}}$$

where

- T_{ONMAX0} is the maximum switch ON time (6)

Input power demand is an expression of the ratio of input power over maximum input power.

$$P_{Dem} = \frac{P_{In}}{P_{InMax}} = \frac{V_{InPkL}^{2}}{V_{InMinPkL}^{2}} \times \frac{R_{InEqMin}}{R_{InEq}} = \frac{V_{InPkL}^{2}}{V_{InMinPkL}^{2}} \times \frac{T_{ON}(\theta) \times \delta_{ONDCH}(\theta)}{T_{ONMAX0}} \quad (7)$$

Equation 8 rearranges Equation 7 to express $T_{ON}(\theta)$ time as a function of power demand.

$$T_{ON}(\theta) = P_{Dem} \times \frac{V_{InMinPkL}^{2}}{V_{InPkL}^{2}} \times T_{ONMAX0} \times \frac{1}{\delta_{ONDCH}(\theta)} = \frac{V_{CO}}{V_{COMax}} \times G_{FF} \times \frac{T_{ONMAX0}}{\delta_{ONDCH}(\theta)} \quad (8)$$

Equation 8 represents the CrM/DCM T_{ON} control principle implemented by UCC28056. This equation is quadratic in nature but UCC28056 employs the value of $\delta_{ONDCH}(\theta)$ from previous cycles as the basis for computing $T_{ON}(\theta)$ for the current cycle. The process is similar to solving an equation numerically by iteration.

A range of operating frequency options are available for CrM/DCM light-load operation. At one extreme, it can operate at high frequency with low current pulses in CrM mode (T_{DCM} = 0). At the other extreme it can operate, in DCM mode, at minimum frequency (T_{DCM} = T_{DCMMax}) with current pulses of maximum amplitude. The controller can select a T_{DCM} value anywhere between these two extremes. Conduction loss normally dominates when operating at minimum operating frequency leading to reduced efficiency. Switching loss normally dominates when operating at maximum operating frequency (CrM) also leading to reduced efficiency. Typically the most efficient operating frequency occurs when the pulse current amplitude is approximately one third of the maximum value.

$$\frac{I_{LPkSOpt}}{2 \times I_{LMaxPkL}} = \frac{1}{3.5} \quad (9)$$

$$I_{LMaxPkL} = \frac{V_{InMinPkL} \times T_{ONMAX0}}{2 \times L_{BST}} \quad (10)$$

The UCC28056 transitions from CrM to DCM operation when the peak inductor current across a Line Cycle drops below $I_{LPkSOpt}$. While in DCM operation it adjusts the switching frequency to ensure that the peak inductor current across a Line Cycle remains close to $I_{LPkSOpt}$ for all Line and Load conditions. In this way, UCC28056 attempts to maximize efficiency for all loads and for all Line voltages.

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Feature Description (continued)

8.3.2 Line Voltage Feed-Forward

The controller applies Line Voltage Feed-Forward to the COMP pin voltage (V_{CO}) before it computes the T_{ON} and T_{DCM} durations. This sequence ensures that COMP voltage represents input power regardless of Line voltage and ensures that Burst operation occurs at the same level of output power for all Line voltages. It also ensures fixed gain between the COMP pin voltage and input power simplifying compensation of the voltage control loop.

$$G_{FF} = \left(\frac{V_{InMinPkL}}{V_{InPkL}} \right)^2 \tag{11}$$

For ease of computation, UCC28056 employs seven discrete G_{FF} levels, the most appropriate value being selected by a series of comparators monitoring the peak input voltage level. Hysteresis is built into each comparator to avoid repetitive changes in the selected G_{FF} value and the step change in Line current that would result. The comparator thresholds and G_{FF} levels are selected to ensure that the demand to input power gain (P_{In}/V_{CO}) does not vary by more than ±20% over the full Universal Line voltage range (between 90 and 264 V_{RMS}).

8.3.2.1 Peak Line Voltage Detection

UCC28056 internally reconstructs the input voltage waveform for the purpose of Peak Line voltage sensing and Zero Current Detection (ZCD). In DCM or CrM mode the cycle average voltage across the Boost inductor must be zero. UCC28056 generates an internal representation of input voltage by extracting the Drain waveform from the ZCD/CS pin waveform and filtering it to extract the average Drain voltage across a switching cycle ($V_{InSyn}(\theta)$)

The digital peak detector selects the value of G_{FF} based upon the highest comparator threshold crossed over the period $T_{HLinMax}$. The switch to a higher G_{FF} value is implemented as soon as the corresponding threshold is crossed. The switch to a lower G_{FF} value is only implemented once the period $T_{HLinMax}$ expires and the peak detector has captured the Line voltage peak. The $T_{HLinMax}$ timer is not synchronized to the Line operating frequency.

Prior to the start of switching operation, at power - up or after a Burst - OFF period, the ZCD/CS pin voltage is sampled and used to select the appropriate starting G_{FF} level. This method assumes that the input rectifier and capacitor after the rectifier bridge have captured the peak Line voltage during the period of no switching.

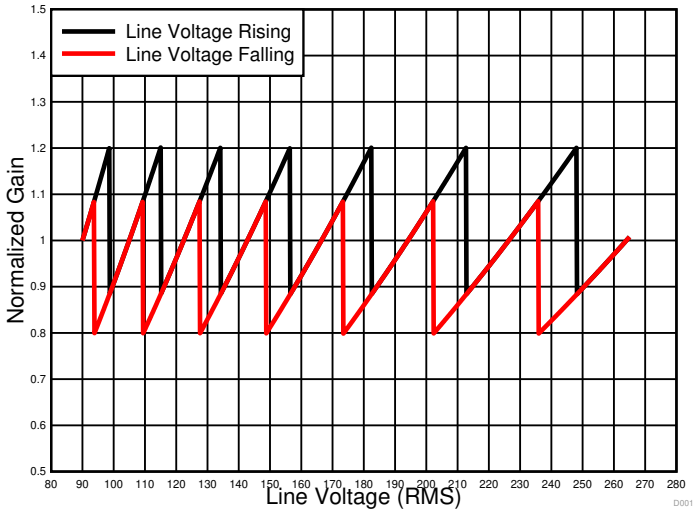

Figure 20. Normalized Gain vs Line Voltage

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Feature Description (continued)

8.3.3 Valley Switching and CrM/DCM Hysteresis

The UCC28056 controller achieves maximum efficiency enabling power switching operation when the drain voltage of the MOSFET is at a minimum (sometimes referred to as *valley*), of the resonance that occurs during the T_{DCM} period . Any energy stored in the Drain node capacitance (C_{DE}) dissipates in the power switch during its turnon transition time. Valley switching ensures minimum energy is stored in C_{DE} prior to the turnon period and hence minimum switching loss. After the T_{DCM} period, the controller waits for the next available valley on the drain voltage before initiating a new switching cycle. The actual T_{DCM} duration is therefore always an integer multiple of the drain resonance period. If the calculated T_{DCM} period extends over a valley boundary the actual T_{DCM} duration steps up in value by one resonant period. This step change in T_{DCM} duration causes a step change in Line current that rapidly decays as the $T_{ON}(\theta)$ computation iterates to a new solution to reflect the step change in T_{DCM} duration. Line current distortion, resulting from valley transitions, is kept to a minimum by computing the T_{DCM} duration from the COMP voltage. The COMP voltage varies little over the period of a Line cycle and hence the calculated T_{DCM} duration changes very little over the period of a Line cycle.

Line current distortion is particularly severe during the transition from the first valley (CrM) to the second valley (DCM) operation while the input voltage is low. In this region, the first valley duration is extended by the clamping action of the power switch body diode. In this region Line current is reduced when switching on the first valley, (CrM) , because the inductor current is negative at the start of the on period. The reduction in Line current is not observed for second or subsequent valley (DCM) operation because the inductor current starts the on period from zero. UCC28056 implements hysteresis in the T_{DCM} computation to virtually eliminate the possibility of repeated CrM/DCM transitions across a Line cycle. Such transitions can only occur if the twice Line frequency ripple on the COMP voltage is greater than 12% at the CrM/DCM boundary.

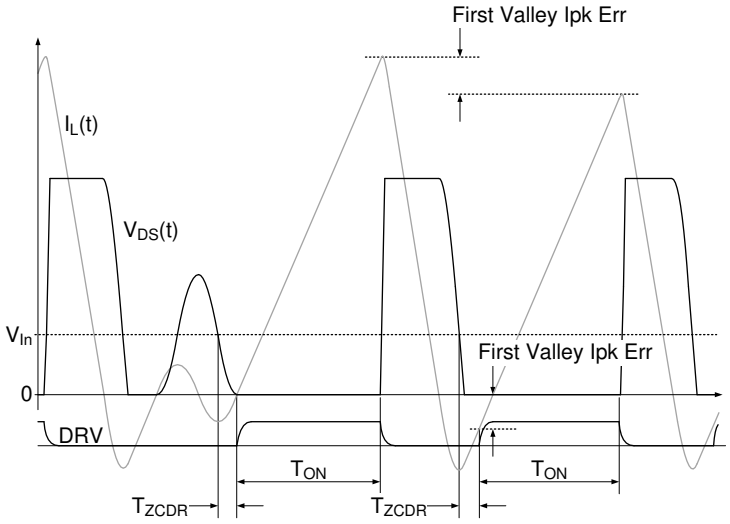

Figure 21. Drain Voltage and Inductor Current Transitioning from DCM to CrM

8.3.3.1 Valley Delay Adjustment

The UCC28056 delivers maximum efficiency when controlling power stages that have widely differing natural resonant frequencies. The application achieves this efficiency because the designer externally programs the delay between the ZcdVIn comparator crossing and the rising edge of DRV (T_{ZCDR}). Ideal valley switching for different power stage designs that may have very different natural resonant frequencies.

The T_{ZCDR} delay can be set to one of eight different values (T_{ZCDR0} – T_{ZCDR7}) by setting the value of a resistor (R_{DG}) connected externally between the DRV and GND pins. During the startup period or when recovering from a long fault, the controller transitions from the Stopb state to the RDGRdb state and then to the BstOffb state. While in the RDGRdb state, an internal current source (I_{DG}) transitions to the DRV pin. The the voltage that results from this current determines the appropriate T_{ZCDR} delay. The controller uses this delay period for all valley switching operation until a long fault causes the controller to return to the Stopb state.

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Feature Description (continued)

After entering its RDGRdb state, the controller waits for T_{DGSmpl} before reading the pin voltage. To ensure that the controller consistently detects the external resistance value correctly, do not allow the total external capacitance connected between the DRV and GND pins to exceed 12 nF.

8.3.4 Transconductance Amplifier with Transient Speed-up Function

The voltage error amplifier is a transconductance amplifier. Voltage loop compensation connects from the error amplifier output, COMP, to ground. The recommended type-2 compensation network is shown in . For loop-stability purposes, the controller calculates the compensation network values based on small-signal perturbations of the output voltage using the nominal transconductance gain g_M.

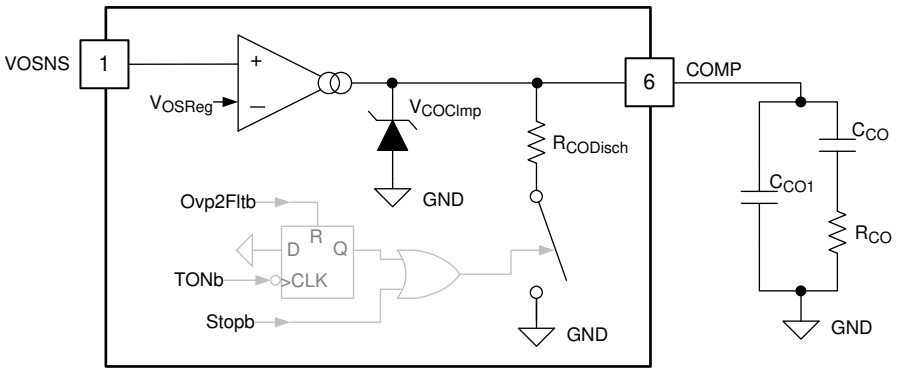

Figure 22. Transconductance Error Amplifier with Typical Compensation Network

To improve the transient response to large perturbations, the error amplifier gain increases by a factor of six times (6×) when the error amplifier input deviates more than ±3% from the nominal regulation voltage, V_{OSReg}. This increase allows faster charging and discharging of the compensation components to recover from step changes in load current.

8.3.5 Faults and Protections

The UCC28056 includes a comprehensive set of protection features to ensure safer and more robust operation during all operating conditions.

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Feature Description (continued)

8.3.5.1 Supply Undervoltage Lockout

Supply undervoltage lockout (UVLO) protection ensures that the controller operates only while the supply voltage is in a range that ensures correct operation and adequate Gate drive amplitude for the power switch.

The controller remains in a dormant state, consuming little I_{CC} current ($I_{CC_Startup}$), until the VCC pin voltage exceeds $V_{CCStart}$. Once $V_{CCStart}$ is exceeded, the controller wakes into its Stopb state. After waking, the controller proceeds with its normal start-up process.

The controller stops switching if the VCC pin voltage falls below V_{CCStop} for a longer period than $T_{UVLOBlk}$. The controller then returns to a dormant condition. During this dormant period, the controller consumes a relatively small amount of supply current (I_{CC}) until it exceeds the $V_{CCStart}$ threshold again.

8.3.5.2 Two Level Over-Current Protection

The UCC28056 controller includes two overcurrent protection mechanisms to deliver safe robust protection without danger of false tripping during operating transients. During the ON period of the switch, a current sense resistor (R_{CS}) connected in the source lead of the power switch senses the inductor current. The ZCD/CS pin detects the voltage across the current sense resistor. Equation 12 dscribes the current sense voltage signal applied to the ZCD/CS pin. Typically the second term in the bracket is much smaller than current sense resitance value (R_{CS}) and can be neglected.

$$V_{ZC}(t) = I_L(t) \times \left(R_{CS} + R_{DSON} \times \frac{R_{ZC2}}{R_{ZC1} + R_{ZC2}} \right) \approx I_L(t) \times R_{CS} \tag{12}$$

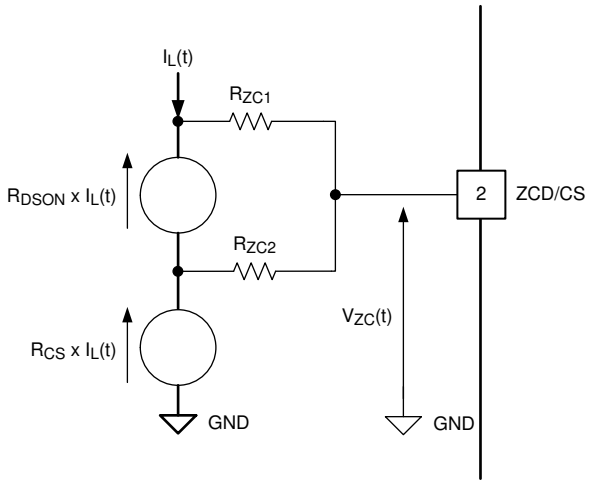

Figure 23. Equivalent Circuit of External Current Sense Network

8.3.5.2.1 Cycle-by-Cycle Current Limit Ocp1

Cycle-by-cycle peak current protection (Ocp1) terminates the on-time (T_{ON}) duration early if the current sense voltage rises above 0.5 V. This current protection method limits the peak inductor current, thus avoiding inductor saturation or damage to the power stage. When cycle-by-cycle current limit is active, it impacts Line current distortion, but in all other respects normal switching operation continues and the controller maintains output regulation.

The controller applies leading edge blanking to the current sense voltage signal. This application ensures that the leading edge current spike caused by discharging C_{DE} does not cause the Ocp1 comparator to terminate the DRV pulse too early.

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Feature Description (continued)

8.3.5.2.2 Ocp2 Gross Over-Current or CCM Protection

A second comparator (Ocp2) with a higher threshold, and shorter blanking time, also monitors the current sense voltage signal. If triggered, this second Ocp2 comparator also terminates the current on-time (T_{ON}) duration early. In addition, if the controller triggers the Ocp2 comparator on three consecutive switching cycles, it also triggers a long fault. The long fault halts switching operation and prevents restart for a period $T_{LongFlt}$. After this delay, the controller proceeds with its normal start-up process. In all transient or mild fault conditions the Ocp1 comparator, with its lower threshold, triggers first and prevents the Ocp2 comparator from acting. The Ocp2 comparator acts only if there is a gross fault such as a shorted output capacitor or bypass diode.

Under some fault conditions, including output overload, inductor current may become continuous because the reset voltage is low. In this case even the relatively short Ocp1 blanking time may allow the inductor current to continue ramping up. The UCC28056 controller addresses this condition by reducing the switching frequency to allow a longer period for the inductor current to ramp down between on-time pulses.

The maximum allowed diode conduction period (T_{DCHMax}) is doubled in the sequence (250 µs, 500 µs, 1000 µs) each time the on-time duration terminates early by either one of the OCP comparators. If there is no ZCD signal to indicate that the inductor current has fallen to zero, then the T_{DCHMax} interval must expire before the next switching cycle so the switching frequency is halved. The T_{DCHMax} period is halved to reverse the sequence each time the on-time period does not terminate early by one of the OCP comparators to restore the switching frequency. If the ZCD signal indicates that inductor current has reached zero, then T_{DCHMax} has no effect and normal operation resumes automatically.

8.3.5.3 Output Over-Voltage Protection

The UCC28056 controller provides two independent forms of output over-voltage protections. This is done to ensure that no single fault can result in excessive output voltage.

8.3.5.3.1 First Level Output Over-Voltage Protection (Ovp1)

The VOSNS pin monitors output capacitor voltage via an external resistor divider comprising R_{OS1} and R_{OS2}. An internal comparator (Ovp1) monitors the VOSNS pin voltage (V_{OS}). If the voltage on this pin rises above $V_{Ovp1Rise}$, indicating excessive output capacitor voltage, then the controller transitions to its BstOffb state. In this state switching halts to prevent further increase in the output capacitor voltage. The controller returns to the Runb state, and resumes switching operation, only after V_{OS} falls below $V_{Ovp1Fall}$, indicating that the output voltage has returned to normal range. To limit audible noise, the on-time pulse duration ramps during the transition between Runb and BstOffb states. This ramp method is identical to that for Burst Mode operation.

8.3.5.3.2 Second Level Over-Voltage Protection (Ovp2)

During the T_{DCH} period when the Boost diode is conducting, (and neglecting impedance in series with the Boost diode) the voltage across the MOSFET approximates to the output voltage. The controller monitors the voltage across the MOSFET via an external divider network connected to the ZCD/CS pin. This monitoring provides a second independent method to detect excessive output voltage in case the VOSNS pin divider becomes damaged. An Ovp2 comparator with a fixed threshold (V_{Ovp2Th}) monitors the ZCD/CS pin voltage during the T_{DCH} period. A fixed blanking period ($T_{Ovp2Blk}$) is applied after the falling edge of the DRV waveform to ensure that the Ovp2 comparator is not tripped by inductive spikes on the leading edge of the Drain waveform.

The UCC28056 controller can operate with an in-rush limiting NTC resistor located on the load side of the Boost MOSFET. Placing the NTC resistor in this location allows the use of a smaller controller with reduced current rating and delivers better efficiency. The voltage drop across the series resistance introduced by the NTC, particularly when cold, causes a voltage drop across the Boost MOSFET that is higher than the output voltage, for example during the early part of the T_{DCH} period when the current flowing through the Boost diode and NTC resistor is highest. The excess voltage across the Boost MOSFET caused by a cold NTC has two important consequences:

- It may cause the Ovp2 comparator to be tripped when the output voltage is not excessive.
- Excessive voltage stress applied to the Boost MOSFET, during a cold start, may cause it to be damaged.

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Feature Description (continued)

The UCC28056 triggers an Ovp2 fault if the time between the falling edge of the Ovp2 comparator output and the Zcdb signal is less than T_{Ovp2En} for three consecutive switching cycles. The series impedance required to trigger a false Ovp2 fault is greatly increased because the Ovp2 comparator must be tripped close to the Zcdb point when the current flowing through the NTC resistor is small.

An internal discharge resistor ($R_{CODisch}$) between the COMP and GND pins connected for each switching cycle causes the Ovp2 comparator to trip. This internal resistance discharges the external compensation network reducing power demand and therefore the peak current flowing through the NTC resistor. The internal COMP discharge resistor remains connected for any switching cycle that triggers the Ovp2 comparator. The internal COMP discharge resistor becomes disconnected after the first switching cycle that does not trigger the Ovp2 comparator. By limiting the peak current flowing through the cold NTC resistor, the effect of this circuit is to limit the peak voltage stress applied to the Boost MOSFET during a cold start.

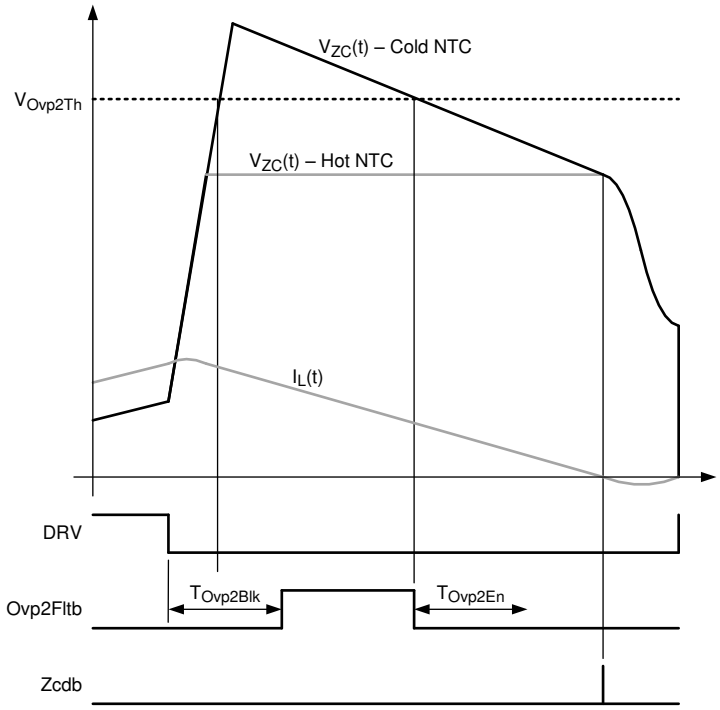

Figure 24. Waveforms to Illustrate Ovp2 Operation

8.3.5.4 Thermal Shutdown Protection

The controller includes an internal temperature sensor. During the switching period, the controller triggers a Thermal ShutDown (TSD) fault if the internal silicon temperature exceeds $T_{TSDRise}$ for three consecutive switching cycles. The TSD fault halts switching operation and causes the controller to transition to its Stopb state for a period $T_{LongFlt}$. After this delay the controller continues the normal start-up process.

The controller does not exit the Stopb state to begin switching operation while the internal silicon temperature is above $T_{TSDFall}$.

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Feature Description (continued)

8.3.5.5 Line Under-Voltage or Brown-In

The input rectifier and capacitor form an analog peak detector that accumulates the peak Line voltage applied to the input. This peak Line voltage appears across the Boost MOSFET. The controller observes peak Line voltage via the external divider network attached to the ZCD/CS pin. The Line voltage start comparator does not allow the controller to exit the Stopb state until the ZCD/CS pin voltage rises above the $V_{ZCBoRise}$ threshold. This behavior ensures that switching operation does not start until the Line voltage is high enough (85 V_{RMS}) to deliver full output power. During switching operation, the controller continues to operate regardless of the Line voltage, until a fault causes it to enter a Stopb state.

8.3.6 High-Current Driver

An integrated, high-current driver allows the UCC28056 controller to drive the power MOSFET switch directly. The controller limits the voltage applied to the DRV pin to V_{DRHigh}. This limit enables a high VCC supply rail to drive the controller without exceeding the V_{GS} voltage rating of the power MOSFET. This limit also reduces power dissipation in the internal gate driver when the controller operates from a VCC rail that is higher than V_{DRHigh}.

The integrated driver is protected against temporary short circuit of the DRV and GND pins.

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8.4 Controller Functional Modes

8.4.1 Burst Mode Operation

The UCC28056 controller provides leading light-load efficiency and standby power by implementing Burst mode of operation with the following key features:

1. Power during burst is controlled to be approximately 11% of maximum output power for UCC28056/C and 16% of maximum power for UCC28056A/B for all Line voltage levels.
2. During the Burst OFF period, the current consumption of UCC28056 drops to less than 132 μA.
3. The T_{ON} pulse width is ramped up over the first four cycles, and ramped down over the last four cycles of each Burst-on period. This Soft-ON/OFF scheme ramps the Line current at the edge of each Burst ON period to limit audible noise and disturbance of the EMI filter.

Two comparator thresholds applied to the COMP pin voltage provide Burst Mode Operation. Switching halts after four soft-OFF cycles when the COMP pin voltage falls below the $V_{BstFall}$ threshold. Switching resumes with four Soft-ON cycles, when the COMP pin voltage rises above the $V_{BstRise}$ threshold. The average voltage of these two thresholds represents approximately 11% $V_{COMax}$for UCC28056/C and 16% V_{COMax} for UCC28056A/B. The power delivered during Burst ON is approximately 11% of maximum input power for UCC28056/C.

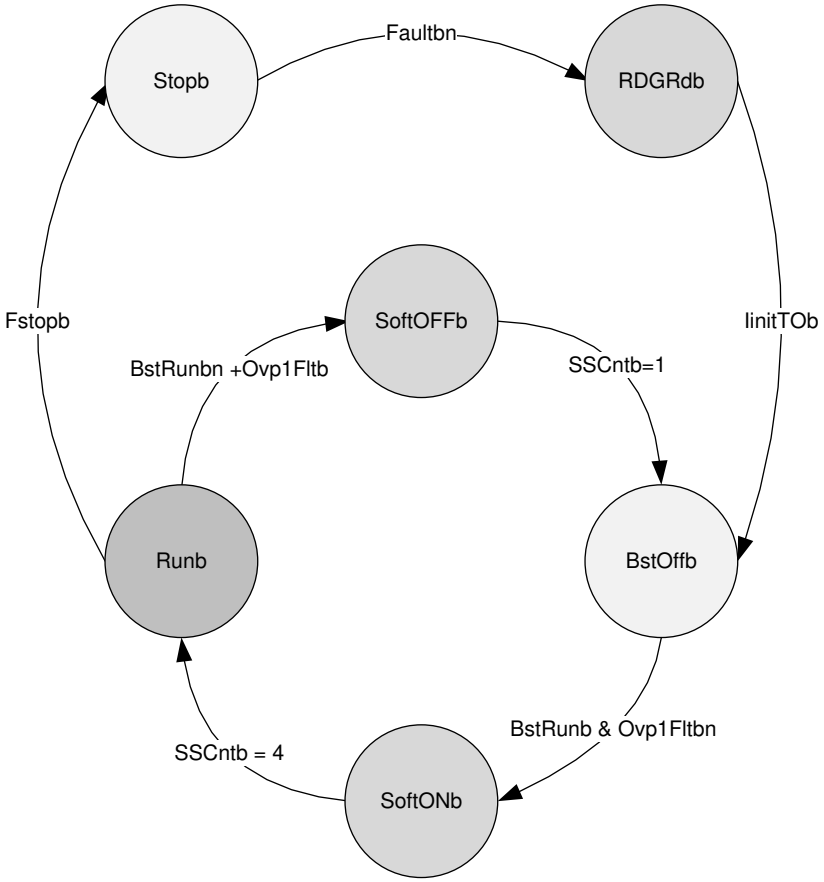

Figure 25. Fault and Burst Mode State Diagram

8.4.2 Soft Start

During Stopb state operation, an internal resistor ($R_{CODisch}$) is connected between the COMP and GND pins to discharge the external compensation network. Start-up transitions through the BstOffb state and switching commence only after the COMP pin voltage rises above the $V_{BstRise}$ threshold. Switching therefore always starts with the power demand at 12.5% of its maximum value. The Soft-ON feature ensures that the on-time period ramps up over the first four switching cycles to the demanded value. These features limit audible noise at start-up.

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Controller Functional Modes (continued)

Because the controller enables the error amplifier fast transient gain a startup, the input power ramps to maximum at a rate limited only by the time constant of the external compensation network. This condition ensures that the output capacitance charges rapidly to limit start-up delay.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC28056 controller can be used in a wide range of applications in which a PFC stage is needed. This design example demonstrates the features of the controller.

- EVM hardware
- Excel design calculator

9.2 Typical Application

Figure 26 shows a typical application of the UCC28056 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts

- the control circuit centering on the UCC28056
- the power section

The power section is a Boost converter, with the inductor operating in Transition Mode (TM/CrM) or Discontinuous Mode (DCM) according to Line and Load.

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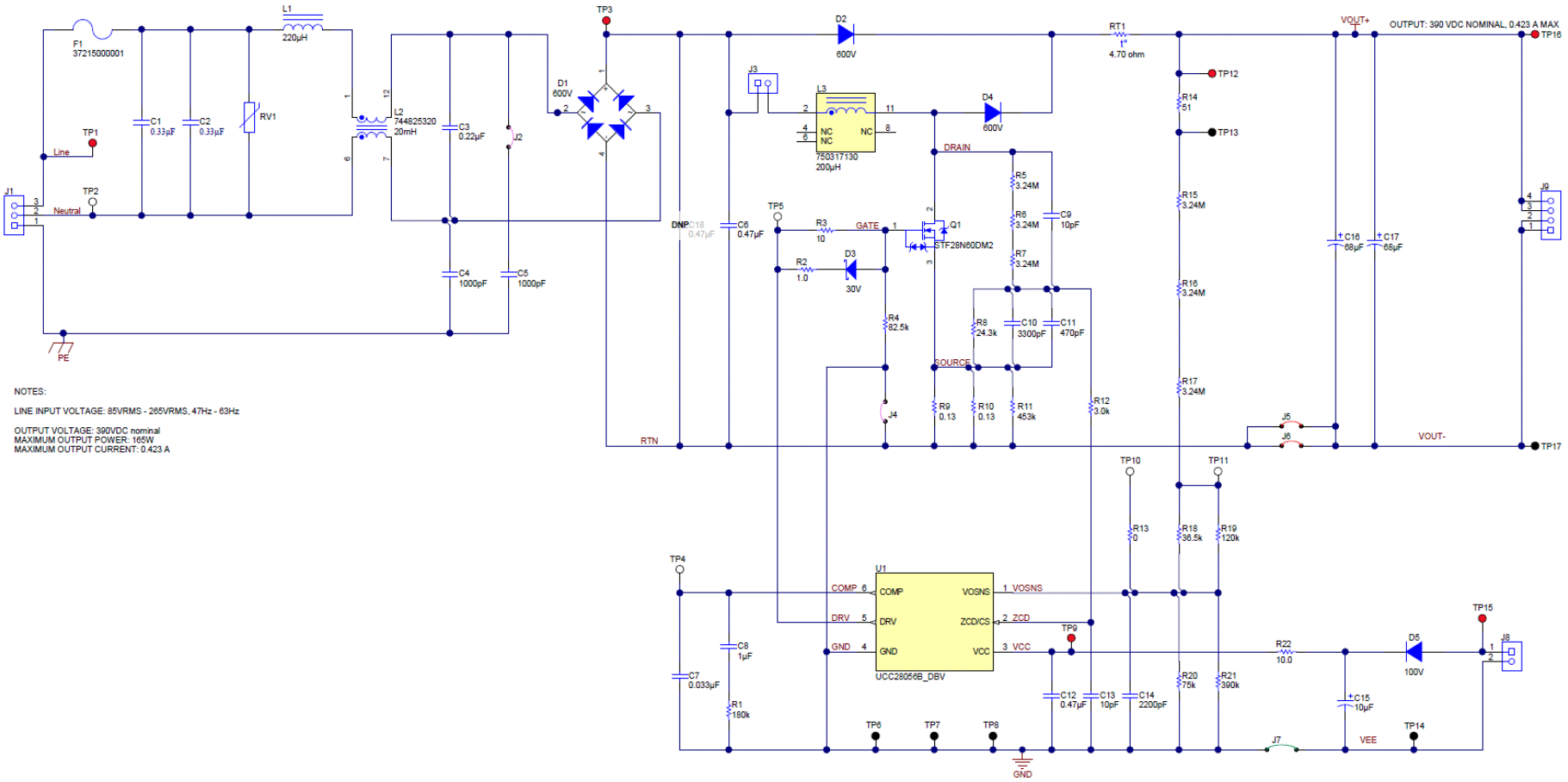

NOTES:

LINE INPUT VOLTAGE: 85VRMS - 265VRMS, 47Hz - 63Hz

OUTPUT VOLTAGE: 390VDC nominal
MAXIMUM OUTPUT POWER: 165W
MAXIMUM OUTPUT CURRENT: 0.423 A

Figure 26. Typical Application Circuit for 165-W Pre-Regulator

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9.2.1 Design Requirements

For this design example, use the parameters listed in the table below as the input parameters.

Table 1. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
AC Voltage range		85		265	VAC
AC Voltage frequency		47		63	Hz
OUTPUT CHARACTERISTICS					
Output Power, P_{OutMax}	85 VAC to 265 VAC			165	W

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28056 controller with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters (efficiency, footprint,cost) using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Power Stage Design

The first step in the power stage design is to calculate the PFC inductor value needed to achieve the specification, then the ratings for all other power components can be computed.

9.2.2.2.1 Boost Inductor Design

The minimum equivalent resistance presented, to the Line, by the input of the Boost PFC stage changes according to the current Line Feed-Forward setting. $R_{InEqMin0}$ and $R_{InEqMin1}$ present the minimum equivalent input resistance for the first two Line Feed-Forward levels.

$$R_{InEqMin0} = \frac{2 \times L_{BST}}{T_{ONMAX0}} \tag{13}$$

$$R_{InEqMin1} = \frac{2 \times L_{BST}}{T_{ONMAX0} \times G_{FF1}} \tag{14}$$

Equation 15 calculates the maximum input power that can be drawn from a given Line voltage. The maximum input power is set to 110% of P_{OutMax} to account for power stage efficiency.

$$P_{InMax} = \frac{V_{InRMSMin}^{2}}{R_{InEqMin}} = 110\% \times P_{OutMax} \tag{15}$$

Equation 16 calculates the Boost inductance value required to ensure that maximum load can be delivered from minimum Line voltage.

$$L_{BST0} = \frac{V_{InRMSMin}^{2}}{110\% \times P_{OutMax}} \times \frac{T_{ONMAX0}}{2} = 255\ \mu H \tag{16}$$

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Ensure that P_{OutMax} can be delivered from the lowest Line voltage for G_{FF1}. Use Equation 17 to calculate the required Boost inductor value .

$$L_{BST1} = \frac{(K_{ZC} \times V_{FF0Fall})^2}{110\% \times 2 \times P_{OutMax}} \times \frac{T_{ONMAX0} \times G_{FF1}}{2} = 235\ \mu H \quad (17)$$

Choose the lower of the two values calculated in Equation 16 and Equation 17 (L_{BST0} and L_{BST1}). Using a smaller inductance value compromises light load efficiency. A larger inductance value cannot deliver the required maximum load power (P_{OutMax}) across the required range of Line voltage.

Choose a Boost inductor value of 200 µH, considering a tolerance of 10%. In order to deliver maximum load power the inductor must be able to operate with a peak current that is greater than both I_{LPk0} and I_{LPk1}

$$L_{BST} = 200\ \mu H \quad (18)$$

$$I_{LPk0} = \frac{V_{InRMSMin} \times \sqrt{2} \times T_{ONMAX0}}{L_{BST}} = 7.69\ A \quad (19)$$

$$I_{LPk1} = \frac{K_{ZC} \times V_{FF0Fall} \times T_{ONMAX0} \times G_{FF1}}{L_{BST}} = 6.24\ A \quad (20)$$

$$I_{LPk} = I_{LPk0} = 7.69\ A \quad (21)$$

Use Equation 22 to calculate a current sense resistance that ensures the required peak inductor current (I_{LPk}) does not cause early termination of the T_{ON} period.

$$R_{CS} = \frac{V_{ZCOcp1Min}}{I_{LPk}} = 0.06\ \Omega \quad (22)$$

Achieve this amount of resistance by connecting three resistors in parallel.

$$R_{CS} = \frac{1}{\frac{2}{0.125\ \Omega} + \frac{1}{3\ \Omega}} = 0.062\ \Omega \quad (23)$$

Use Equation 24 to calculate an inductance value that allows a saturation current above the maximum Ocp1 current limit value.

$$I_{LSat} = \frac{V_{ZCOcp1Max}}{R_{CS}} = 8.8\ A \quad (24)$$

Maximum current in the power components flows while delivering maximum load when supplied from minimum Line voltage. In this condition, the UCC28056 controller always operates in transition mode (CrM). shows the inductor current waveforms for ideal CrM operation.

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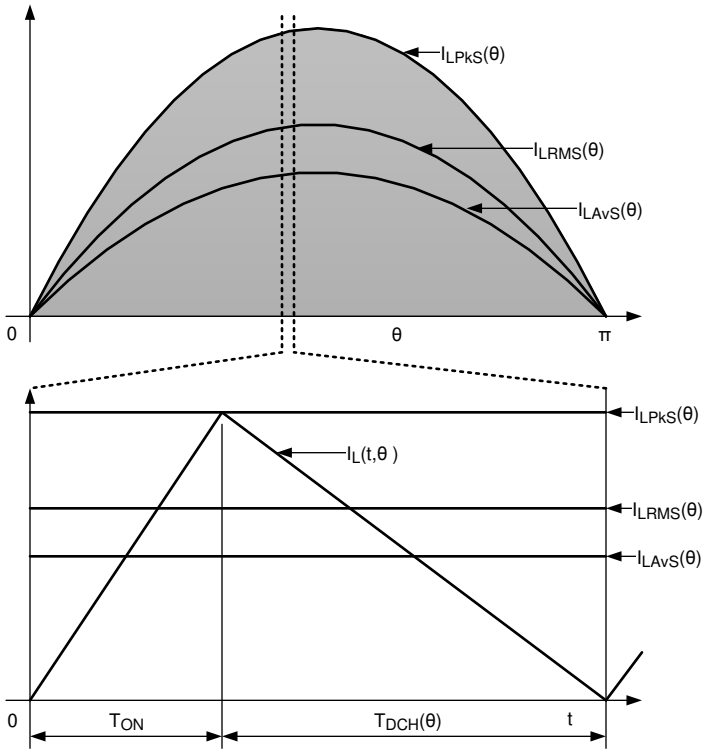

Figure 27. Ideal Transition Mode (CrM) Inductor Current

Equation 25 describes the he Boost inductor RMS current over a single switching cycle, at angle θ through the Line half-cycle.

$$I_{LRMS}(\theta) = \frac{I_{LPkS}(\theta)}{\sqrt{3}} = \frac{2 \times I_{LAvS}(\theta)}{\sqrt{3}} = \frac{2}{\sqrt{3}} \times \frac{V_{InPkL}}{R_{InEqMin}} \times \sin(\theta) \quad (25)$$

Equation 26 describes the Boost inductor RMS current over a complete Line cycle.

$$I_{LRMS} = \sqrt{\frac{1}{\pi} \times \int_{0}^{\pi} I_{LRMS}(\theta)^2 \, d\theta} = \frac{2}{\sqrt{3}} \times \frac{V_{InRMS}}{R_{InEq}} \quad (26)$$

Maximum Boost inductor RMS current occurs at minimum Line voltage and maximum input power.

$$I_{LRMSMax} = \frac{2}{\sqrt{3}} \times \frac{110\% \times P_{OutMax}}{V_{InRMSMin}} = 2.5 \text{ A} \quad (27)$$

Based upon the inductor requirements, a custom magnetic can be designed, or a suitable catalogue controller selected.

Table 2. Inductor Requirements

Description	Value	Unit
Inductance	200	µH
RMS Current	2.5	A
Saturation Current	8.8	A

9.2.2.2.2 Boost Switch Selection

The power switch carries the Boost inductor current during its ON period (T_{ON}). It carries no current during its OFF period (T_{DCH}). Equation 28 describes the switch RMS current, over a single switching cycle, at angle θ in the Line half-cycle.

$$I_{MosRMS}(\theta) = I_{LPkS}(\theta) \times \sqrt{\frac{\delta_{Mos}(\theta)}{3}} = 2 \times \frac{V_{InPkL}}{R_{InEq}} \times \sin(\theta) \times \sqrt{\frac{\delta_{Mos}(\theta)}{3}} \quad (28)$$

Equation 29 describes the duty cycle of switch conduction for ideal transition mode (CrM) operation.

$$\delta_{Mos}(\theta) = \frac{T_{ON}}{T_{ON} + T_{DCH}(\theta)} \quad (29)$$

The switch ON time is constant across the Line cycle but the OFF time varies according to the position in the Line cycle. Volt-second balance across the Boost inductor, within each switching cycle, requires that.

$$\frac{T_{DCH}(\theta)}{T_{ON}} = \frac{|V_{In}(\theta)|}{V_{Out} - |V_{In}(\theta)|} \quad (30)$$

Equation 31 calculates the duty cycle of switch conduction.

$$\delta_{Mos}(\theta) = 1 - \sqrt{2} \times \frac{V_{InRMS}}{V_{Out}} \times |\sin(\theta)| \quad (31)$$

Equation 32 describes the RMS switch current across a complete Line half-cycle.

$$I_{MosRMS} = \sqrt{\frac{1}{\pi} \times \int_0^{\pi} I_{MosRMS}(\theta)^2 \, d\theta} = \frac{V_{InRMS}}{R_{InEq}} \times \sqrt{\frac{4}{3} - \frac{32 \times \sqrt{2} \times V_{InRMS}}{9 \times \pi \times V_{Out}}} \quad (32)$$

Maximum RMS current in the switch occurs at maximum load and minimum Line.

$$I_{MosRMSMax} = \frac{110\% \times P_{OutMax}}{V_{InRMSMin}} \times \sqrt{\frac{4}{3} - \frac{32 \times \sqrt{2} \times V_{InRMSMin}}{9 \times \pi \times V_{Out}}} = 2.1\ A \quad (33)$$

Use the following guidelines for MOSFET selection for the Boost switch.

- The voltage rating must be greater than the maximum output voltage. Under transient or Line surge testing the output voltage may exceed the normal regulation level. For this design example, the MOSFET voltage rating is 650 V supports a regulated output voltage of 390 V.
- Based upon an acceptable level of conduction loss in the MOSFET, the required on-resistance ($r_{DS(on)}$) value can be calculated from the maximum RMS current. For this example design an STF24N60DM2 MOSFET, from STMicrolelectronics was selected with an on-resistance of 0.37 Ω, when T_J = 125°C which allows maximum conduction power loss (less than 1.7 W) in the MOSFET.
- For best efficiency, use a MOSFET that incorporates a fast body diode. Operation using discontinuous inductor current (DCM) from a low input voltage incurs additional switching power loss if a MOSFET with slow body diode is used.

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9.2.2.2.3 Boost Diode Selection

The Boost diode carries the Boost inductor current while the switch is OFF (T_{DCH}), and carries zero current while the switch is ON (T_{ON}). Equation 34 calculates The RMS diode current over a single switching cycle, at angle θ in the Line half-cycle .

$$I_{DioRMS}(\theta) = I_{LPkS}(\theta) \times \sqrt{\frac{\delta_{Dio}(\theta)}{3}} = 2 \times \frac{V_{InPkL}}{R_{InEq}} \times \sin(\theta) \times \sqrt{\frac{\delta_{Dio}(\theta)}{3}} \tag{34}$$

Equation 35 describes the duty cycle of Boost diode conduction for ideal transition mode operation .

$$\delta_{Dio}(\theta) = 1 - \delta_{Mos}(\theta) = \sqrt{2} \times \frac{V_{InRMS}}{V_{Out}} \times \left|\sin(\theta)\right| \tag{35}$$

Equation 36 describes the RMS Boost diode current across a complete Line half-cycle .

$$I_{DioRMS} = \sqrt{\frac{1}{\pi} \times \int_0^{\pi} I_{DioRMS}(\theta)^2 \, d\theta} = \frac{4}{3} \times \frac{V_{InRMS}}{R_{InEq}} \times \sqrt{\frac{2 \times \sqrt{2}}{\pi} \times \frac{V_{InRMS}}{V_{Out}}} \tag{36}$$

The maximum RMS current in the Boost diode occurs at maximum load and minimum Line.

$$I_{DioRMSMax} = \frac{4}{3} \times \frac{110\% \times P_{OutMax}}{V_{InRMSMin}} \times \sqrt{\frac{2 \times \sqrt{2}}{\pi} \times \frac{V_{InRMSMin}}{V_{Out}}} = 1.3 \text{ A} \tag{37}$$

Conduction power loss in the Boost diode is primarily a function of the average output current.

$$I_{DioAVGMax} = \frac{P_{OutMax}}{V_{Out}} = 0.42 \text{ A} \tag{38}$$

Use the previous calculations and these guidelines to select the Boost diode:

- Ensure that the Boost diode voltage rating exceeds the maximum output voltage. Under transient or Line surge testing the output voltage may rise far above its normal regulation level.
- The Boost diode must have average and RMS current ratings that are higher than the numbers calculated by Equation 37 and Equation 38.
- Diodes are available with a range of different speed/recovery charge. Fast diodes, with low reverse recovery charge, typically have higher forward voltage drop. Fast diodes have higher conduction loss but lower switching loss. Slow diodes, with high reverse recovery charge, typically have lower forward voltage drop. Slow diodes have lower conduction loss but higher switching loss. Ensure maximum efficiency by matching the diode speed rating to the application.
- When Line voltage is first applied, to the Boost converter input, an uncontrolled current flows through the Boost diode while the output capacitor charges to the Line voltage peak level. The charging current is limited only by the impedance of the Line and EMI filter stage, and may reach a very high magnitude during the output capacitor charging period. Any diode carrying this current must be rated to carry this non-repetative surge current. It is normal practice to add a bypass diode to divert most of this charging current away from the Boost diode. The bypass diode can be a slow type with lower forward voltage drop. It is therefore cheaper and more robust than the faster Boost diode.
- For this example design the STTH5L06 diode from STMicroelectronics® was selected. This diode has a voltage rating of 600 V and an average current rating of 5 A. It has a forward voltage drop of approximately 0.85 V giving a conduction loss in the Boost diode, of less than 0.5 W.

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9.2.2.2.4 Output Capacitor Selection

Power drawn by the PFC stage from the Line supply may be represented by the following expression.

$$P_{In}(\theta) = 2 \times V_{InRMS} \times I_{InRMS} \times \sin(\theta)^2 \tag{39}$$

Assuming a typical application, with constant load power, for some parts of the Line cycle excess power is drawn from the supply and stored in the output capacitor. In other parts of the Line cycle load power exceeds input power and this deficit must be supplied from the output capacitor. This process of energy transfer to an from the output capacitor necessarily results in twice Line frequency output voltage ripple. The amplitude of this twice Line frequency ripple depends only upon the ratio P_{Out}/C_{Out} and the Line frequency.

$$\Delta V_{Outpp} = \frac{P_{Out}}{C_{Out}} \times \frac{1}{2 \times \pi \times f_{Line} \times V_{OutReg}} \tag{40}$$

Choose an output capacitor value by prioritizing one of a number of application requirements:

- Twice Line frequency output ripple voltage at maximum load.
- Output voltage hold-up time after the Line supply has been disconnected.
- Output voltage deviation as a result of a transient load step.

For this design example assume that the twice Line frequency output ripple voltage amplitude is less than 3% of its regulation level. The P_{OutMax}/C_{Out} ratio required to achieve this can be calculated using Equation 41

$$\frac{P_{OutMax}}{C_{Out}} \geq \left(2 \times \pi \times f_{Line} \times {V_{OutReg}}^2 \times 3\%\right) = 1.43 \frac{W}{\mu F} \tag{41}$$

Use Equation 42 to calculate the required capacitance value for this 165-W example design.

$$C_{Out} \geq \frac{165W}{1.43 \frac{W}{\mu F}} = 115\ \mu F \tag{42}$$

For best Line current total harmonic distortion (THD), the maximum output voltage ripple amplitude must satisfy the condition presented in Equation 43. Satisfying this condition ensures that the error amplifier non-linear gain does not activate due to extremes of the output voltage ripple.

$$\frac{\Delta V_{Outpp}}{V_{OutReg}} = \frac{2 \times DSuThs}{V_{OSReg}} = 5.4\% \tag{43}$$

Use Equation 44 to calculate the maximum RMS ripple current flowing in the output capacitor.

$$I_{COutRMSMax} = \sqrt{{I_{DioRMSMax}}^2 - \left(\frac{P_{OutMax}}{V_{OutReg}}\right)^2} = 1.19\ A \tag{44}$$

This current flowing into the output capacitor includes a switching frequency component ($I_{COutRMSHF}$) and a twice Line frequency ripple component ($I_{COutRMSLF}$).

$$I_{COutRMSLF} = \frac{1}{\sqrt{2}} \times \frac{P_{OutMax}}{V_{OutReg}} = 0.3\ A \tag{45}$$

$$I_{COutRMSHF} = \sqrt{{I_{DioRMSMax}}^2 - \frac{3}{2} \times \left(\frac{P_{OutMax}}{V_{OutReg}}\right)^2} = 1.15\ A \tag{46}$$

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Electrolytic capacitors typically have a ripple current rating at twice Line frequency (120 Hz) and a different ripple current rating at switching frequency (100 kHz). These ratings reflect the fact that the capacitor ESR is higher at twice Line frequency and hence ripple current at this frequency leads to higher power loss than the same amplitude of switching frequency ripple. Consider the equivalent high-frequency ripple current flowing in the capacitor in order to select the correct capacitor.

$$I_{CEquRMSHF} = \sqrt{I_{COutRMSLF}^{2} \times K_{HLF}^{2} + I_{COutRMSHF}^{2}} \quad (47)$$

The parameter K_{HLF} is the ratio of high frequency to low frequency RMS ripple current rating for the particular capacitor series to be used.

$$K_{HLF} = \frac{100kHz_ripple_current_rating}{120Hz_ripple_current_rating} \quad (48)$$

In this example design, for reasons of size and rating, two 68-µF, 450 V capacitors are selected from Rubycon BXW series (450BXW68MEFC12.5X45), connected in parallel. In this way, both the capacitance value requirement and ripple current rating are met with some additional margin.

$$C_{Out} = 2 \times 68\ \mu F = 136\ \mu F \quad (49)$$

$$I_{CEquRMSHF} = \sqrt{(0.3\ A)^2 \times \left(\frac{1.525}{0.610}\right)^2 + (1.15\ A)^2} = 1.37\ A \quad (50)$$

9.2.2.3 ZCD/CS Pin

An external divider network attached to the ZCD/CS pin transfers both the attenuated Drain voltage waveform (V_{DS}) and the current sense signal (V_{CS}) into the controller. This transfer is possible because the current sense signal requires observation only when the switch is ON and the V_{DS} signal is close to zero. While the Drain voltage waveform requires sensing only when the switch is OFF and the current sense signal is close to zero.

$$V_{ZC}(t) = V_{CS}(t) + V_{DS}(t) \times \frac{Z_{ZC2}}{Z_{ZC1} + Z_{ZC2}} \quad (51)$$

Equation 52 describes the attenuated Drain voltage during the on-time period when the MOSFET is switched ON.

$$V_{ZC}(t) = I_L(t) \times \left(R_{CS} + R_{DSON} \times \frac{Z_{ZC2}}{Z_{ZC1} + Z_{ZC2}}\right) \quad (52)$$

The ON state resistance of the MOSFET (R_{DSON}) typically has a similar value to the current sense resistor (R_{CS}). The attenuation of the divider (Z_{ZC1}, Z_{ZC2}) is 1/401 and hence the second term of Equation 52 may be neglected.

$$V_{ZC}(t) = I_L(t) \times R_{CS} \quad (53)$$

Hence the required current sense resistor value can be calculated from the maximum peak inductor current obtained in section 9.2.2.2.1

Outside the T_{ON} period, when the MOSFET is switched OFF, the current flowing through the current sense resistor is close to zero. In this case Equation 51 may be expressed as follows.

$$V_{ZC}(t) = V_{DS}(t) \times \frac{Z_{ZC2}}{Z_{ZC1} + Z_{ZC2}} \quad (54)$$

UCC28056 prevents the start of a new switching cycle until increasing negative slope is detected on the ZCD/CS pin voltage waveform. The increasing negative slope indicates that the inductor current has fallen to zero so the output diode is already OFF. Turn-ON switching loss is further reduced by synchronizing the start of each new switching cycle with a minimum, or valley, on the Drain waveform.

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In theory, a simple resistor divider can be used to attenuate the Drain voltage waveform fed into the ZCD/CS pin. In practice, the parasitic capacitance associated with the PCB traces and the ZCD/CS pin filter the attenuated signal and introduce phase shift. The resulting distortion and phase shift negatively impact the ability of the part to synchronize to the zero inductor current transitions. The problem is compounded by the need to limit power dissipation in the resistive divider, which dictates the use of high resistance values, and increased filtering of the attenuated signal.

Add a capacitor divider in parallel with the resistor divider in order to use of high value resistors without introducing filtering and associated phase shift. In this case, ensure that the reactive divider ratio is equal to the resistor divider ratio.

$$\frac{R_{ZC2}}{R_{ZC1} + R_{ZC2}} = \frac{X_{ZC2}}{X_{ZC1} + X_{ZC2}} \tag{55}$$

Hence:

$$\frac{R_{ZC1}}{R_{ZC2}} = \frac{C_{ZC2}}{C_{ZC1}} \tag{56}$$

There are number of internal voltage thresholds driven by the attenuated Drain voltage signal supplied to the ZCD/CS pin. These include Brown-Out ($V_{ZCBoRise}$), Line feed-forward ($V_{FFxRise}$, $V_{FFxFall}$) and second output over-voltage (V_{Ovp2Th}). The same external divider ratio (K_{ZC}) drives all of these thresholds. Scope to vary the attenuation ratio specified is limited because it impacts all of these thresholds in unison.

$$K_{ZC} = \frac{R_{ZC1}}{R_{ZC2}} + 1 = 401 \tag{57}$$

$$V_{InRMSBoRise} = V_{ZCBoRise} \times \frac{K_{ZC}}{\sqrt{2}} = 85.1\ V \tag{58}$$

The controller infers Line voltage from the switching cycle average voltage on the Drain node. Neglecting any resistive voltage drop in the Boost inductor this must be equal to the voltage supplied from the input rectifier, provided the Boost inductor current returns to zero at the end of each cycle (TM/CrM/DCM). Voltage drops in the input rectifier bridge and EMI filter stage cause an error between predicted and measured threshold values. An internal peak detector determines the peak input voltage across a Line half-cycle. Equation 58 above converts this peak value to an RMS quantity, but assumes an ideal sinusoidal Line supply

Equation 59 calculates the output voltage required to trigger the second output overvoltage comparator (Ovp2).

$$V_{OutOvp2} = V_{Ovp2Th} \times K_{ZC} = 451\ V \tag{59}$$

This parameter is observed via the Drain waveform, voltage drops in the Boost Diode and series NTC resistor, causes the Ovp2 comparator to trip at a lower output voltage level.

Power dissipation in the Drain sensing resistor divider chain reaches its highest value during the Burst OFF condition. During the Burst OFF condition, the Drain voltage approximates a DC voltage equal to the Line voltage peak. This approximation assumes the time constant $C_{IN} \times (R_{ZC1} + R_{ZC2})$ is long compared with a Line half-period. Under no-load conditions, the Burst OFF duty cycle is high therefore maximum power dissipation in the Drain sensing resistor divider chain, occurs at high Line and no-load, as described in Equation 60.

$$P_{ZCMax} = \frac{V_{InRMSMax}^{2} \times 2}{R_{ZC1} + R_{ZC2}} \tag{60}$$

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Equation 61 calculates the maximum value of R_{ZC1} c, allowing a budget of 1% error due to input bias current (I_{ZCBias}), on the lowest voltage threshold ($V_{ZCBoRise}$).

$$R_{ZC1} \le \frac{Err\% \times K_{ZC} \times V_{ZCBoRise}}{I_{ZCBias}} = \frac{1\% \times \sqrt{2} \times 85V}{100nA} = 12.0\,M\Omega \quad (61)$$

The upper resistor in the divider chain (R_{ZC1}) must withstand the peak output voltage under a surge test. For a rugged solution, the resistor(s) in this location must have a voltage rating above the avalanche rating of the Boost MOSFET. This design uses a series chain of three 1206, SMT, 3.24 MΩ resistors for this location, which yields DC voltage withstand capability above 600 V.

$$R_{ZC1} = 3 \times 3.24\,M\Omega = 9.72\,M\Omega \quad (62)$$

$$R_{ZC2} = \frac{R_{ZC1}}{K_{ZC} - 1} = 24.3\,k\Omega \quad (63)$$

Use Equation 60 to calculate the power dissipation in the ZCD/CS pin divider resistors.

$$P_{ZCMax} = \frac{V_{InRMSMax}^{\ 2} \times 2}{R_{ZC1} + R_{ZC2}} = 14\,mW \quad (64)$$

Once arranged on the PCB, the resistor divider circuit has some parasitic capacitance across both the upper (R_{ZC1}) and lower (R_{ZC2}) resistors. Experience suggests a parasitic capacitance (C_{ZC1}) of approximately 0.1 pF across resistor R_{ZC1}, when it is made up of three 1206 SMT components, assuming a *compact* PCB layout. In theory this parasitic capacitance could be used to form the entire value of C_{ZC1} and an appropriate value of C_{ZC2} added to achieve the ratio required by Equation 56. In practice most designers choose to add an explicit capacitor in this location to improve tolerance to small changes in layout, such as may occur when connecting oscilloscope probes. Ensure the time constant for the divider does not extend over many switching cycles. This limitation ensures that Line surge or system ESD transient events may disturb the ZCD/CS pin DC level but does not persist over an excessive number of switching cycles.

Select a single 10-pF, 1000-V, 0805 SMT capacitor with 5% tolerance.

$$C_{ZC1} = 10\,pF \quad (65)$$

Use Equation 66 calculate the lower divider capacitor value.

$$C_{ZC2} = K_{ZC} \times C_{ZC1} = 4.01\,nF \quad (66)$$

In practice, once the final PCB layout is complete, adjust the lower capacitor value to account for parasitic capacitances present on the PCB. Consider both the Drain and ZCD/CS pin waveforms and adjust the lower capacitance value (C_{ZC2}) until the value allows the required ratio in signal amplitude. Use a low capacitance probe for the ZCD/CS pin connection. Figure 28, Figure 29 and Figure 30 present the type of waveforms that occur during this tuning process.

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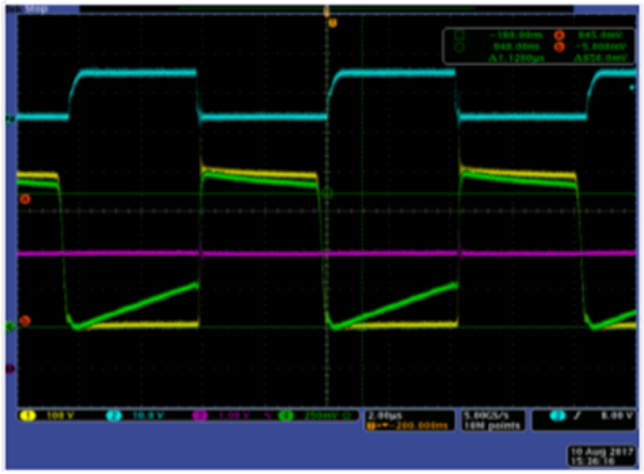
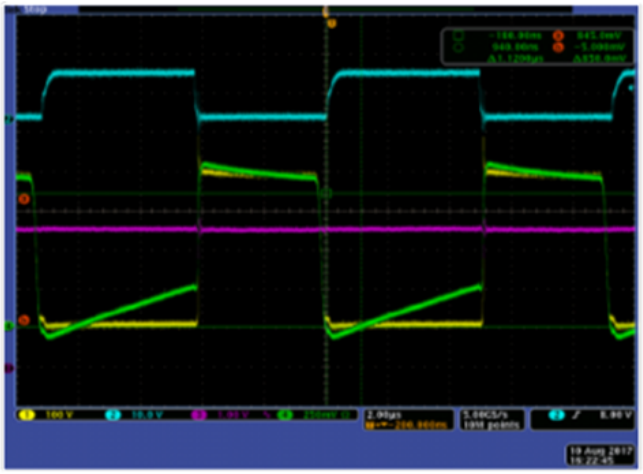


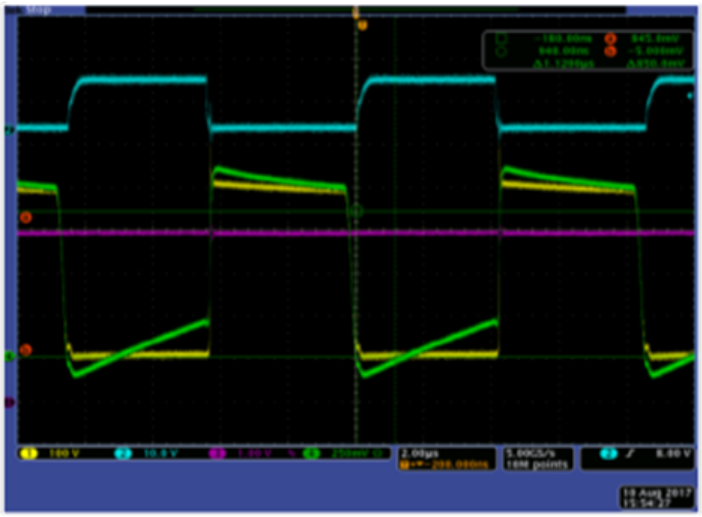
CH1 = V_{DS} CH2 = V_{DR}
CH3 = V_{CO} CH3 = V_{ZC}

Figure 28. Amplitude V_{ZC} < (V_{DS}/401). Reduce C_{ZC2} Capacitance



CH1 = V_{DS} CH2 = V_{DR}
CH3 = V_{CO} CH3 = V_{ZC}

Figure 29. Amplitude V_{ZC} = (V_{DS}/401). Correct C_{ZC2} Capacitance



CH1 = V_{DS} CH2 = V_{DR}
CH3 = V_{CO} CH3 = V_{ZC}

Figure 30. Amplitude V_{ZC} > (V_{DS}/401). Increase C_{ZC2} Capacitance

9.2.2.3.1 Voltage Spikes on the ZCD/CS pin Waveform

Voltage offset on the ZCD/CS pin is likely to result from high-amplitude switching edge spikes on the waveform applied to this pin. These switching edge spikes are clamped by any non-linear controller, such as the internal ESD structures, and upset the DC operating point of the divider. This can be observed as a voltage offset on the ZCD/CS pin signal, particularly at times when rate of change of current is highest (high load around the Line voltage peaks). When designing the ZCD/CS pin divider, prevent it from picking up switching edge spikes. Use of a low inductance type current sense resistor is also important for the same reason. If necessary an RC filter, with a time constant of approximately 30 ns, may be added between the voltage divider and the ZCD/CS pin to attenuate switching edge spikes. Ensure the capacitance (C_{ZC3}) of this filter is small relative to the value of C_{ZC2}. Limit the error introduced by the R-C filter to less than 1%, by ensuring that the series resistance is below the value calculated in Equation 67.

$$R_{ZC3} < \frac{V_{ZCBoRise}}{I_{ZCBias}} \times 1\% = 30\ k\Omega \quad (67)$$

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For this example design, the following values were selected for the RC filter to attenuate switching edge spikes.

$$R_{ZC3} = 3\,k\Omega \tag{68}$$

$$C_{ZC3} = 10pF \tag{69}$$

9.2.2.4 VOSNS Pin

The VOSNS pin voltage is applied to the inverting input of an internal trasnconductance error amplifier. A fixed reference voltage (V_{OSReg}) being applied to the non-inverting input. The error amplifier has high gain hence in steady-state, assuming VCOMP < 5-V, average voltage on the VOSNS pin must be approximately equal to the reference voltage (V_{OSReg}). Output voltage regulation set point (V_{OutReg}) is therefore determined by the external resistor divider network connecting the output voltage to the VOSNS pin according to the following expression.

$$V_{OutReg} = V_{OSReg} \times \left(\frac{R_{OS1}}{R_{OS2}} + 1 \right) \tag{70}$$

The resistive divider that feeds the VOSNS pin makes a significant contribution to the unloaded input power. Higher resistor values reduce power consumption of the divider.

$$P_{OSDiv} = \frac{V_{OutReg}^{2}}{R_{OS1} + R_{OS2}} \tag{71}$$

Regulation accuracy degrades with increased resistor values due to the effect of VOSNS pin bias current (I_{OSBias}).

$$\frac{\Delta V_{OSReg}}{V_{OSReg}} = \frac{I_{OSBias} \times R_{OS1}}{V_{OutReg}} \tag{72}$$

To ensure that VOSNS pin bias current degrades output voltage regulation by less than 1%, the upper voltage divider resistor value must be constrained as show in Equation 73.

$$R_{OS1} < \frac{\Delta V_{OSReg}}{V_{OSReg}} \times \frac{V_{OutReg}}{I_{OSBias}} = 1\% \times \frac{390\ V}{100\ nA} = 39\,M\Omega \tag{73}$$

Equation 73 confirms that reduction of the VOSNS divider dissipation to below 4 mW does not negatively affecting the regulation accuracy.

The PFC stage, of this design example, is to be followed by an LLC stage, that is controlled by UCC256301 device. The UCC28056 controller and the UCC256301 device operate together to form a complete off-Line power supply system with excellent light-load efficiency and standby power. To limit no-load input power a single resistor divider feeds both the VOSNS pin (UCC28056) and the BLK pin (UCC256301). A resistor divider with two taps is required because the UCC28056 requires a different divide ratio (K_{OS}) to that required for the UCC256301 device (K_{BLK}). The upper divider resistor (R_{OS1}) is divided into two parts (R_{OS11}, R_{OS12}) to achieve the additional tap.

$$K_{OS} = \frac{V_{OutReg}}{V_{OSReg}} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS2}} = 156 \tag{74}$$

$$K_{BLK} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS12} + R_{OS2}} = 108 \tag{75}$$

For this design example select an upper divider resistor made up of three series-connected, 3.24-MΩ, 1206 SMT resistors. This compact and cost-effective design produces a suitable high-voltage resistor. If a single resistor is preferred, use a high voltage type, rated for the maximum voltage that can appear across the output capacitor during a Line surge test.

$$R_{OS11} = 3 \times 3.24\,M\Omega = 9.72\,M\Omega \tag{76}$$

Solving Equation 74 and Equation 75 simultaneously results in:

$$R_{OS12} = \frac{R_{OS11}}{K_{OS}} \times \left(\frac{K_{OS} - 1}{K_{BLK} - 1} - 1 \right) = 27.95\,k\Omega \tag{77}$$

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$$R_{OS2} = \frac{R_{OS11} + R_{OS12}}{K_{OS} - 1} = 62.89\ k\Omega \tag{78}$$

These two divider resistor values can be implemented using easily obtainable values as follows:

$$R_{OS2} = 75\ k\Omega\ //\ 390\ k\Omega = 62.9\ k\Omega \tag{79}$$

$$R_{OS12} = 36.5\ k\Omega\ //\ 120\ k\Omega = 28.0\ k\Omega \tag{80}$$

Actual regulation set point is therefore:

$$V_{OutReg} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS2}} \times V_{OSReg} = 390\ V \tag{81}$$

Power dissipated in the VOSNS resistor divider is:

$$P_{OSDiv} = \frac{V_{OutReg}^{2}}{R_{OS11} + R_{OS12} + R_{OS2}} = 15.5\ mW \tag{82}$$

9.2.2.5 Voltage Loop Compensation

The design of the voltage control loop of a PFC stage is requires compromise. The voltage control loop must be fast to achieve a good transient response to steps in load current, but tTo minimize distortion of the Line current it must be slow. This section describes the selection of compensation components that deliver a target Line current distortion and phase margin.

9.2.2.5.1 Plant Model

The first step is to produce a small signal model of the PFC Boost converter. A constant power load is assumed to be connected across the output capacitor. This provides the most accurate representation of a switched mode regulator delivering constant output voltage. The plant gain is assumed to be independent of Line voltage due to the action of the internal Line voltage feed-forward circuit. Across the Universal Line voltage range (90 V_{RMS}-264 V_{RMS}), plant gain actually varies by ±-20% due to the quantized nature of the Line voltage feed-forward circuit.

$$\frac{v_{Out}(j\omega)}{v_{CO}(j\omega)} = G_{Plant}(j\omega) = \frac{1}{j\omega} \times G_{Plant0} = \frac{1}{j\omega} \times \frac{P_{OutMax}}{V_{COMax} \times V_{OutReg} \times C_{Out}} \tag{83}$$

9.2.2.5.2 Compensator Design

The integrator response of the plant provides a gain roll off of –20dB/decade and introduces a phase lag of 90°. A simple integrating compensation network provides unacceptable phase margin because it introduces a second 90° of phase lag into the voltage loop. To ensure adequate phase margin, use a type 2 compensation network to provide the desired phase boost a the gain cross-over frequency. Equation 84 describes the mall-signal gain of the error amplifier and type 2 compensation network.

$$\frac{v_{CO}(j\omega)}{v_{Out}(j\omega)} = G_{Ctrl}(j\omega) = \frac{V_{OSReg}}{V_{OutReg}} \times g_M \times \frac{\left(R_{CO} + \frac{1}{j\omega \times C_{CO}}\right) \times \frac{1}{j\omega \times C_{CO1}}}{R_{CO} + \frac{1}{j\omega \times C_{CO}} + \frac{1}{j\omega \times C_{CO1}}} \tag{84}$$

Equation (84) may also be expressed as follows:

$$G_{Ctrl}(j\omega) = \frac{G_{Ctrl0}}{j\omega} \times \frac{1 + \frac{j\omega}{2 \times \pi \times f_Z}}{1 + \frac{j\omega}{2 \times \pi \times f_P}}$$

where

$$f_Z = \frac{1}{2 \times \pi \times (C_{CO} \times R_{CO})} \tag{86}$$

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$$f_P = \frac{C_{CO} + C_{CO1}}{2 \times \pi \times (C_{CO} \times C_{CO1} \times R_{CO})} \quad (87)$$

$$G_{Ctrl0} = \frac{V_{OSReg}}{V_{OutReg}} \times g_M \times \frac{1}{(C_{CO} + C_{CO1})} \quad (88)$$

(88)

Rearranging Equation 86, Equation 87 and Equation 88 yields:

$$C_{CO1} = \frac{f_Z}{f_P} \times \frac{1}{G_{Ctrl0}} \times \left(\frac{V_{OutReg}}{V_{OSReg}} \times g_M \right) \quad (89)$$

$$C_{CO} = \frac{f_P - f_Z}{f_Z} \times C_{CO1} \quad (90)$$

$$R_{CO} = \frac{1}{2 \times \pi \times f_Z} \times \frac{1}{C_{CO}} \quad (91)$$

For maximum phase Boost at the gain cross-over frequency, compensator design proceeds by placing the pole and zero an equal distance above and below the gain cross-over frequency (f_B) on the Bode plot. Because the frequency axis is logarithmic this yields the following pole (f_P) and zero (f_Z) frequencies:

$$f_Z = \frac{f_B}{K} \quad (92)$$

$$f_P = f_B \times K \quad (93)$$

Phase margin of the loop is equal to the phase boost provided by the type 2 compensator, because the underlying integrator characteristics of the plant and compensator combine to provide 180° of phase lag. To achieve the desired phase margin (Φ_{PM}) at f_B the separation between the pole and zero frequencies may be found by substituting Equation 92 and Equation 93 into Equation 85, and solving for K in terms of the phase boost angle.

$$K = \tan\left(\frac{\Phi_{PM}}{2} + \frac{\pi}{4} \right) \quad (94)$$

The next step is to select the desired phase margin. A typical phase margin range 45° to 75°. For this example design a target phase margin of 65° is selected.

$$\Phi_{PM} = 65° \times \frac{\pi}{180°} \quad (95)$$

$$K = \tan\left(\frac{\Phi_{PM}}{2} + \frac{\pi}{4} \right) = 4.51 \quad (96)$$

The next step is to determine the loop gain cross-over frequency (f_B). A faster loop, results in more twice Line frequency ripple on the COMP pin voltage, leading to increased Line current distortion.

Begin by setting a target of 1% third harmonic distortion due to twice Line frequency COMP voltage ripple. To achieve this target, the twice Line frequency COMP pin ripple must be less than 2% of the DC value during steady-state full power operation. The design proceeds by selecting the loop gain cross-over frequency (f_B) that ensures twice Line frequency COMP pin ripple amplitude does not exceed 2% of its DC level.

Use Equation 97 to calculate twice Line frequency voltage ripple amplitude across the output capacitor.

$$\Delta V_{Out} = \frac{P_{OutMax}}{V_{OutReg}} \times \frac{1}{2 \times 2 \times \pi \times f_{Line} \times C_{Out}} = 4.95\ V \quad (97)$$

The output voltage ripple amplitude must be attenuated by the feedback network to meet our target of 2% ripple amplitude on the COMP pin voltage.

$$\left| G_{Ctrl}\left(j2 \times \pi \times 2 \times f_{Line} \right) \right| = \frac{V_{COMax} \times 2\%}{\Delta V_{Out}} \quad (98)$$

Equation 99 simplifies Equation 98.

$$G_{Ctrl0} = \frac{0.0202}{K^2} \times 4 \times \pi \times f_{Line} = 0.624\ Hz$$

where

- $2 \times f_{Line} >> f_P$
- $2 \times f_{Line} >> f_Z$ (99)

Equation 100 describes unity at the gain cross-over frequency.

$$\left|G_{Plant}\left(j2 \times \pi \times f_B\right)\right| \times \left|G_{Ctrl}\left(j2 \times \pi \times f_B\right)\right| = 1 \quad (100)$$

Equation 100 can also be expressed as shown in Equation 101.

$$f_B = \frac{1}{2 \times \pi} \times \sqrt{G_{Plant0} \times G_{Ctrl0} \times K} = 6.66\ Hz \quad (101)$$

Calculate the pole and zero frequencies using Equation 92 and Equation 93. Then determine the compensation component values using Equation 89, Equation 90 and Equation 91.

$$f_Z = \frac{f_B}{K} = 1.48\ Hz \quad (102)$$

$$f_P = f_B \times K = 30.0\ Hz \quad (103)$$

$$C_{CO1} = \frac{f_Z}{f_P} \times \frac{1}{G_{Ctrl0}} \times \frac{V_{OSReg}}{V_{OutReg}} \times g_M = 25\ nF \quad (104)$$

$$C_{CO} = \frac{f_P - f_Z}{f_P} \times C_{CO1} = 0.49\ \mu F \quad (105)$$

$$R_{CO} = \frac{1}{2 \times \pi \times f_Z} \times \frac{1}{C_{CO}} = 220\ k\Omega \quad (106)$$

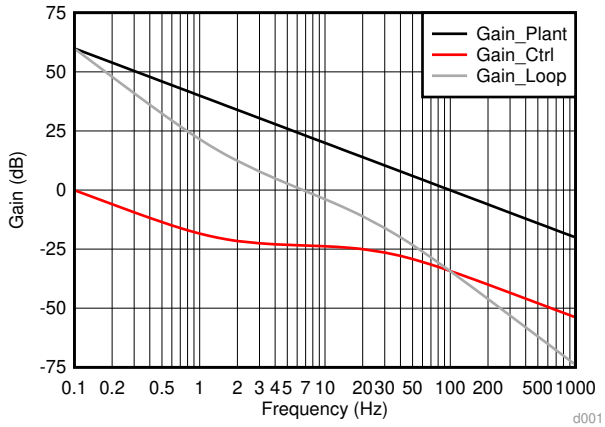

Figure 31. Gain vs Frequency

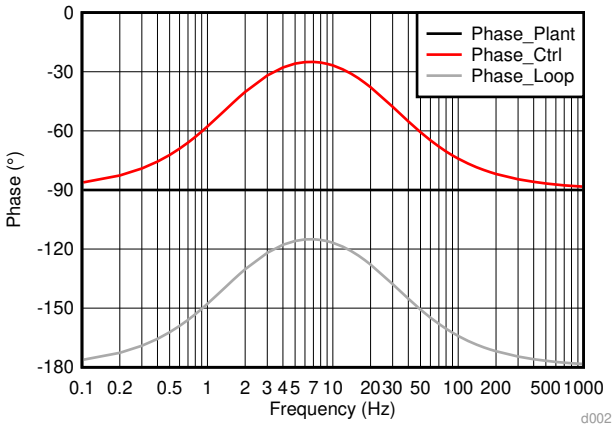

Figure 32. Phase vs Frequency

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9.2.3 Application Curves

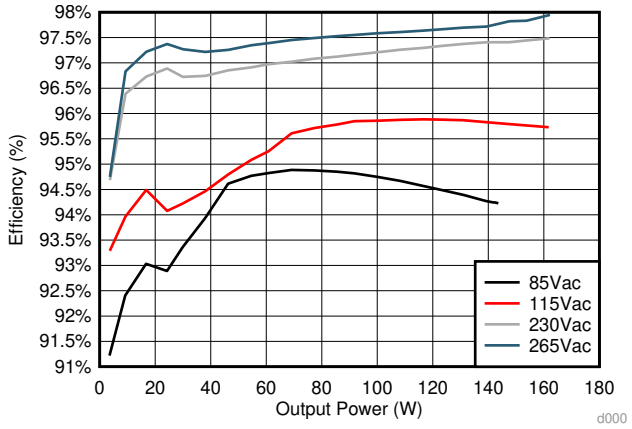

Figure 33. Efficiency vs Output Power

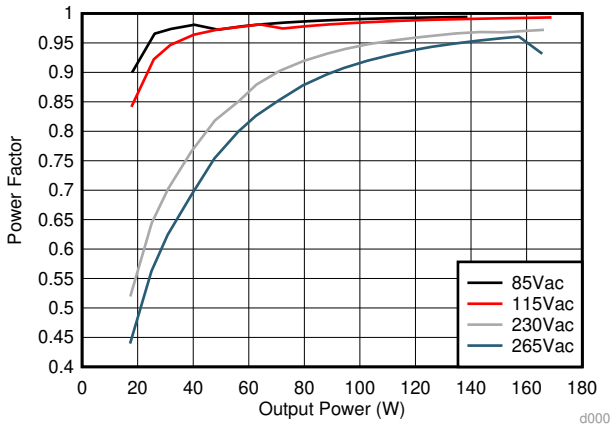

Figure 34. Power Factor vs Output Power

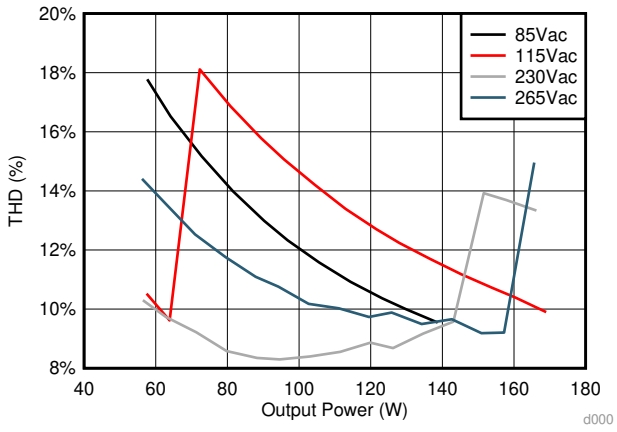

Figure 35. THD vs Output Power

10 Power Supply Recommendations

To operate UCC28056 must be powered from an external VCC supply voltage of 11 V to 34 V. To limit package dissipation ensure that the supply voltage is not higher than 12 V. Locally decouple the VCC supply with a capacitor of at least 1 µF connected between the VCC and GND pins using short PCB traces. The controller may consume current from the VCC rail for a significant period of time; the exact duration depends upon Line and load, before the output voltage (V_{Out}) reaches regulation. The supply used to power the UCC28056 must be able to source this energy during the period that output voltage attains regulation.

11 Layout

11.1 Layout Guidelines

11.1.1 VOSNS Pin

Locate the R_{OS2} and C_{OS2} components adjacent to the VOSNS pin along with the lowest resistor(s) that comprise R_{OS1}. High voltage drops across the resistor(s) that comprise R_{OS1}. Allow adequate spacing around the high-voltage nodes that connect to and within R_{OS1} to avoid air discharge across the PCB surface.

11.1.2 ZCD/CS Pin

Switching edge spikes imposed on the signal feeding this pin may cause the internal ESD structures to conduct, causing a voltage offset to appear on the capacitive divider feeding this pin. To limit this risk, place the voltage divider close to the ZCD/CS pin and far from the region of fast changing magnetic field. See the shaded area show in Figure 37. Maintain a small number of nets between the resistors and capacitors in the divider to limit capacitive pickup within the divider chain. Maintain the loop identified in Figure 36 small and contain the minimum area to limit magnetic pickup. Run the connections between the current sense resistor and UCC28056 directly to the terminals of resistor and not be shared with power circuit traces.

When laying out the PCB start with the ZCD/CS pin divider placement and routing to ensure that the needs of this pin come first.

11.1.3 VCC Pin

A local decoupling capacitor should be connected directly between the VCC and GND pins via short, dedicated, PCB traces. This capacitor supplies the high current pulses needed to charge the gate capacitance of the power MOSFET.

11.1.4 GND Pin

Be sure to separate the PCB traces for the GND net of the UCC28056 far from the power circuit GND net. Connect the GND pin of the UCC28056 device to the power circuit GND at only one terminal of the current sense resistor. This connection method ensures that the voltage between the UCC28056 device GND pin and the ZCD/CS pins remains equal to the voltage across the current sense resistor during the MOSFET conduction period.

11.1.5 DRV Pin

Avoid placing the DRV pin traces close to other high-impedance nets such as ZCD/CS or VOSNS. The fast rising and falling edges associated with the waveform on this pin may capacitively couple onto these high impedance nets causing disturbance near the switching edges.

11.1.6 COMP Pin

Locate the RC network attached to this pin close to the pin. Return to the GND pin should be via a short PCB trace.

11.2 Layout Example

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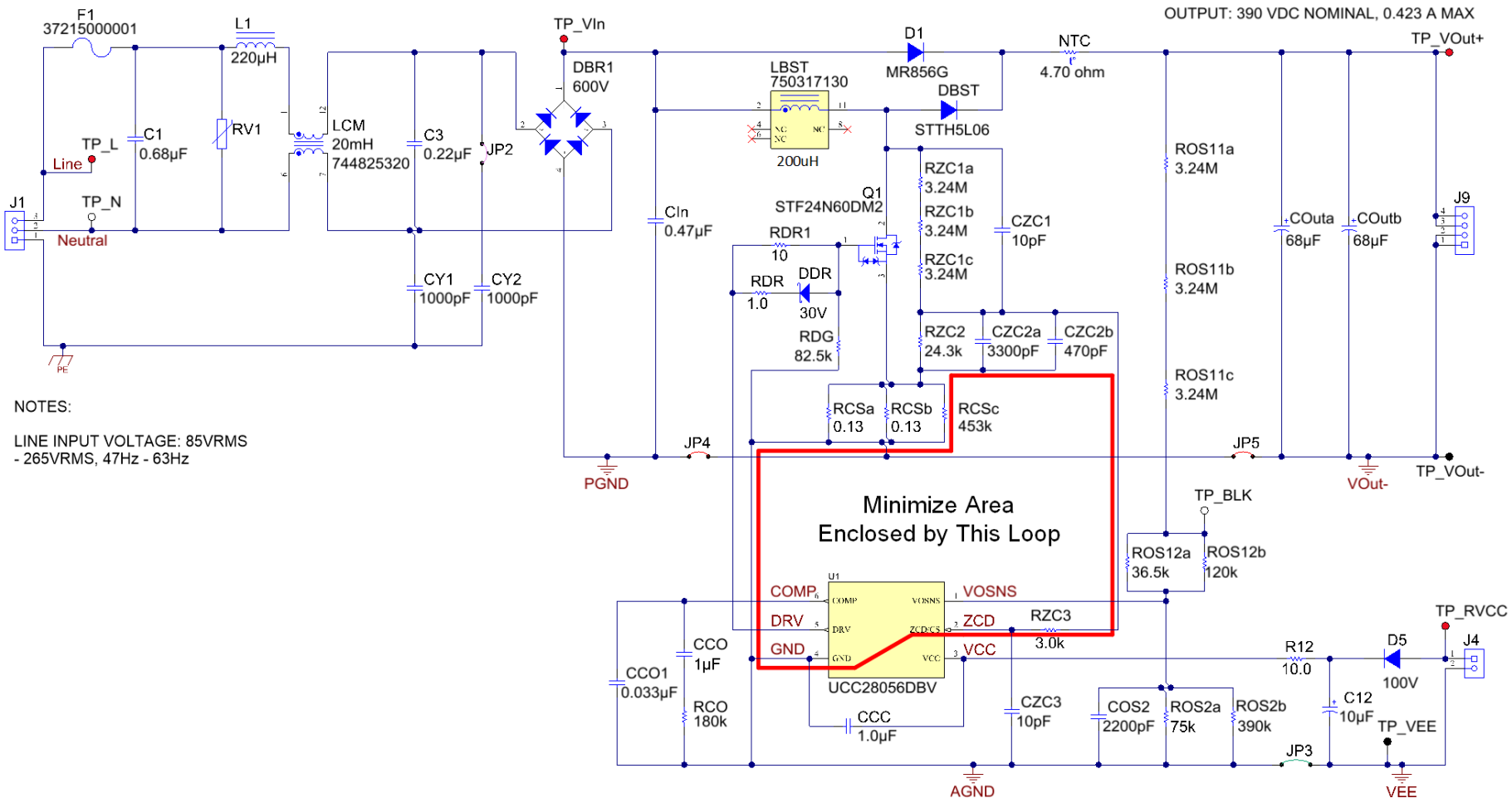

Figure 36. Schematic with Layout Guidelines

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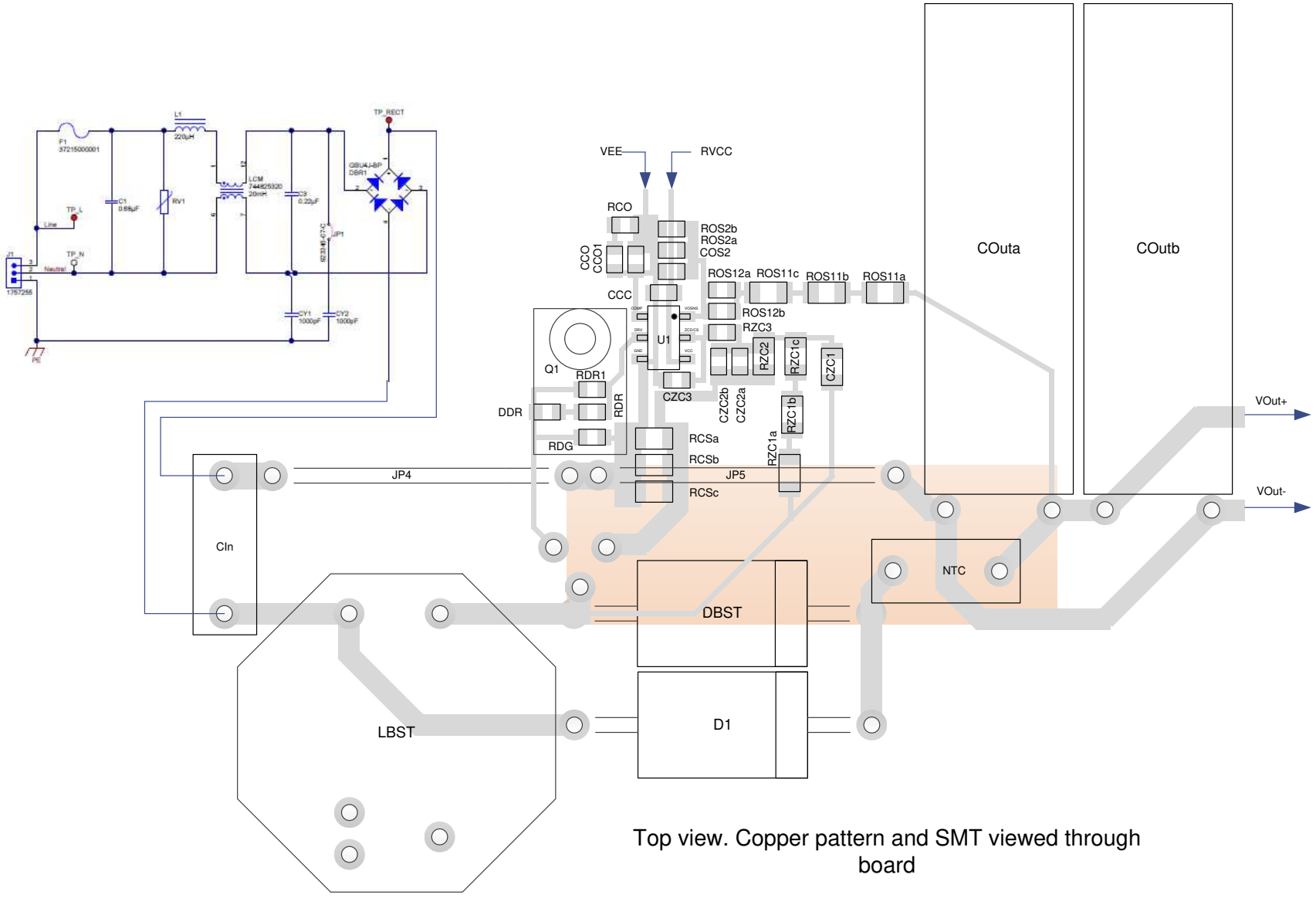

Top view. Copper pattern and SMT viewed through board

Figure 37. Recommended PCB Layout (Single-Sided Assembly)

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12 Device and Documentation Support

12.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28056 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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In most cases, these actions are available:

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28056ADBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVTG4.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056ADBVTG4.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	805A
UCC28056BDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	805B
UCC28056BDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805B
UCC28056BDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805B
UCC28056BDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	805B
UCC28056BDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805B
UCC28056BDBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805B
UCC28056CDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	805C
UCC28056CDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805C
UCC28056CDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805C
UCC28056CDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	805C
UCC28056CDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805C
UCC28056CDBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	805C
UCC28056DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056
UCC28056DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056
UCC28056DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056
UCC28056DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056
UCC28056DBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056
UCC28056DBVTG4.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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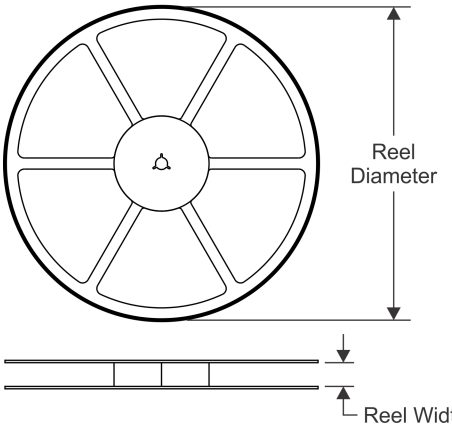
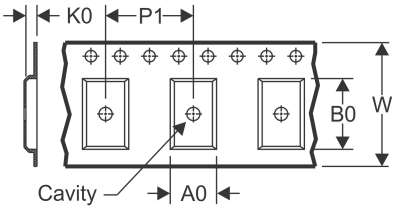
TAPE AND REEL INFORMATION

REEL DIMENSIONS

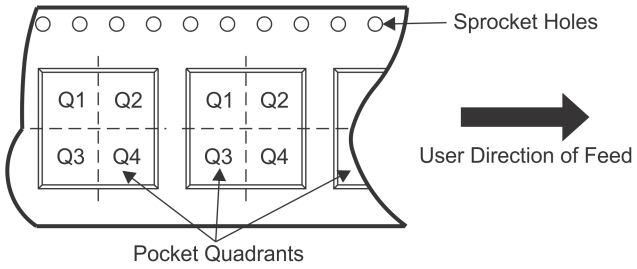


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

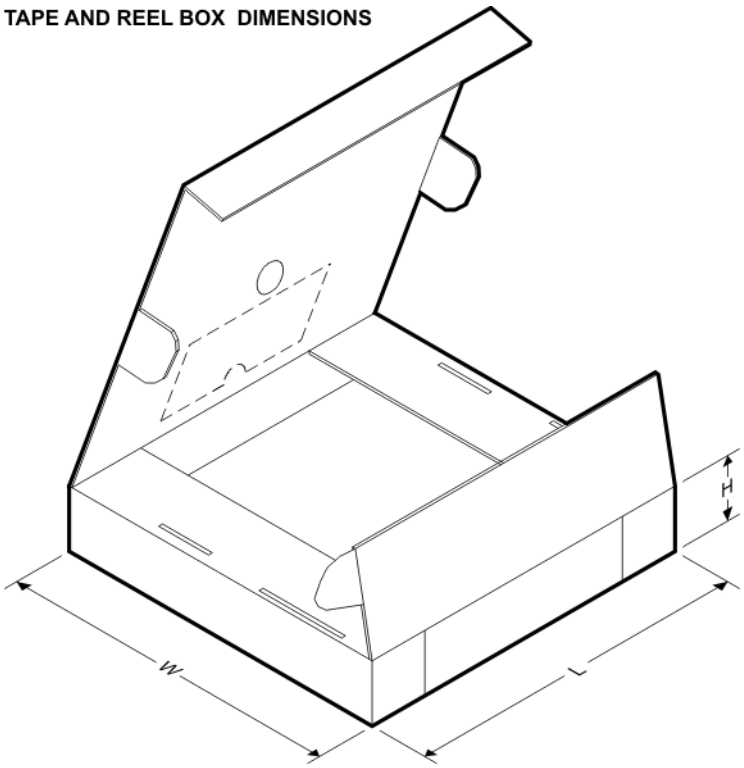
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28056ADBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056ADBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056BDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056BDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056CDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056CDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28056DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

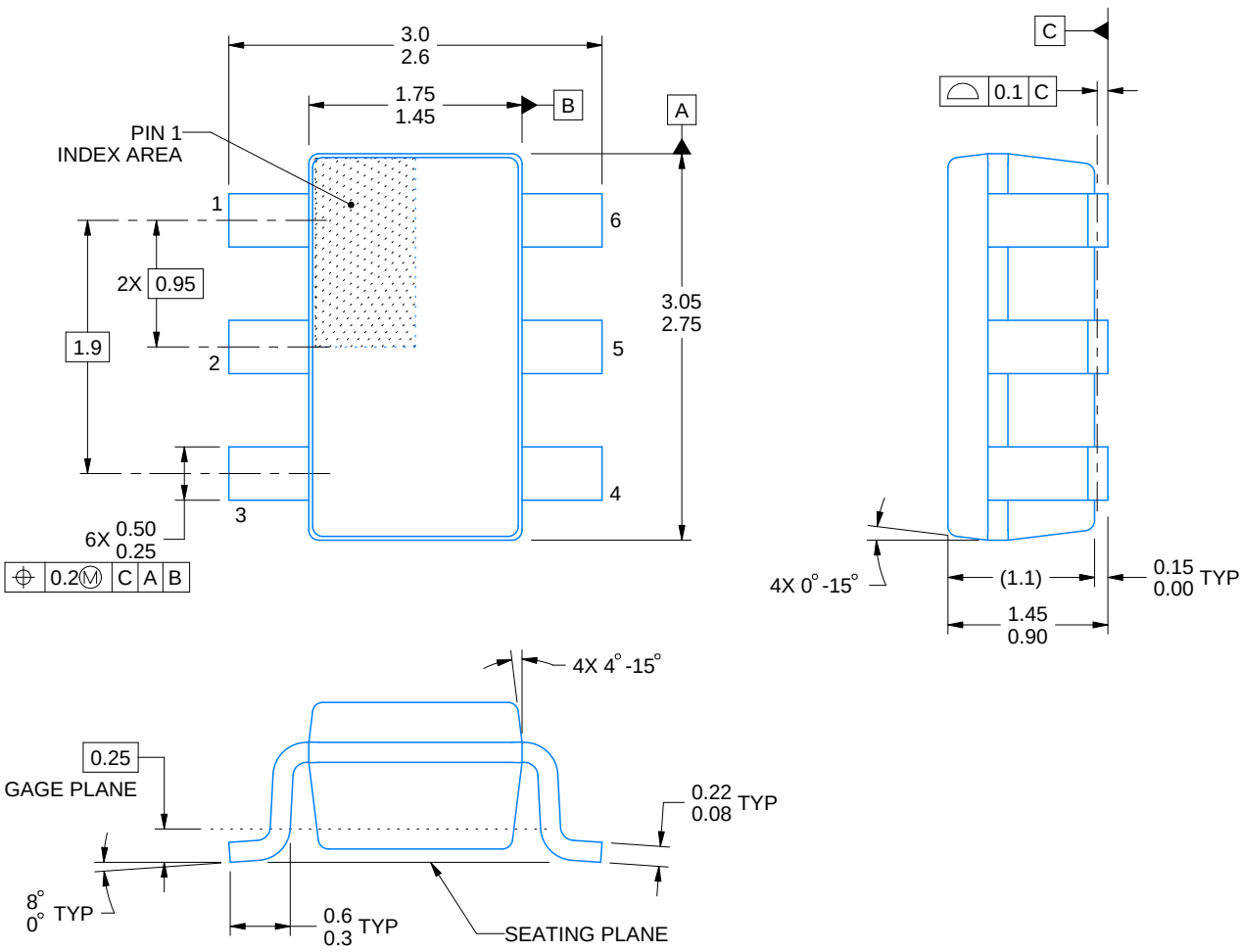
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28056ADBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28056ADBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC28056BDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28056BDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC28056CDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28056CDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC28056DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28056DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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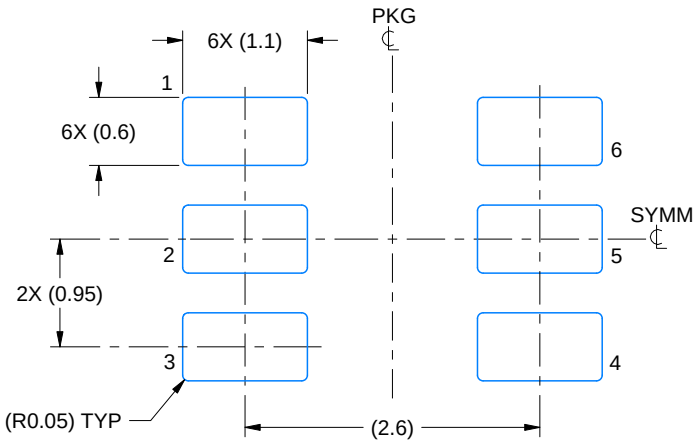
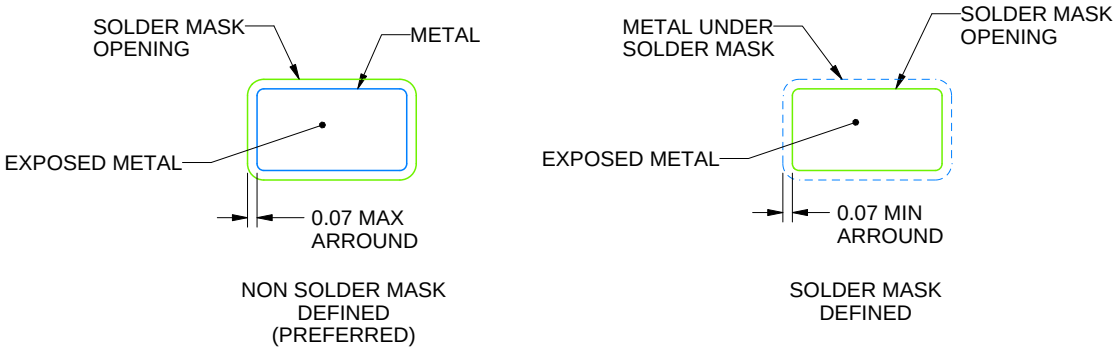
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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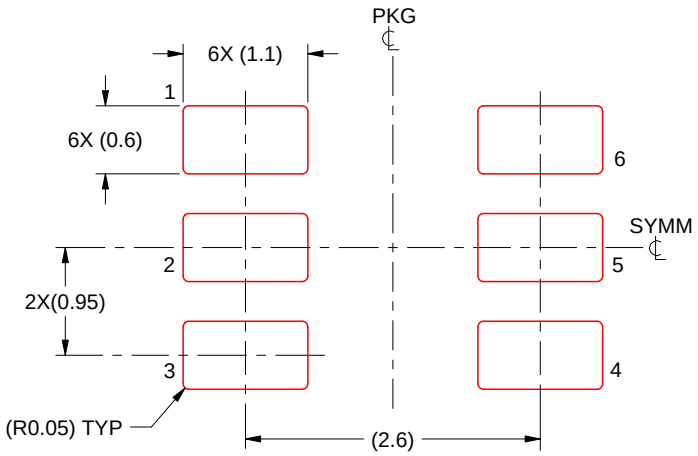
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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