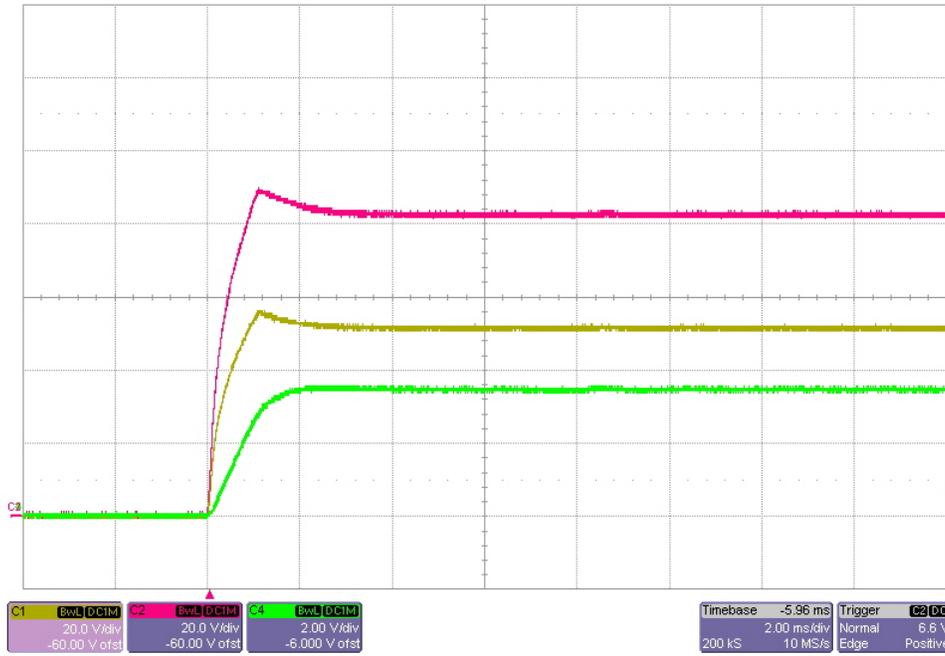
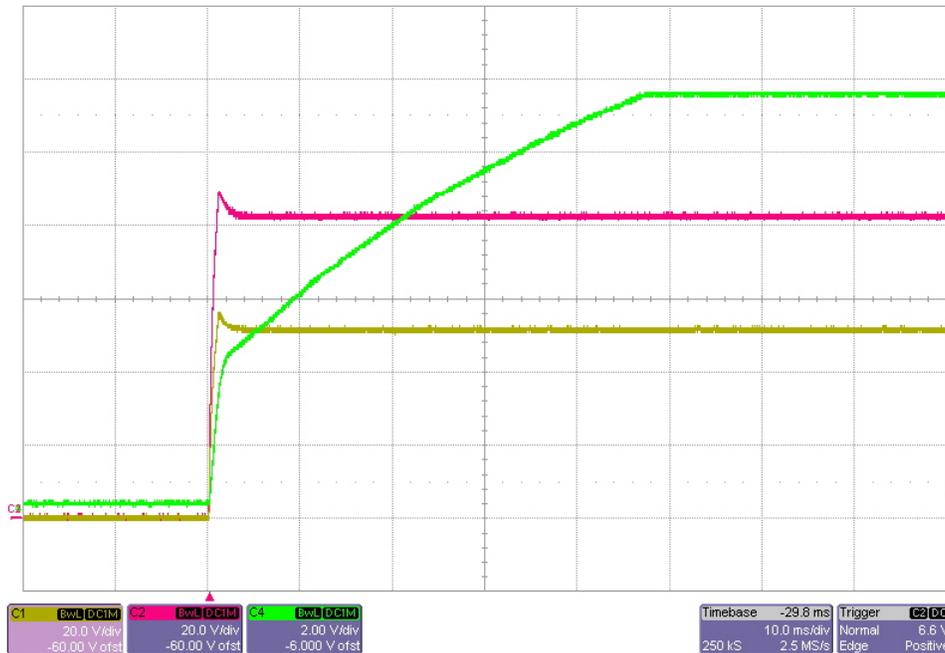


1 Startup

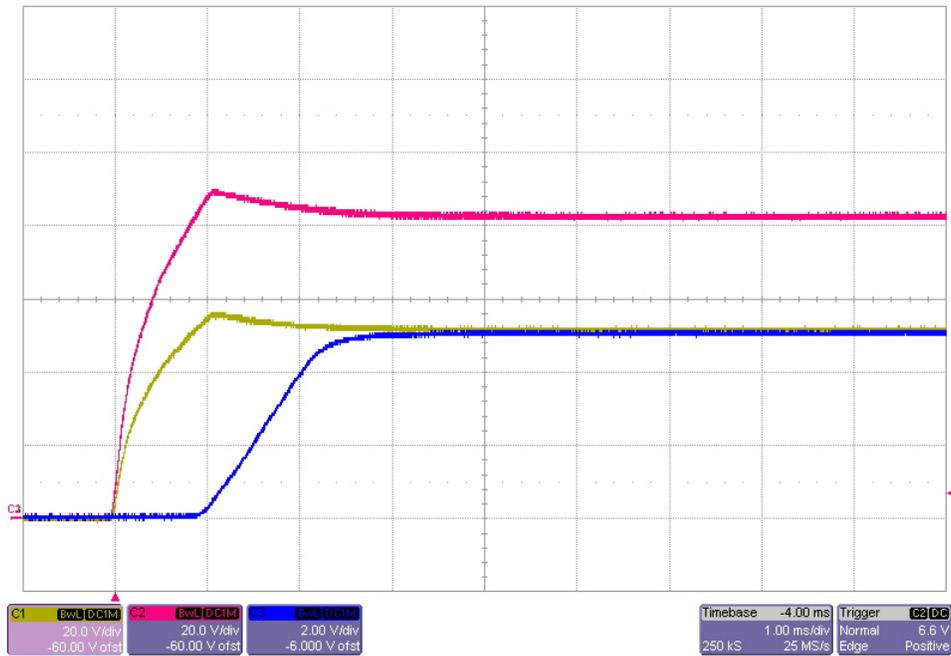
The 82V, 52V and 3.7V output voltage startup waveforms are shown in the figure below after the application of 14Vin. The outputs voltages were loaded to max. The 3.7V output was measured with respect to the 3.7V RTN. (82V/52V = 20V/DIV, 3.7V = 2V/DIV, 2mS/DIV)



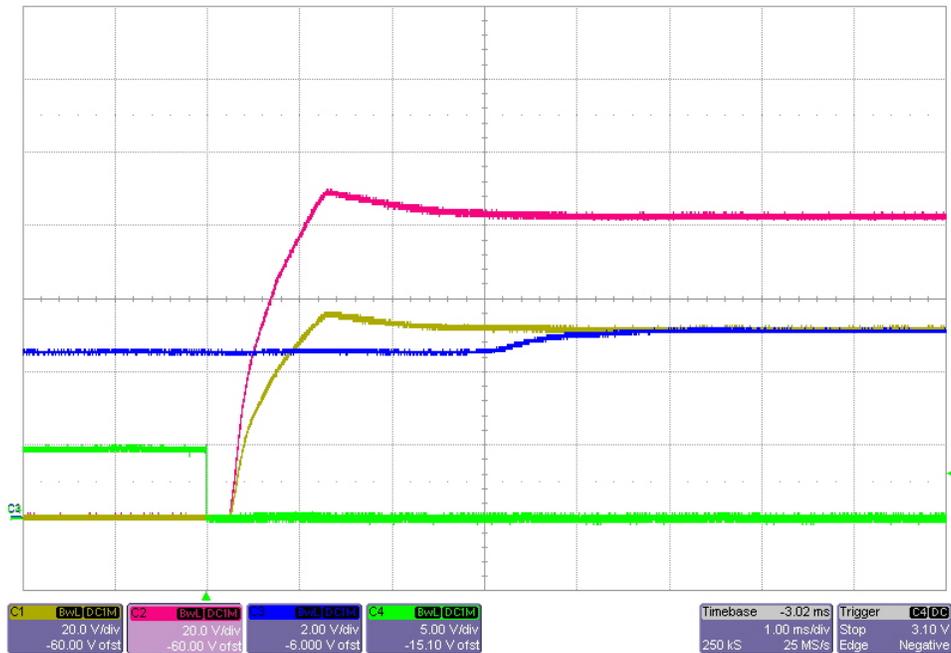
The 82V, 52V and 3.7V output voltage startup waveforms are shown in the figure below after the application of 14Vin. The outputs voltages were loaded to max. The 3.7V output was measured with respect to the GND (3.7V output voltage is offset by 8.2V zener diode D6). (82V/52V = 20V/DIV, 3.7V = 2V/DIV, 10mS/DIV)



The 82V, 52V and 5V output voltage startup waveforms are shown in the figure below after the application of 14Vin. The outputs voltages were loaded to max. (82V/52V = 20V/DIV, 5V = 2V/DIV, 1mS/DIV)

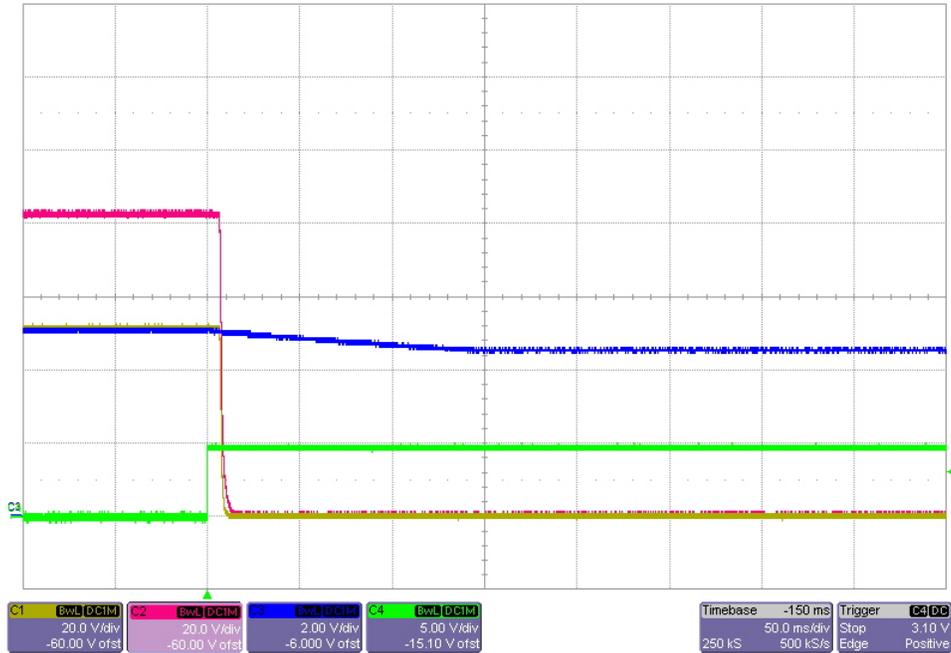


The 82V, 52V and 5V output voltage startup waveforms are shown in the figure below after the removal of the Shutdown signal. Vin = 14Vin. The 82V and 52V outputs voltages were loaded to max and the 5V was loaded to 1mA. The linear regulator is holding up the output voltage at 4.5V before the 5V output turns on. (Shutdown = 5V/DIV, 82V/52V = 20V/DIV, 5V = 2V/DIV, 1mS/DIV)



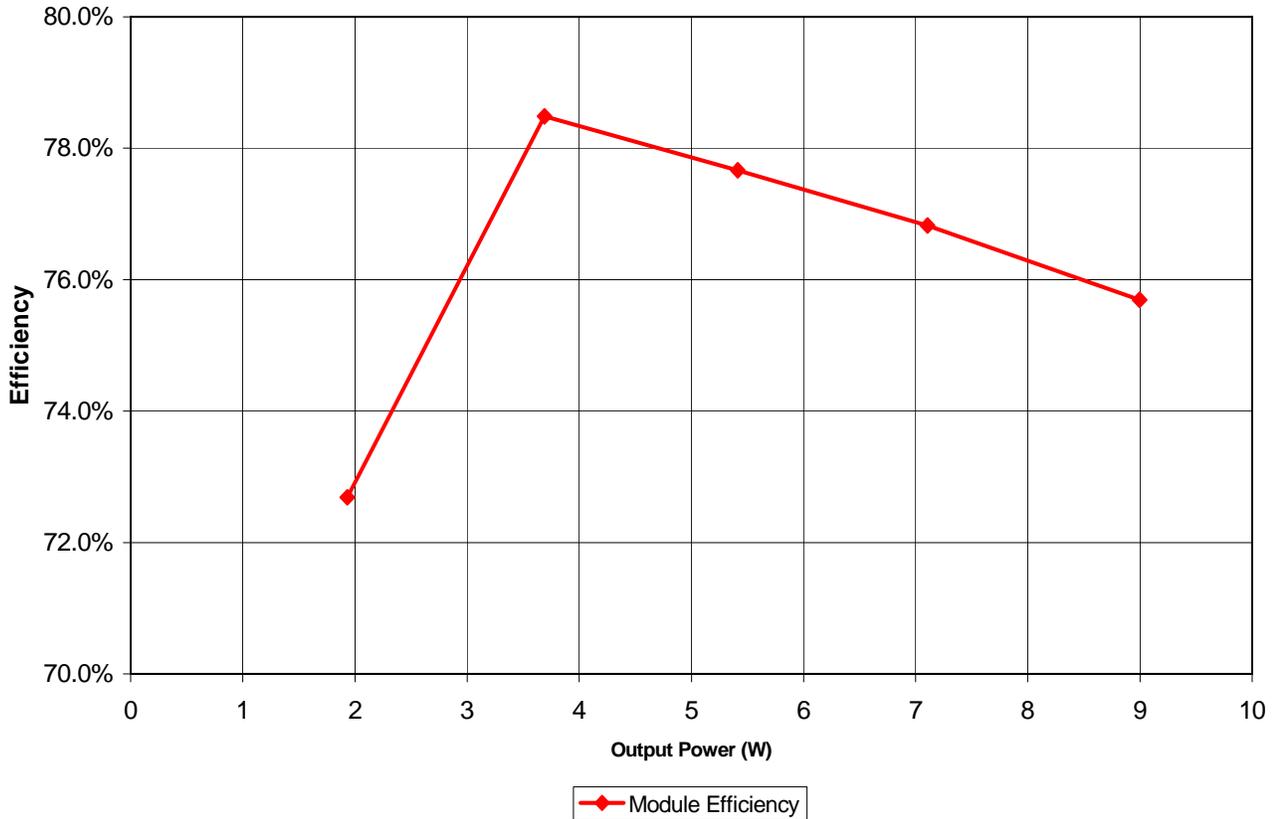
The 82V, 52V and 5V output voltage turnoff waveforms are shown in the figure below after the application of the Shutdown signal. $V_{in} = 14V_{in}$. The 82V and 52V outputs voltages were loaded to max and the 5V was loaded to 1mA. The linear regulator holds the 5V output voltage at 4.5V.

(Shutdown = 5V/DIV, 82V/52V = 20V/DIV, 5V = 2V/DIV, 50mS/DIV)



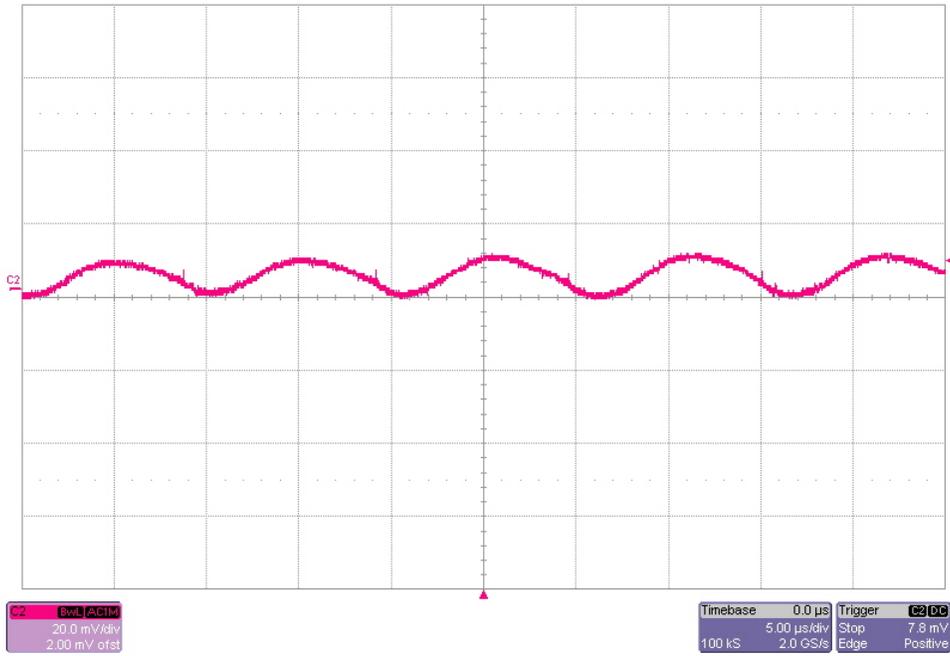
2 Efficiency

The total module efficiency is shown in the figure below. Each output voltage was loaded proportionally with data points at 20% load steps. Output voltages were measured at the converter output capacitors. $V_{in} = 14V$.

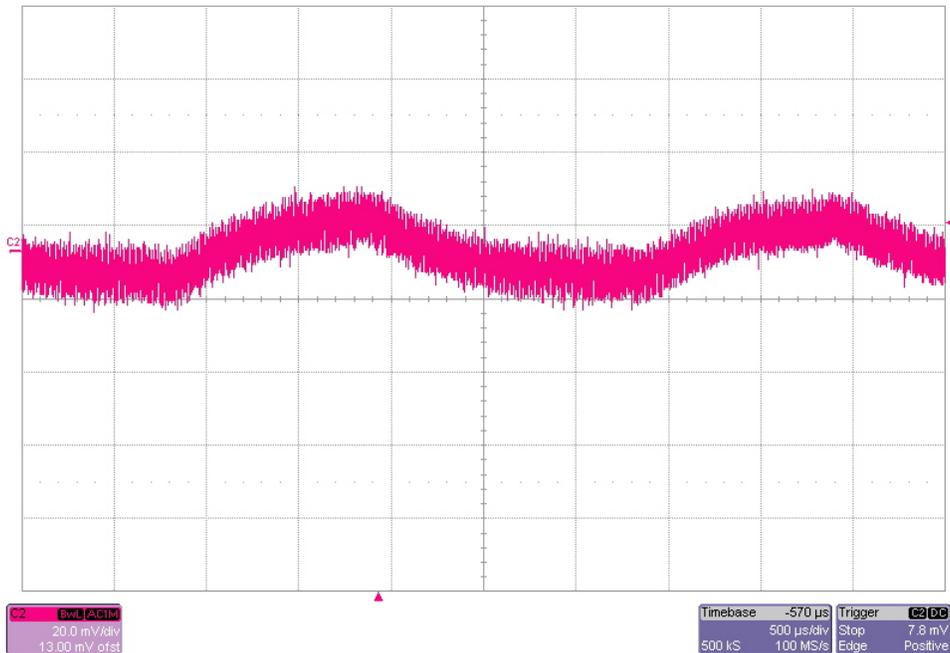


3 Output Ripple Voltage

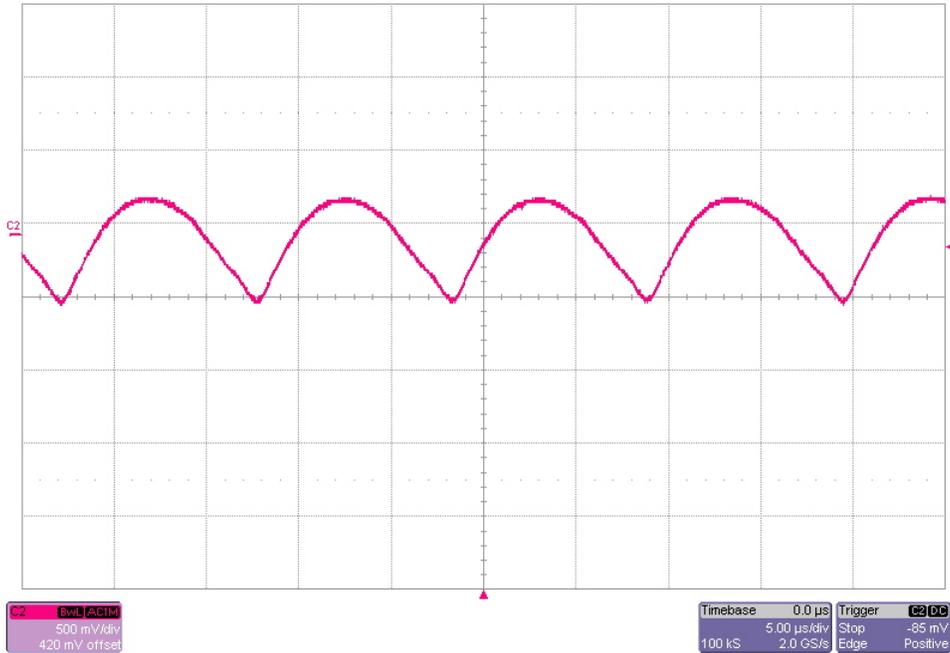
The 5V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max load (5V @ 0.5A, 82V @ 30mA, 52V @ 40mA, 3.7V @ 0.5A). $V_{in} = 14V$ (20mV/DIV, 5uS/DIV)



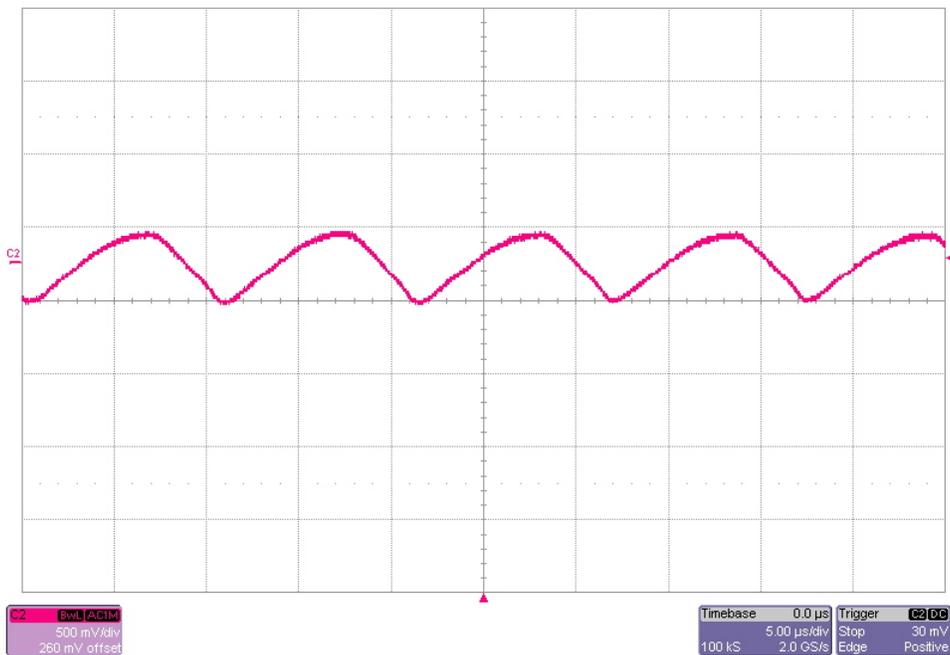
The 5V output dither frequency ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max load (5V @ 0.5A, 82V @ 30mA, 52V @ 40mA, 3.7V @ 0.5A). $V_{in} = 14V$ (20mV/DIV, 500uS/DIV)



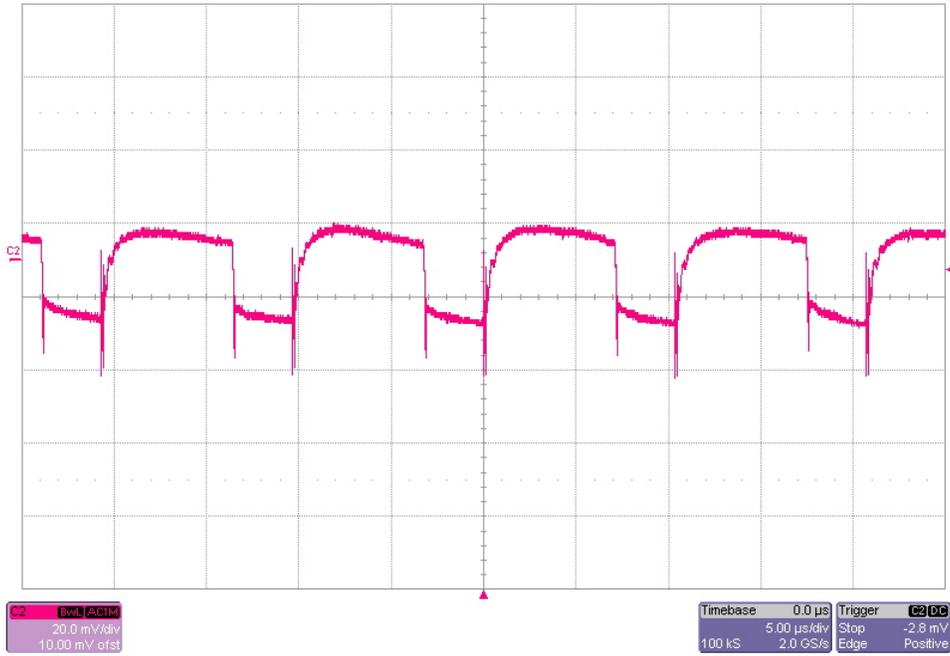
The 82V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max load (5V @ 0.5A, 82V @ 30mA, 52V @ 40mA, 3.7V @ 0.5A). $V_{in} = 14V$ (500mV/DIV, 5uS/DIV)



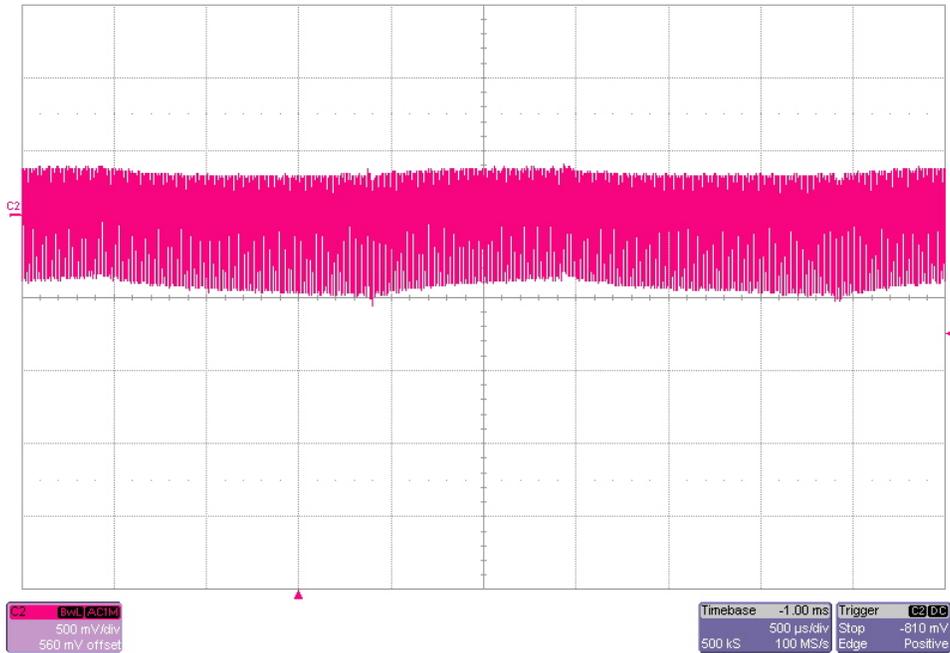
The 52V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max load (5V @ 0.5A, 82V @ 30mA, 52V @ 40mA, 3.7V @ 0.5A). $V_{in} = 14V$ (500mV/DIV, 5uS/DIV)



The 3.7V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max load (5V @ 0.5A, 82V @ 30mA, 52V @ 40mA, 3.7V @ 0.5A). Vin = 14V (20mV/DIV, 5uS/DIV)

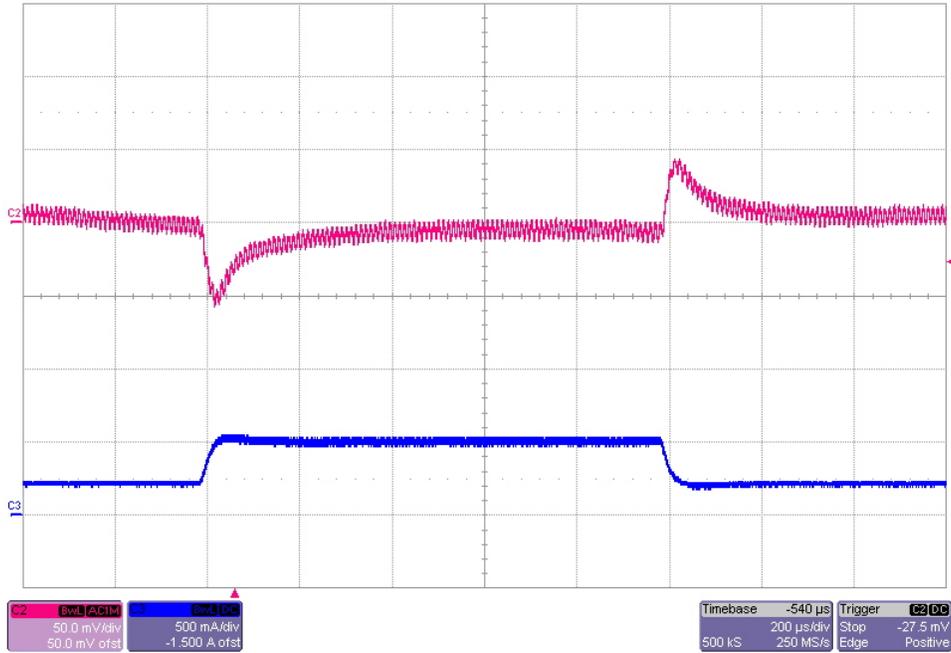


The 82V output dither frequency ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max load (5V @ 0.5A, 82V @ 30mA, 52V @ 40mA, 3.7V @ 0.5A). Vin = 14V (500mV/DIV, 500uS/DIV)

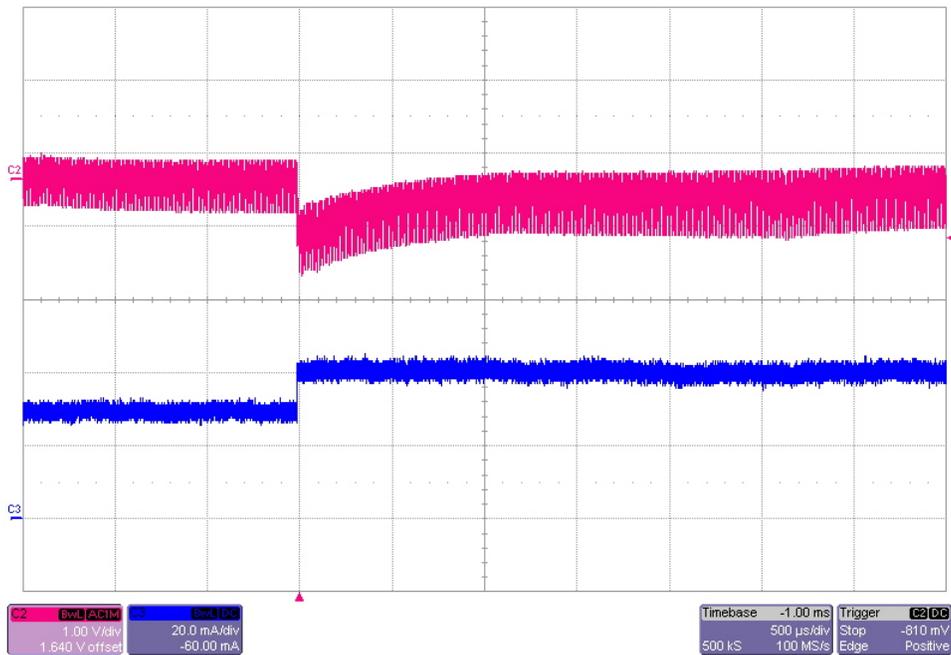


4 Load Transient Response

The photo below shows the 5V output response and recovery to a 0.25A to 0.5A step load. $V_{in} = 14V$. (50mV/DIV, 0.5A/DIV, 200uS/DIV)

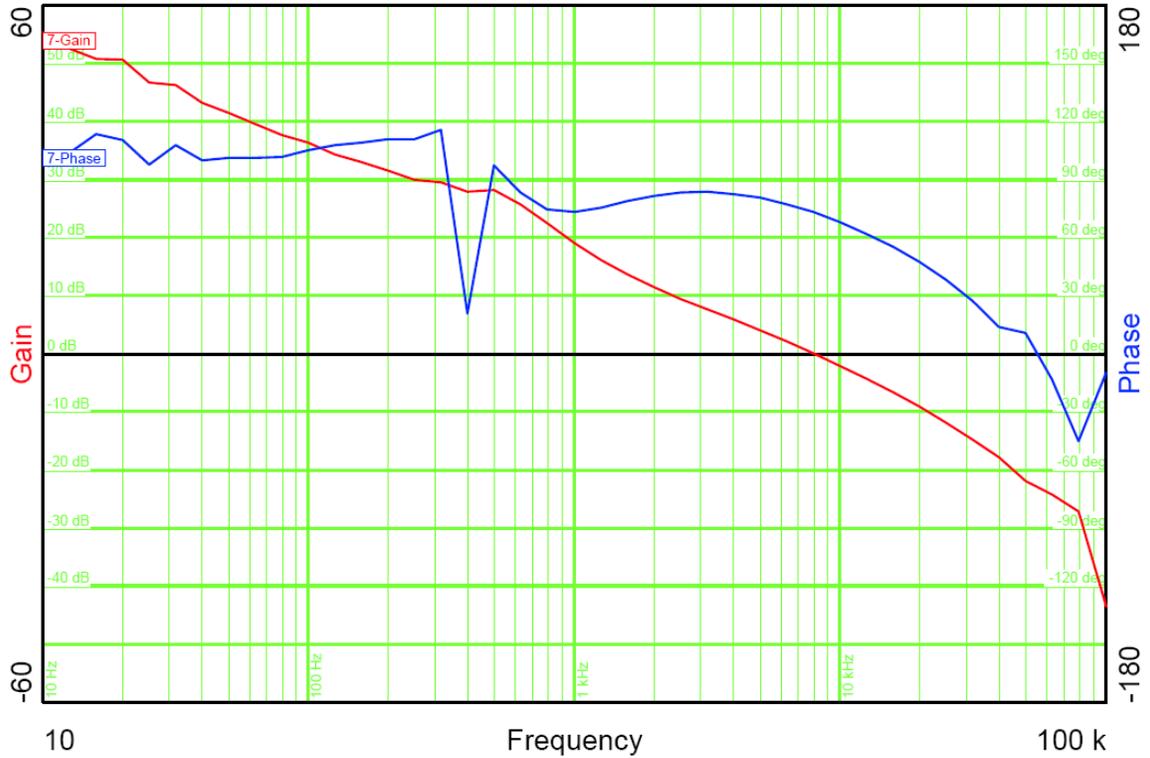


The photo below shows the 82V output response and recovery to a 30mA to 40mA step load. $V_{in} = 14V$. (1V/DIV, 20mA/DIV, 500uS/DIV)



5 Loop Gain / Stability

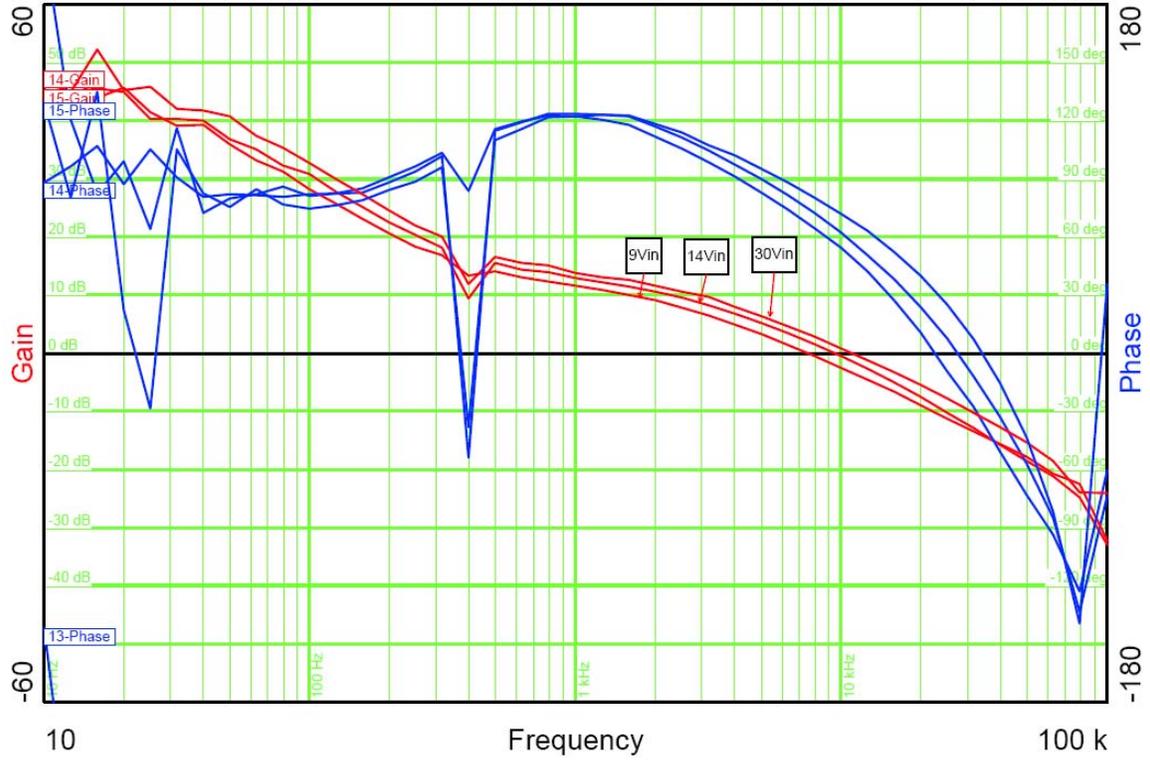
The plot below shows the 5V converter closed loop gain and phase margin. Vin = 14V, 0.5A load
Band Width = 8KHz Phase Margin = 73 degrees



The plot below shows the 82V converter closed loop gain and phase margin. Vin = 9V, 14V, 30V and max loads.

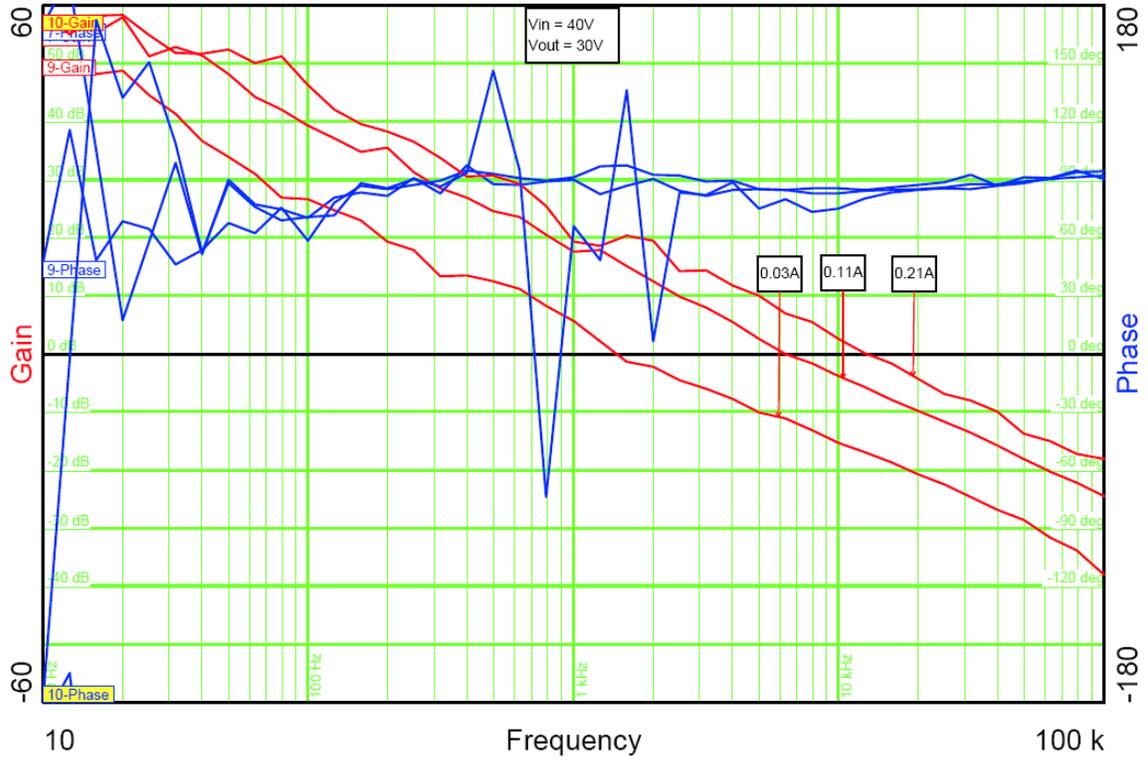
Band Width = 10KHz

Phase Margin = 60 degrees



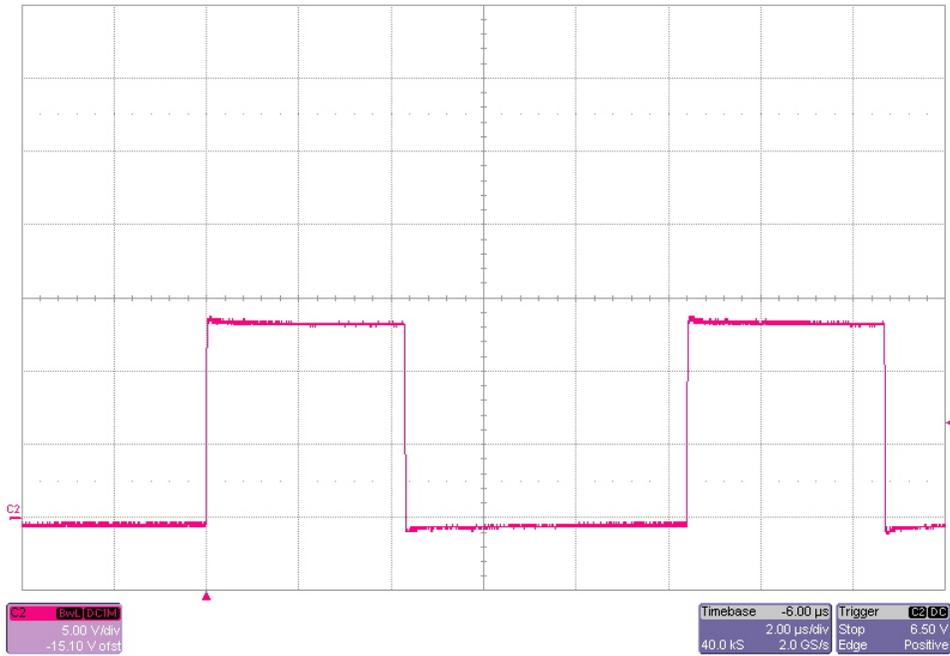
The plot below shows the 30V pre-regulator circuits closed loop gain and phase margin. $V_{in} = 40V$ and 0.03A, 0.11A and 0.21A loads.

Band Width = 12KHz (0.21A) Phase Margin = 80 degrees (0.21A)



6 Waveforms

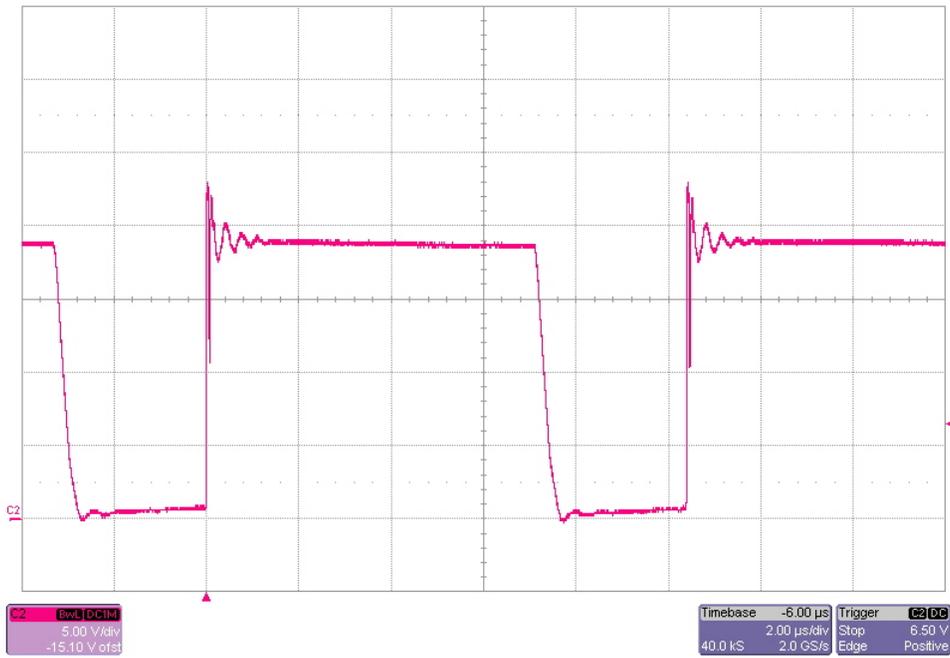
The photo below shows the switch node voltage (TP11) of the 5V converter. The dithering circuit has been disabled. The outputs were loaded to max loads. $V_{in} = 14V$. (5V/DIV, 2uS/DIV)



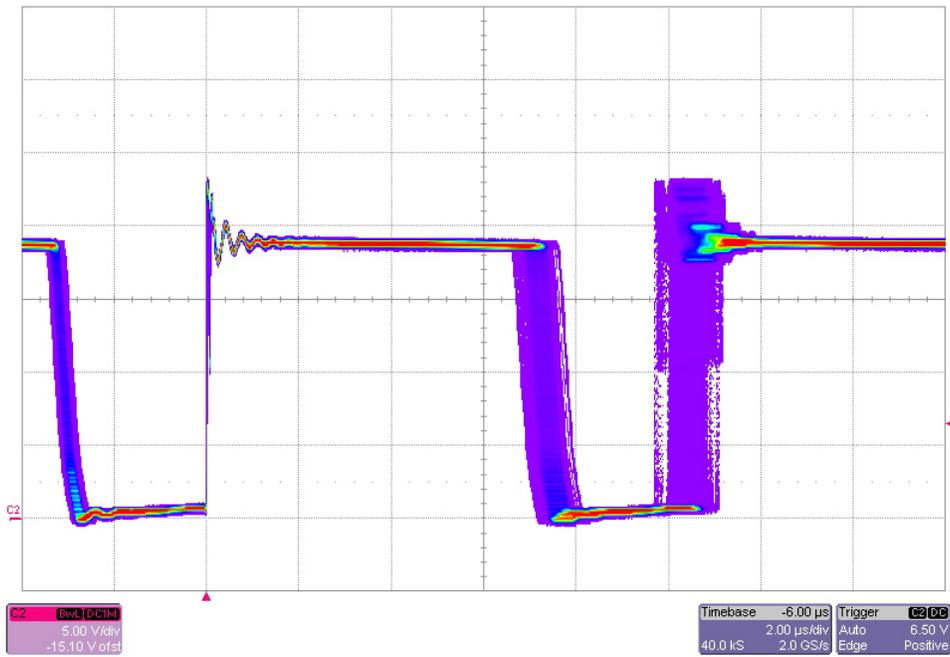
The photo below shows the switch node voltage (TP11) of the 5V converter. The dithering circuit is operational. The outputs were loaded to max loads. $V_{in} = 14V$. (5V/DIV, 2uS/DIV)



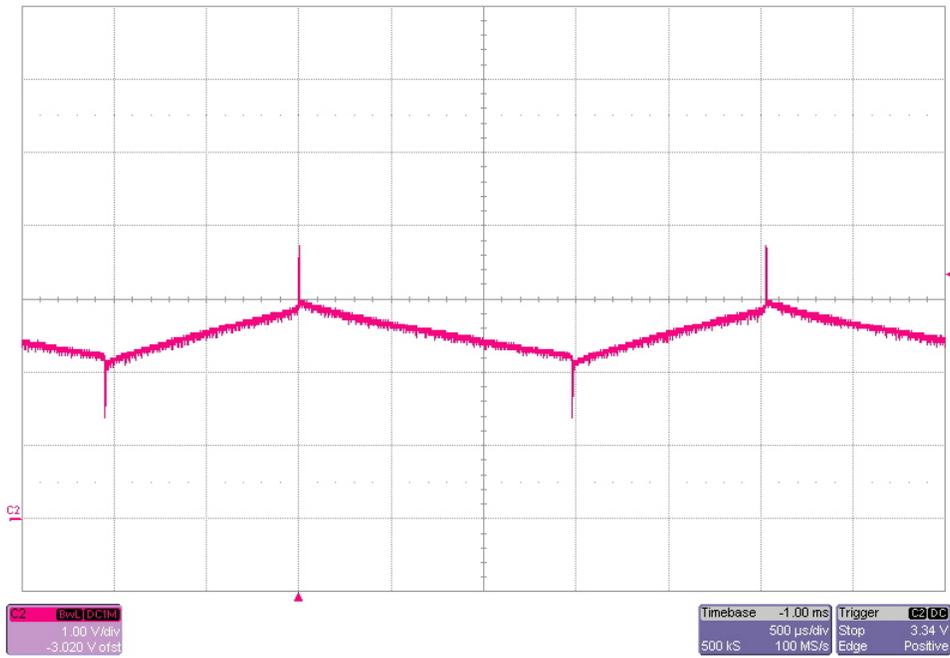
The photo below shows the switch node voltage (TP6) of the 82V converter. The dithering circuit has been disabled. The outputs were loaded to max loads. $V_{in} = 14V$. (5V/DIV, 2 μ S/DIV)



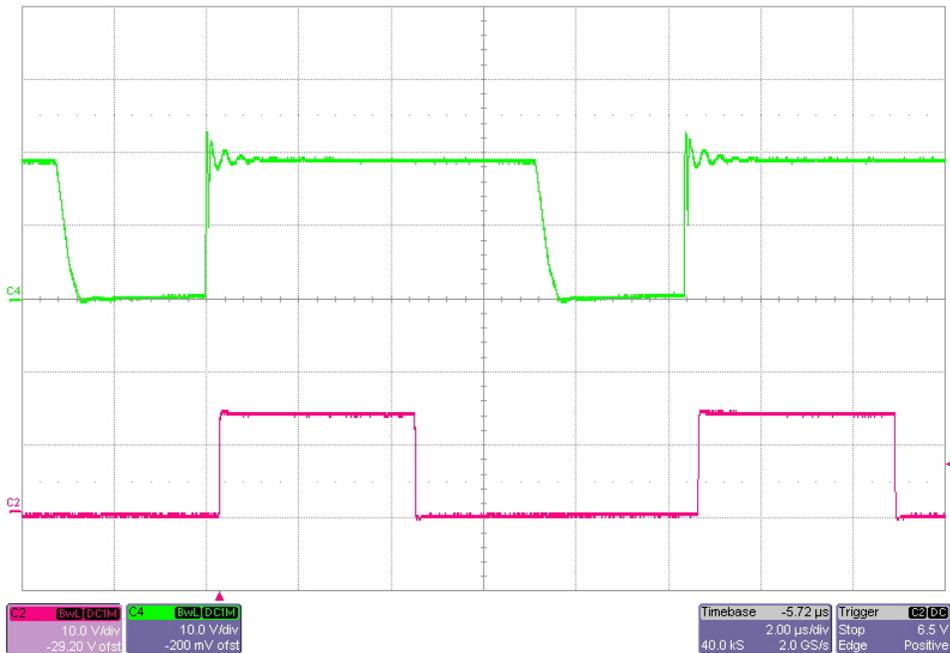
The photo below shows the switch node voltage (TP6) of the 82V converter. The dithering circuit is operational. The outputs were loaded to max loads. $V_{in} = 14V$. (5V/DIV, 2 μ S/DIV)



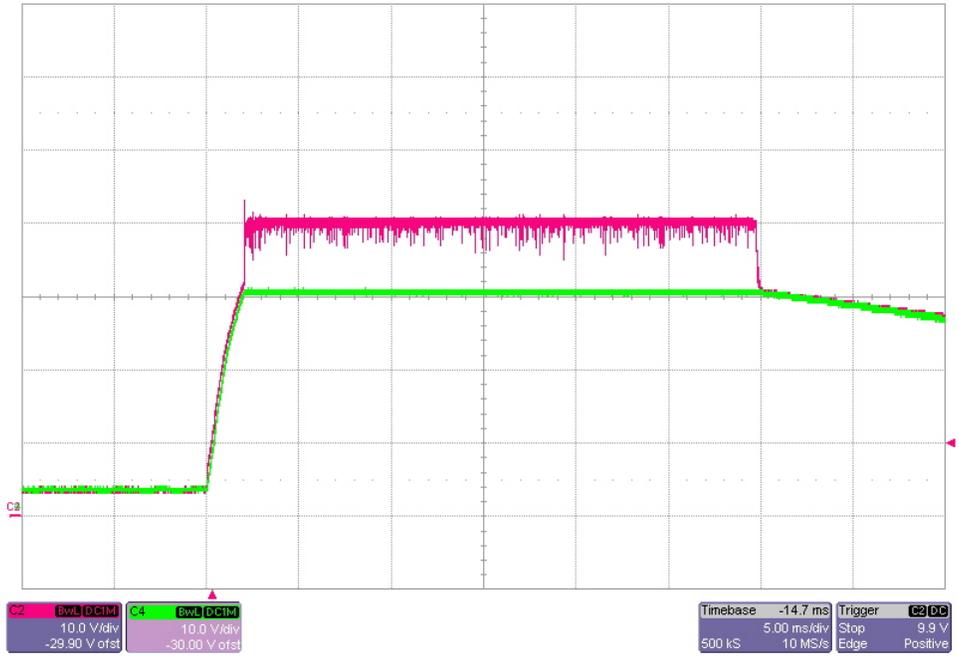
The photo below shows the dither oscillator voltage present on U2 - pin1. Vin = 14V. frequency = 400Hz (1V/DIV, 500uS/DIV)



The photo below shows the synchronous operation of the 82V flyback converter and the 5V buck converter. The dither circuit is operational (single scope capture). The output voltages are loaded to max. Vin = 14V. (10V/DIV, 2uS/DIV)



The photo below shows the input voltage to the module and the output of the “input clamping circuit” with the application of a 40V input. The output voltage was measured at L1 (switcher side). A 1 Ohm resistor was added in series with the input voltage to limit inrush current through Q6. (10V/DIV, 5mS/DIV)



The photo below shows the 5V output voltage when turned off by the SHUTDOWN input. The LOWBAT transitions low below its set point of 3.3V. The 5V output was loaded to 0.2A and Vin = 14V. (5V = 1V/DIV, LOWBAT = 2V/DIV, 1mS/DIV)



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