The Implication of Synchronous Rectifiers to the Design of Isolated, Single-Ended Forward Converters

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ABSTRACT

Synchronous rectification is a commonly used technique to improve the efficiency of DC/DC converters with low (<=5V) output voltages and high output currents. Control of the synchronous rectifiers in forward converters has been accomplished in many different ways, from self-driven to complexly controlled techniques. Most existing control techniques allow the synchronous rectifier's body diode to conduct for some small time interval, thus degrading efficiency. The focus of this design review is a new control technique that virtually eliminates body diode conduction in synchronous rectifiers. Measurement results from a 30W resonant reset forward converter will complement the paper.

I. INTRODUCTION

Forward converters have traditionally been used for low output voltage DC/DC converters, particularly for the telecom input voltage range of 36 to 75V. The reasons behind this topology choice are many and varied. The forward converter has only a single primary side switch, which is ground referenced, and several transformer reset methods are available. The control loop dynamics are well understood by extending the control models of standard buck converters. Although the forward topology has been quite popular, it has limitations. As the output voltage is decreased, the efficiency of the forward topology becomes limited by the output rectifier's loss. The rectifier loss, which is essentially the forward drop of the rectifier times the output load current, becomes the dominant loss in the converter in high current, low voltage applications. Although there have been good improvements in Schottky diode technology, synchronous rectification is needed to realize higher efficiency.

Manufacturers of power MOSFETs have responded by marketing very low on resistance, low voltage devices in compact packages. MOSFETs suitable for synchronous rectification with less than 3mΩ on resistance have been reported[2]. As a result, the only major decision the designer is left with is how to control the synchronous rectifiers.

II. FORWARD CONVERTER WITH DIODE RECTIFICATION

A. Transformer Reset Options

Before discussing synchronous rectification, it would be beneficial to look at the forward converter using conventional diode rectification. The basic power stage of a forward converter with diode rectification is shown in Fig. 1.

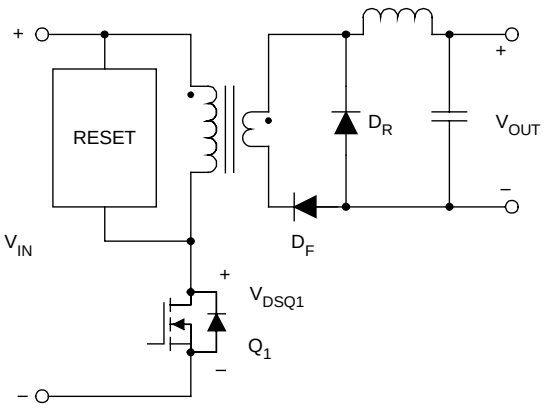

Fig. 1. Forward converter with diode rectification.

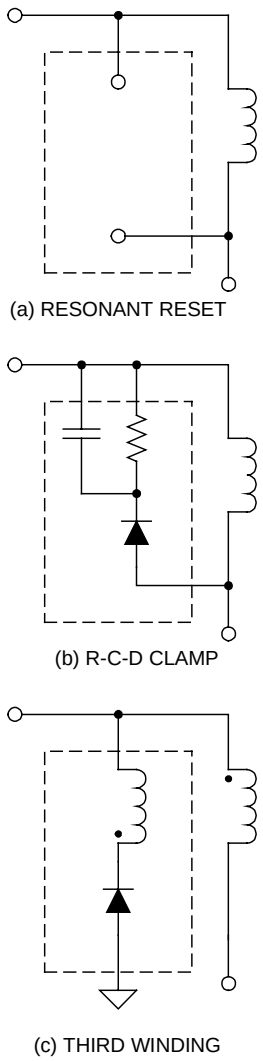

Fig. 2. Possible reset mechanisms.

There are several possible reset mechanisms, as shown in Fig. 2. These are (a) Resonant Reset, (b) R-C-D Clamp, and (c) Third Winding.

While all of these techniques allow for resetting the transformer magnetizing current during the off time of the main switch Q_1, the method and the amplitude to which magnetizing current is reset is different for each topology. In the Resonant Reset technique, the magnetizing current is reset to negative amplitude through the resonant capacitance, which is primarily equal to the C_{OSS} of Q_1 added to the junction capacitance of D_F [1]. This negative value is equal to one-half the peak-to-peak magnetizing current. The R-C-D clamp is very similar, except that it is the clamp voltage that drives the transformer magnetizing current negative.

Therefore, in the R-C-D clamp, the magnetizing current will cycle between negative and positive peak values, which are not necessarily equal to one half of the peak-to-peak magnetizing current. In the traditional Third Winding Reset technique, the magnetizing current is first reset to zero by the third winding, but resonance between the magnetizing inductance and the C_{OSS} of Q_1 will drive the magnetizing current negative. This negative magnetizing current will play an important role when synchronous rectification is applied to the forward converter.

Waveforms that show the primary MOSFET Q_1 drain-to-source voltage and the transformer magnetizing current for an R-C-D Clamp forward converter are shown in Fig. 3.

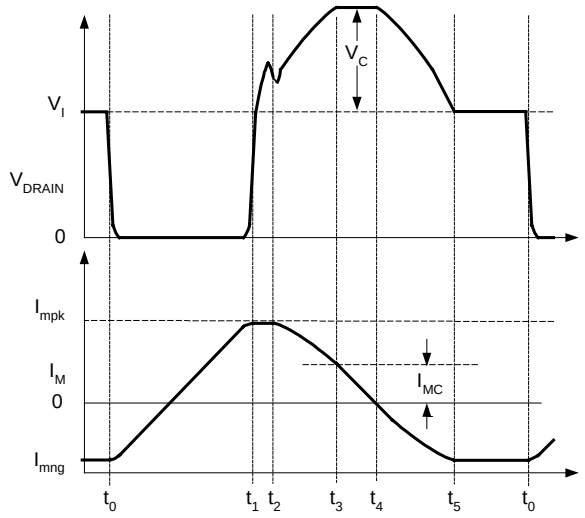

Fig. 3. Primary MOSFET Q_1 drain-to-source voltage and the transformer magnetizing current for an R-C-D clamp forward converter.

Two time intervals are of particular interest. First is the interval from t_1 to t_2, where the transformer leakage inductance resonates with the primary side capacitances and second, the dwell interval from t_5 to t_0.

At t_1, the drain voltage on the primary side MOSFET reaches the input voltage. At this time, the current on the secondary side is flowing through the forward diode D_F and the transformer has zero volts across both the primary and secondary windings. Right after t_1, the freewheeling diode D_R starts to conduct some current and the current in D_F starts decreasing so that the total current flowing in the two diodes is

equal to the inductor current. As soon as D_R begins to conduct current, the transformer secondary is shorted by the conduction of both diodes. With the transformer secondary shorted, the magnetizing current is constant while the total transformer leakage inductance resonates with the primary side capacitances. During this resonance, the transformer primary current decreases from a peak value of the peak magnetizing current plus the reflected inductor current to the peak magnetizing current. The secondary current changes from the peak inductor current to basically zero current. Since the primary and secondary currents change during the resonance seen on the primary side, the current transfer from D_F to D_R is complete after a half-resonant cycle is seen on the primary side MOSFET drain voltage. At t_2, the voltage across D_F starts to resonate, as D_F is reverse biased. Put another way, the transfer of current between the rectifiers is controlled by the total transformer leakage inductance and the primary side capacitances. As seen by the secondary side, this adds a delay between the primary side gate drive signal and the voltage across D_F resonating.

The dwell time interval from t_5 to t_0 will be very important when synchronous rectification is used in the forward converter topology. As described earlier, the transformer has negative magnetizing current at this time, i.e. current is flowing out of the dotted terminal in Fig. 1. Recognizing that this current cannot flow on the primary side, the magnetizing current must flow on the secondary side through D_F. At t_5, the primary side switch drain voltage has resonated down to the input line voltage, and is clamped by the forward diode conducting the magnetizing current. The forward diode conducts the magnetizing current throughout the dwell time interval, until the primary side MOSFET is switched on at t_0.

Experimental waveforms from[1] for the primary side MOSFET drain voltage and the transformer magnetizing current are shown in Fig. 4. Fig. 5 shows both the transformer's primary and secondary currents as well as the drain-to-source voltage of the primary side MOSFET.

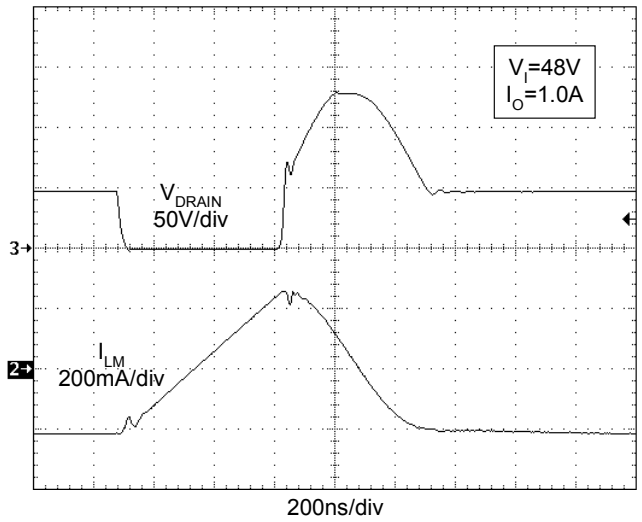

Fig. 4. Primary MOSFET Q1 drain-to-source voltage and transformer magnetizing current.

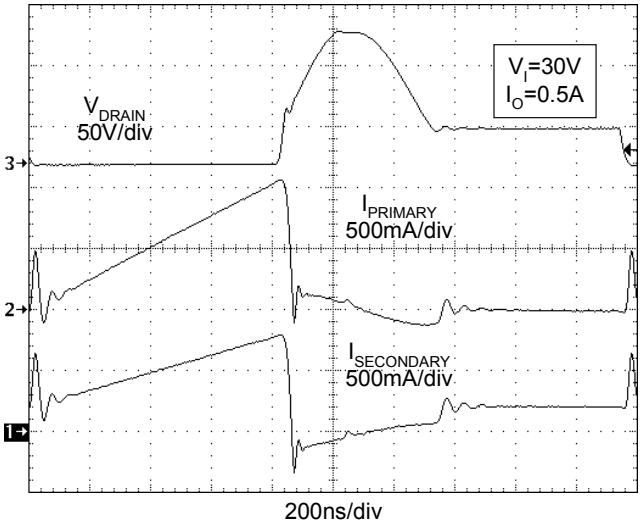

Fig. 5. Primary MOSFET Q1 drain-to-source voltage and transformer primary and secondary currents.

B. Rectifier Reverse Recovery and Conduction Losses

Prior to Q_1 being switched on, the inductor current is flowing mostly through D_R, which has stored junction charge. Because this charge cannot be removed instantaneously, the anode-to-cathode voltage will remain constant as Q_1 is switched on. The input voltage is then placed across the transformer leakage inductance and the current in D_R decreases at a rate determined by the input voltage and leakage inductance. The input voltage magnitude and the transformer

leakage inductance determine the dI/dt in D_R and therefore also determine the reverse recovery of D_R. After the stored charge is removed from D_R, the transformer leakage inductance resonates with the junction capacitance of D_R.

The forward diode also experiences reverse recovery. This occurs at t_2 in Fig. 3, immediately after the current is commutated from D_F to D_R. As discussed earlier, the dI/dt in both D_F and D_R is set by the resonance between the transformer leakage inductance and the primary side resonant capacitance. As the current is decaying to zero in the forward diode D_F, the dI/dt is decreasing in magnitude, which makes the reverse recovery of D_F less severe than the reverse recovery of D_R. Schottky diodes naturally have excellent reverse recovery characteristics, and when these are used for D_F, the reverse recovery will be barely noticeable; however, when MOSFETs are used in place of D_R and D_F, the poor reverse recovery characteristics of the body diodes will become apparent.

III. Self-Driven Synchronous Rectification

The self-driven drive scheme is the simplest synchronous rectifier drive scheme and is pictured in Fig. 6.

The two diodes D_F and D_R are replaced with MOSFETs Q_F and Q_R. In the self-driven technique, the voltage across the transformer secondary is used to drive the gates of the synchronous rectifiers Q_R and Q_F. Although not shown in Fig. 6, separate windings on the secondary side of the transformer can be used to drive the forward synchronous rectifier Q_F and/or the freewheeling synchronous rectifier Q_R[3,4]. This is usually done to allow a different turns ratio from the primary winding to the gate drive winding(s), allowing synchronous rectification to be used for higher or lower output voltages.

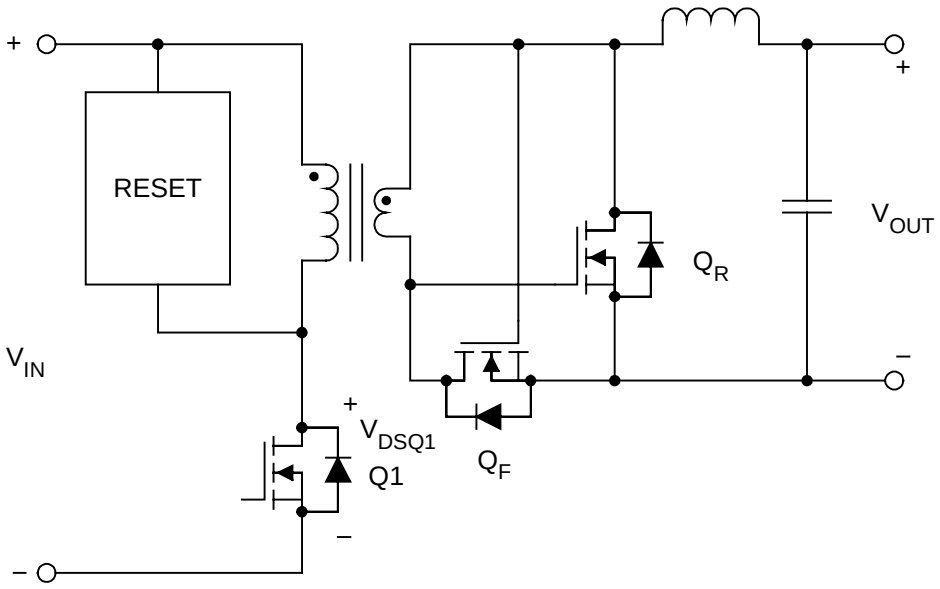

Fig. 6. Forward converter with self-driven synchronous rectifiers.

A. Implications and Trade-Offs of Self-Driven Synchronous Rectification for Resonant Reset Forward Converters.

Fig. 7 displays the waveforms for a resonant reset forward converter with self-driven synchronous rectifiers operating in continuous conduction mode. Shown are the drain-to-source voltages of Q_F and Q_R, as well as the primary side MOSFET Q_1 drain-to-source voltage.

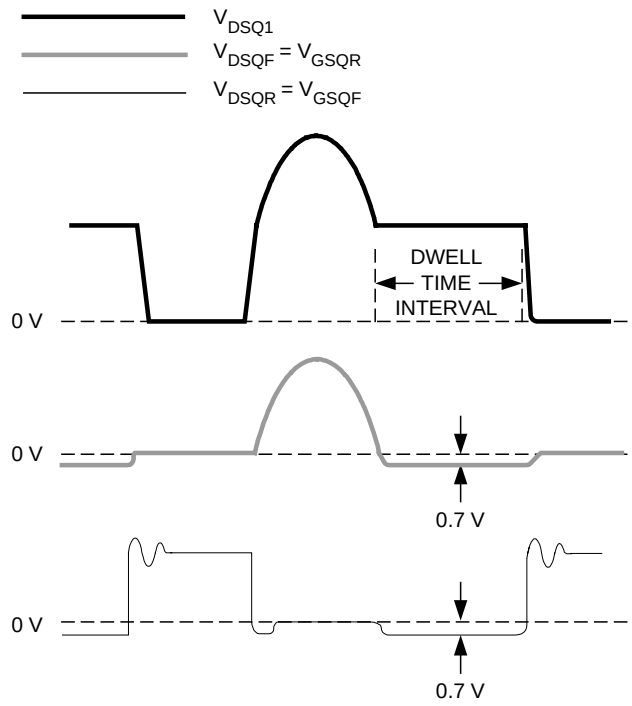

Fig. 7. Typical waveforms for self-driven synchronous forward converters with resonant reset.

The first problem with self-driven synchronous rectification is the conduction intervals for the body diodes of Q_F and Q_R. In an optimum converter, the resonant reset will occur during the entire off-time of the primary side MOSFET Q_1, meaning that at low input line, the Q_1 drain voltage will just return to the input voltage before Q_1 is turned on again. At low line, the converter will be operating at the maximum steady state duty cycle, D_{MAX}, for the converter. Assuming that the converter is to be designed over a 2:1 input range, and that the duty cycle will be inversely proportional to the input line voltage, the steady state operating duty cycle at high line will be $0.5 \cdot D_{MAX}$. In resonant reset converters, the reset time interval does not change over line variations, meaning that the dwell time interval will be $0.5 \cdot D_{MAX}$. It becomes clear then, even for converters operating at a maximum of 50% duty cycle that the dwell time interval will be as high as 25% of the entire switching cycle.

Looking again at Fig. 7, during the dwell time interval, the body diodes of both Q_F and Q_R are conducting. The forward MOSFET is conducting the reflected negative magnetizing current, while the freewheeling MOSFET carries the difference of the inductor and the forward MOSFET currents. Conduction of the Q_R body diode for this long time interval is very undesirable as the losses will be high. Also, since the body diode is carrying a large current, the reverse recovery will be severe when the primary side MOSFET Q_1 is turned on. The forward MOSFET will also experience conduction losses during the dwell time interval due to the conduction of the magnetizing current through the body diode. However, since the magnetizing current is usually much smaller than the load current, this loss isn't as high as in the freewheeling switch.

A second problem with self-driven synchronous rectification is the $R_{DS(on)}$ variation over the line voltage range. Low voltage MOSFETs suitable for self-driven synchronous rectification typically have an $R_{DS(on)}$ rated at $V_{GS} = 4.5V$, and an absolute maximum V_{GS} of ±20V. The gate of the forward synchronous rectifier Q_F is driven with a voltage proportional to the line voltage, while the freewheeling MOSFET gate is driven by a constant voltage during the reset of the power transformer. The designer must select a turns ratio N_P/N_S for the main power transformer low enough for the forward synchronous rectifier to be driven into its ohmic region at low line. The design tradeoff occurs at high line, where it is possible to exceed the maximum gate-to-source rating of the forward synchronous rectifier MOSFET. For the standard telecom input rage of 36 to 75V, a reasonable choice for the turns ratio N_P/N_S is approximately 6:1. At low line, this will give approximately 6V V_{GS} on the forward synchronous rectifier that will increase to approximately 12.5V at high line. A close

examination of the MOSFET datasheet shows a significant $R_{DS(on)}$ change over this V_{GS} range. For some MOSFETs this change can be as high as 10%. If the transformer turns ratio N_P/N_S is higher than 6:1, the $R_{DS(on)}$ variation will also be higher because the $R_{DS(on)}$ increase significantly at gate-to-source voltages less than 6V.

In self-driven synchronous rectification, the gates of the synchronous rectifiers are driven directly from the transformer. The current to turn the rectifiers on and off comes efficiently from the input line. The average current to drive the forward synchronous rectifier will vary proportionally to the switching frequency and proportionally to the gate-to-source voltage. Therefore, over a 2:1 line voltage change, the average current required to drive the forward synchronous rectifiers will also change 2:1. Since the freewheeling synchronous rectifier is driven with a constant gate-to-source voltage, the charge and average current required is constant over the line voltage.

Another drawback of using self-driven synchronous rectifiers in place of diode rectification is the loading of the resonant reset circuit. Fig. 8a shows the capacitances of the resonant circuit, and Fig. 8b shows the equivalent resonant capacitances and inductances reflected to the primary side.

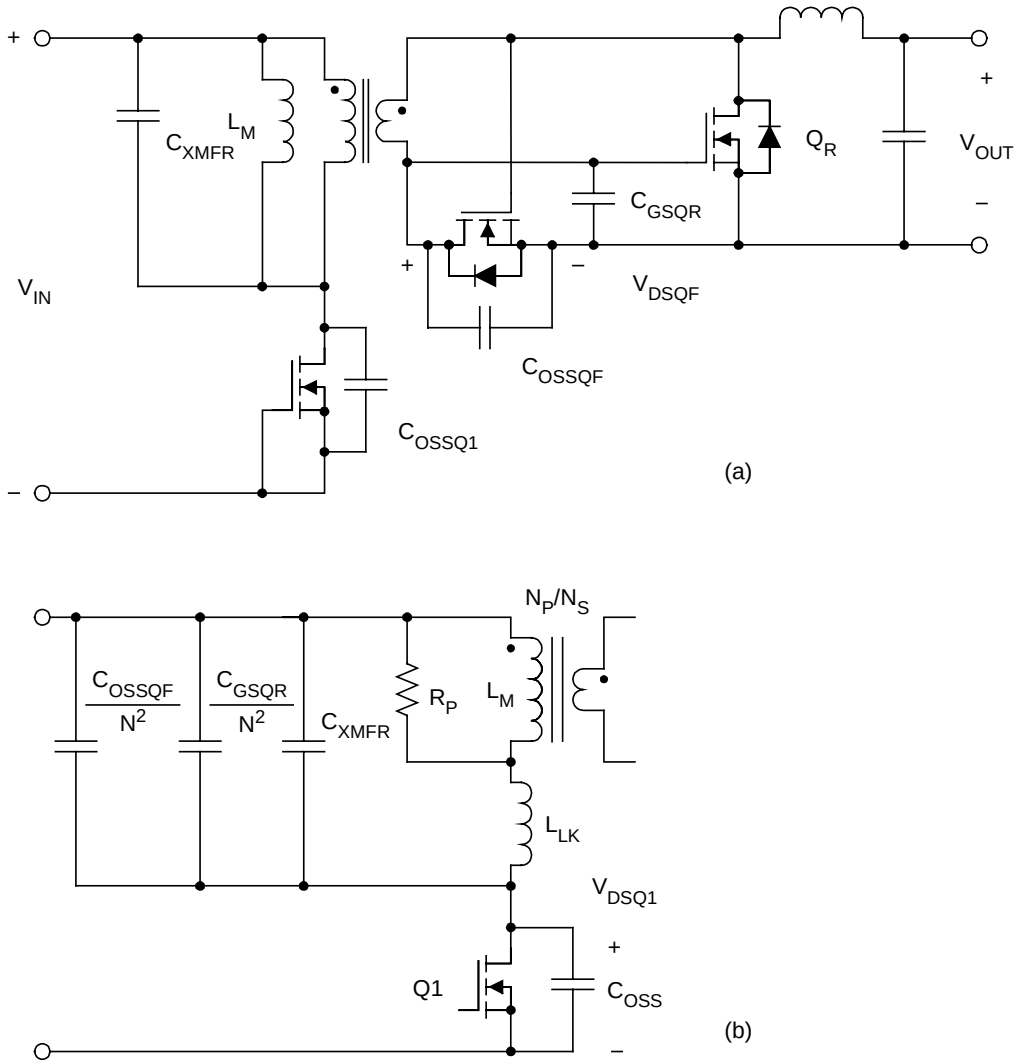

Fig. 8. Capacitances of the resonant circuit (a) and equivalent resonant capacitances and inductance reflected to the primary side (b).

During the reset time interval, the V_{DS} of Q_F has a resonant half-sine wave voltage on it. It can be seen that the gate-to-source capacitance of Q_R and the C_{OSS} of Q_F will load the resonant reset circuit. The net effect of this loading is to extend the time duration of the reset time interval, assuming the transformer magnetizing inductance is kept constant. If the duty cycle needs to be kept constant after adding the self-driven synchronous rectifiers, the magnetizing inductance may have to be decreased, which will result in a shorter reset time, and a higher peak reset voltage. Decreasing the magnetizing inductance will also increase the circulating losses, as more energy will be stored in the transformer.

IV. CONTROL-DRIVEN SYNCHRONOUS RECTIFICATION

After examining the self-driven technique, attention turns to control-driven synchronous rectification. Control-driven techniques are generally more complex than self-driven; however, control-driven techniques can overcome all the limitations of self-driven techniques. Body diode conduction can be eliminated and using precise timing circuitry can minimize reverse recovery losses. Furthermore, the gate drive voltage can be set to an optimum level to minimize $R_{DS(on)}$ while minimizing the gate charge required. The gate drive voltage can be regulated independent of the line voltage. All of these benefits come with the cost of added control complexity.

Knowing the limitations of self-driven synchronous rectification, begin by drawing the desired waveforms for the synchronous rectifier gates with respect to the available control signals. Fig. 9 shows the two synchronous rectifier gate-to-source voltages, drain-to-source voltages, as well as the primary side drain-to-source voltage and PWM CONTROL signals.

Note that the PWM CONTROL signal could be either primary or secondary side referenced, it makes no difference to the waveforms in Fig. 9.

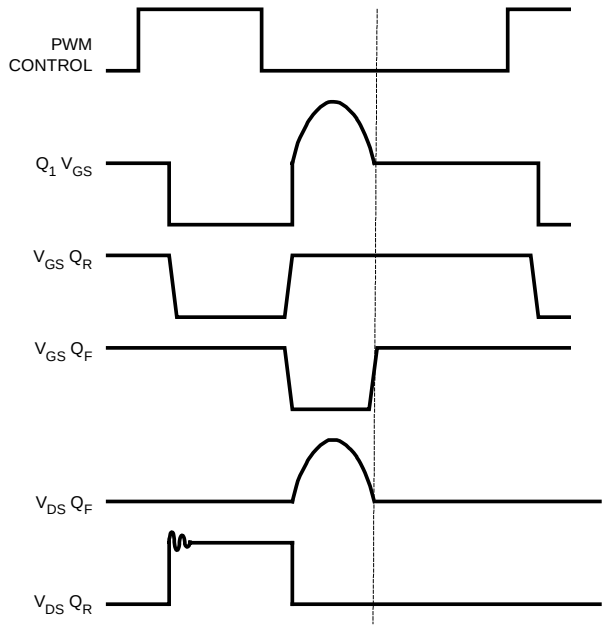

Fig. 9. Control-driven synchronous rectification waveforms.

Why not drive the forward synchronous rectifier Q_F with the PWM CONTROL signal, and the freewheeling synchronous rectifier Q_R with an inverted PWM CONTROL signal? The answer lies first in the time delay between the PWM CONTROL signal and changes in the power stage voltages and currents. When the PWM CONTROL signal originates on the secondary side, it is too far time advanced from changes in the power stage voltage and currents. However, if the PWM CONTROL signal is primary side referenced, it must be brought across the isolation boundary. Depending on how the PWM CONTROL is transmitted from the primary to the secondary side, the resulting signal on the secondary side may be too far time advanced or time retarded. Also, as described previously, it would be desirable to allow both synchronous rectifier channels to conduct during the dwell time interval. Unfortunately this requires overlapping gate drive signals. The time interval when both rectifiers are conducting will vary with line voltage and any changes in parasitic capacitances and inductances. Possibly the optimal solution then, is to use power stage information to determine when the forward synchronous rectifier should be turned on. Examining Fig. 9 closely, Q_F should be turned on exactly when its drain-to-source voltage reaches zero volts. This would allow the

magnetizing current to be conducted by the channel instead of the body diode, eliminating the conduction loss of the body diode. If Q_F is turned on at this time, it will remain on when the primary side MOSFET Q_1 is turned on, and the turn off of Q_F will need to be synchronized to the turn off of Q_1.

Control of Q_R needs to be synchronized to the rectified transformer voltage. As soon as the transformer voltage that is rectified by Q_F falls to zero volts, Q_R needs to be turned on. Ideally, the gate-to-source voltage of Q_R would be approaching its threshold voltage as the drain-to-source voltage of Q_R is falling to zero. This would allow for minimum body diode conduction of Q_R during this time interval. The turn off of Q_R is a very different situation. In the self-driven technique, the channel of Q_R is turned off as the resonant voltage across the drain-to-source of Q_F falls below the threshold voltage of Q_R. The current that was flowing through the channel of Q_R now must flow through the body diode, and when Q_1 is turned on, a high loss reverse recovery will take place. With control-driven synchronous rectification, the goal is to minimize this body diode conduction by actively controlling the turn off of Q_R.

V. CONTROL-DRIVEN IMPLEMENTATION

To minimize conduction and reverse recovery losses, the synchronous rectifiers require precise timing circuitry. Although there are several ways to generate these control signals, a feedback system to actively control the timing of the gate drive signals will be used. The key advantages are that the circuit will adjust for component variation, particularly the uncontrolled capacitances in the synchronous rectifier MOSFETs, and timing delays and the temperature dependence of MOSFET thresholds are also corrected for by this feedback loop.

To control the gate timing, the programmable delay block pictured in Fig. 10 will be used. This delay block is comprised of three main elements; a delay line, a multiplexer (MUX), and a logic AND gate. An input signal to the delay line is delayed several nanoseconds for each delay element. In order to generate a controlled turn-on delay, the MUX selects which delay element to take the output signal from. Finally, the AND gate ensures that the delay is applied to the turn-on (rising) edge only. Control of the delay from IN to OUT is performed by the digital control bus applied to the MUX address input. If the control bus is set to all ones, a maximum delay is seen from IN to OUT. Conversely, if the control bus is set to all zeros, there is practically no delay from IN to OUT. Several different delay blocks can be constructed, giving either a turn-on delay only, a turn-off delay only or symmetric turn-on and turn-off delays. Not shown in Fig. 10 is a voltage sensing circuit and digital controller. For different implementations of the delay cell, different voltage sensing circuits and digital controllers will be used.

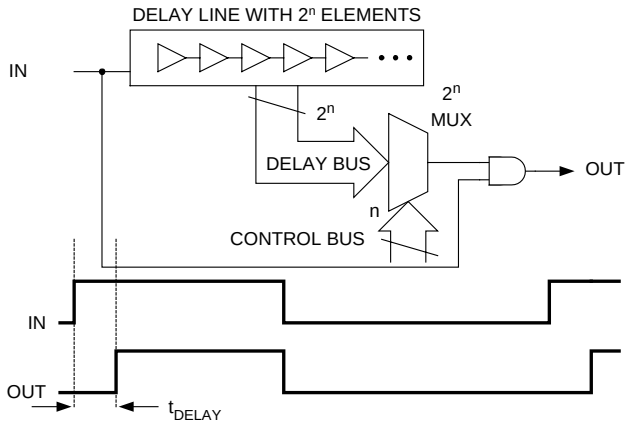

Fig. 10. Delay block.

A. Control-Driven Q_R Implementation

The control-driven circuit design starts with the freewheeling MOSFET Q_R, which should be turned on as soon as its drain-to-source voltage falls to zero. One simple way to accomplish this would be to use a comparator to sense when the drain-to-source voltage of Q_R crosses zero volts. The problem with this method arises when the delay through the comparator, logic, and gate driver are considered. Even with very fast circuitry, this delay can amount to 50ns or more, during which the body diode is conducting and incurring high conduction losses. One logical answer to the inherent time delay from sensing the falling drain-to-source voltage to when the MOSFET is turned on is to use information from the last switching cycle to predict when to turn on the MOSFET. In this anticipatory way, the

MOSFET gate voltage can start increasing before the drain-to-source voltage has fallen. By timing the gate voltage to rise to the MOSFET threshold voltage when the drain-to-source voltage is falling to zero volts, the body diode should never conduct.

Fig. 11 shows the control circuitry to turn Q_R on and off. It uses two multiplexers, two counters, one delay line and glue logic to control the turn-on and turn-off so that body diode conduction is minimized. The circuit description will begin with the turn-on delay portion. The PWM CONTROL signal drives the primary side MOSFET Q_1 and is also fed into the delay line. When the power supply is first started, the LOAD input to the counters is high which sets the turn-on delay counter to all ones, and sets the turn-off delay counter to all zeros. With the counters initialized in this state, the output from the control circuit to the gate driver results in maximum turn-on delay and minimum turn-off delay. With the delays set to these values, the body diode of Q_R will conduct, and the feedback loops will start to adjust the delays to minimize its conduction. Fig. 12 (a) and (b) shows the gate-to-source and drain-to-source voltages of Q_R during the turn-on of Q_R. Fig. 12 (a) shows the circuit operation when the turn-on of Q_R is delayed too long, and Fig. 12 (b) shows optimal timing delay.

To adjust the turn-on delay, a NOR gate with an approximate input threshold of 2V is used to detect when the gate-to-source voltage and drain-to-source voltage of Q_R are both simultaneously low. A high output from the NOR gate indicates to the controller that the delay was too long, and the controller will decrease the delay for the next switching cycle.

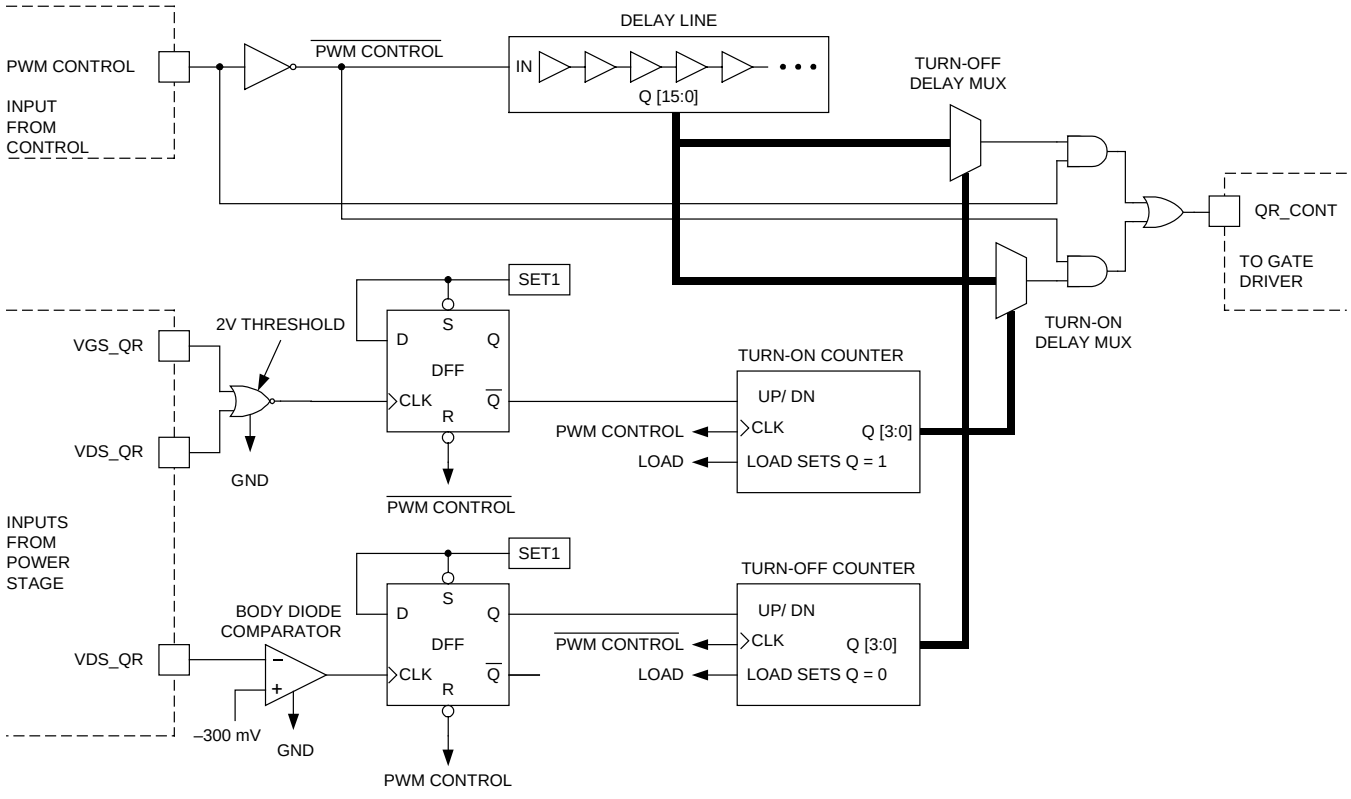

Fig. 11. Q_R control circuitry.

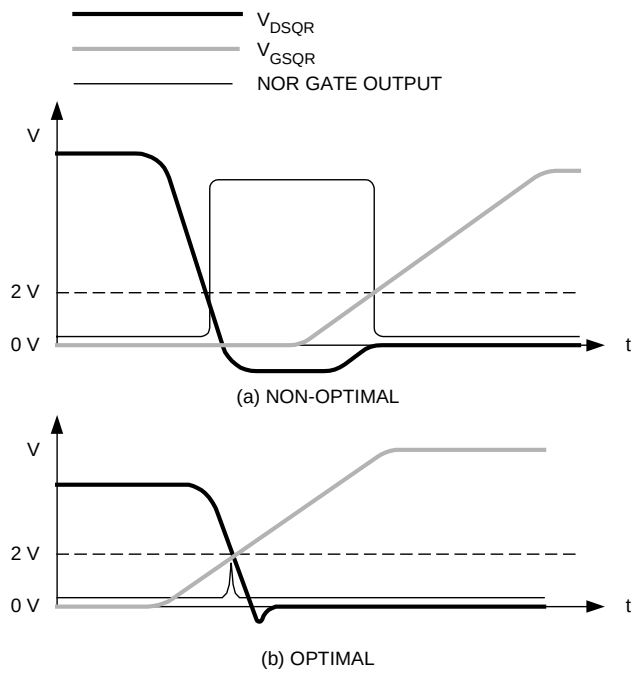

Fig. 12. Q_R turn-on waveforms.

The NOR gate output is latched, inverted, and is fed into the turn-on delay counter's UP/DOWN input. This signal tells the counter to either count up or count down. If the NOR gate's output was high, then the counter will count down, decreasing the delay, while a low NOR output will result in the counter counting up, increasing the delay. The counter effectively holds this delay information for the next cycle. The feedback loop will then adjust the turn-on delay to be shorter until the NOR gate no longer has an output pulse. When the converter is operating at a constant load and line, the turn-on delay for the next cycle will be slightly too long, the NOR gate will give a high output pulse, and the delay will be shortened. In this way, the circuit dithers the delay between two values, one too long, and one very close to optimum.

The turn-off controller operates in a very similar manner to the turn-on controller. The differences reside in the voltage sensing circuit and the direction that the counter counts. A high speed comparator is used to sense when the body diode is conducting. For improved accuracy, a comparator is used to detect body diode conduction instead of the NOR gate. During the turn-on interval, current is commutating from the forward synchronous rectifier to the freewheeling synchronous rectifier. The dI/dt of this current is quite high, and ringing is usually seen on the drain-to-source voltage of Q_R. If a comparator is used for detecting the body diode conduction during the turn-on of Q_R, there could be false triggering due to the ringing drain-to-source voltage. During the turn-off of Q_R, the current is constant through the Q_R MOSFET device, as the current is flowing through either the channel or the body diode. There is very little ringing during the turn-off, and a comparator is used for improved accuracy. The threshold of the comparator must be slightly negative to prevent false triggering of the comparator when the MOSFET channel is conducting.

The drain-to-source voltage during channel conduction is approximately equal to $-I_{LOAD} \cdot R_{DS(on)}$, and allotting for noise, the comparator threshold is set to approximately -300mV. The comparator compares the drain-to-source voltage of Q_R to this fixed threshold and a high output from the comparator indicates to the controller that the body diode is conducting and the delay needs to be increased. This is exactly opposite from the turn-on scenario, because the turn-off delay counter is set to all zeros at start-up. Fig. 13 (a) and (b) show the turn-off waveforms for Q_R and the comparator output.

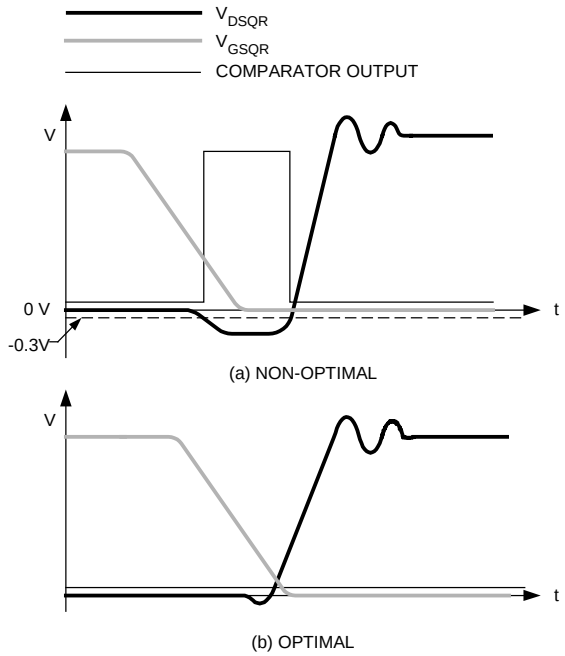

Fig. 13. Q_R turn-off waveforms.

Fig. 13 (a) shows the circuit operation when the delay is set too short, and Fig. 13 (b) shows

optimal timing delay. As in the turn-on of Q_R, the delay for the turn-off dithers between a value that is too long and an optimum value.

The question arises: can the turn-on or turn-off delays be set too short, causing cross-conduction? The answer lies in a careful study of the comparator performance and the delay per element of the delay line. Comparators can only respond to differential input voltages that are present for a sufficient amount of time to slew internal nodes. Suppose the comparator can detect body diode conduction for 5ns. During the next cycle, the delay is adjusted to reduce the diode conduction by one bit on the delay line. Of course, the comparator will not respond to the next-cycle body-diode conduction because it will be approximately 5ns minus the delay time per element on the delay line. The key to avoiding cross conduction is to set the delay per element less than the minimum detectable pulse width of the comparator.

B. Control-Driven Q_F Implementation

Control of the forward synchronous rectifier Q_F is quite different than the freewheeling synchronous rectifier Q_R. One main difference is that the goal is to turn on Q_F after the transformer is reset, which is independent of either the rising or falling edge of the PWM CONTROL signal. This is unlike the freewheeling synchronous rectifier, where the goal was to simply adjust the timing of both the rising and falling edges of the PWM CONTROL signal as needed to minimize body diode conduction in Q_R

With the understanding that the goal is to turn on Q_F after the transformer is reset, a good starting point is the circuitry required to turn on Q_F as shown in Fig. 14.

First, a high-speed body diode comparator is used to detect when the body diode of Q_F starts to conduct, which signals the end of the transformer reset time interval. Unfortunately, as shown in Fig. 15, this comparator will also detect body diode conduction right after the primary side MOSFET Q_1 is turned off.

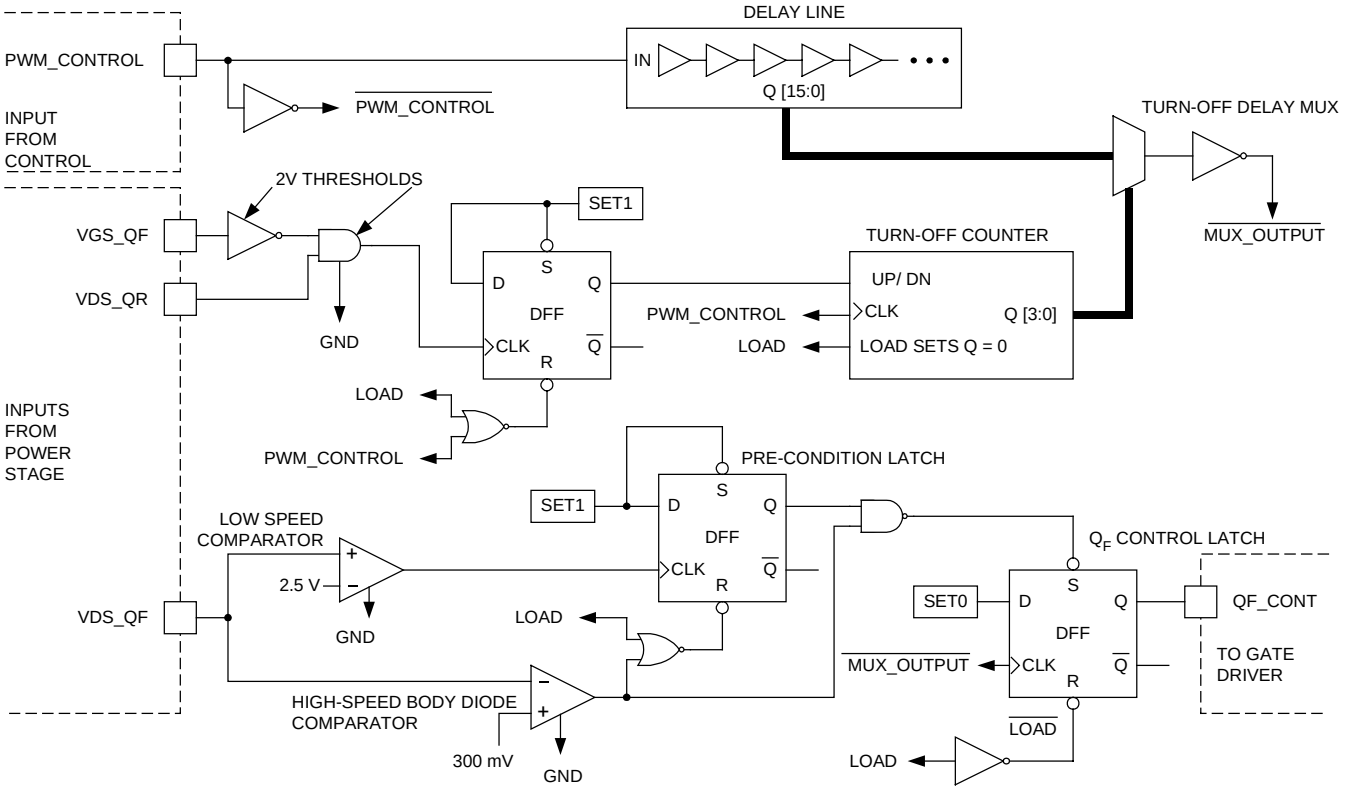

Fig. 14. Q_F control circuitry.

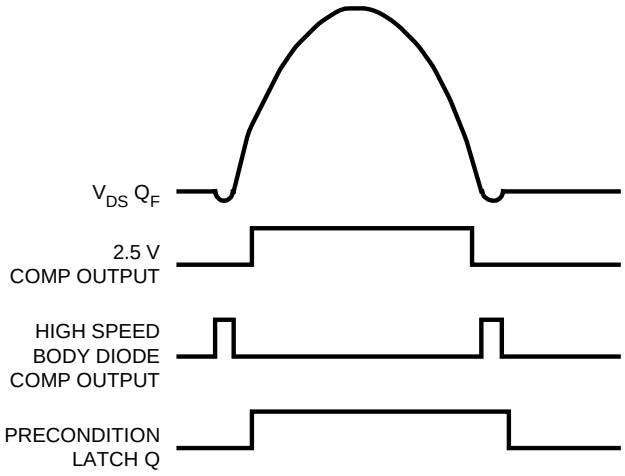

Fig. 15. Q_F pre-condition latch waveforms.

Using the comparator alone would turn on Q_F for the entire off time of Q_1, and the transformer would never be allowed to reset. To avoid this, a low speed comparator is used to detect when the drain-to-source voltage of Q_F has risen above 2.5V. When the drain-to-source voltage of Q_F has risen above 2.5V, a pre-condition latch is set, which then enables the output of the high-speed body diode comparator. As soon as the drain-to-source voltage of Q_F falls past the –300mV threshold of the body diode comparator, Q_F is turned on by setting the Q_F control latch. As soon as the high-speed comparator output goes high, the pre-conditioning latch is reset, and the turn-on circuitry is in the proper state for the next turn-on event. During the inherent delay from the body diode comparator detecting the conduction of the body diode, to the channel of Q_F turning on, the body diode conducts the magnetizing current of the transformer. Although during this time interval there is conduction loss in the Q_F body diode, this is minimal compared to the loss incurred if Q_F was held off for the entire dwell time period. To eliminate this loss completely, one would have to use the same predictive control that was used for the turn-on of Q_R. Although this is possible in theory, it is quite difficult because there is no PWM CONTROL edge present when the transformer has completely reset.

The control for the turn-off of Q_F is quite similar to the turn-on of Q_R. The turn-off circuit uses the predictive control technique, using a delay line, multiplexer and a counter as the controller. The differences between the control of the turn-off of Q_F and the turn-on of Q_R start with the type of logic gate used for the feedback loop. As shown in Fig. 14, the gate-to-source voltage of Q_F is inverted and fed into a 2-input AND gate. The other input to the AND gate is connected to the drain-to-source voltage of Q_R. Both the inverter and the AND gate have approximately 2V input thresholds. This AND gate will synchronize the falling edge of Q_F's gate-to-source voltage with the falling edge of Q_R's drain-to-source voltage.

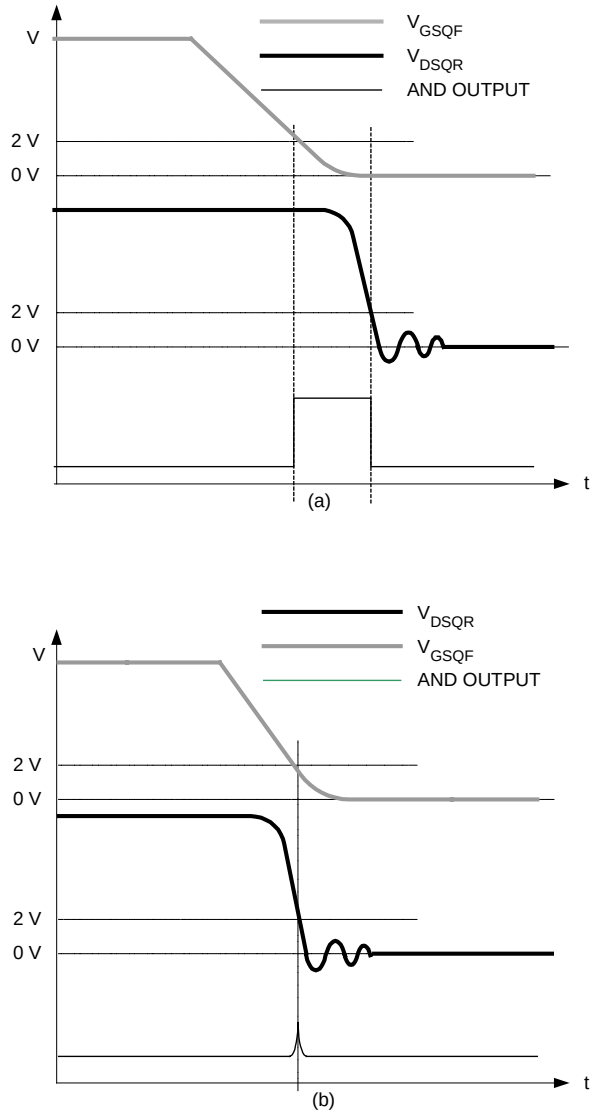

Fig. 16. Q_F turn-off waveforms.

A counter that has its output initially set to all zeros controls the turn-off circuit. With the counter's output set to all zeros, virtually zero delay is set between the falling edge of the PWM CONTROL signal and the gate-to-source voltage of Q_F. The resulting gate-to-source voltage of Q_F, drain-to-source voltage of Q_R and the AND gate output are shown in Fig. 16 (a).

The AND gate in the Q_F turn-off circuit acts much like the NOR gate did in the Q_R turn-on control circuit, giving a command to the counter that directs the counter to count up or down. In the case of the Q_F turn-off circuit, a high output from the AND gate directs the counter to count up at the next clock cycle. When the counter increments up one count value for the next cycle, the delay between falling edge of the PWM CONTROL and the gate-to-source voltage of Q_F is increased, and the output pulse from the AND gate will be narrower. This feedback effect will continue until the gate-to-source of Q_F and the drain-to-source of Q_R are synchronized. When the delay is optimum, the waveforms are as shown in Fig. 16 (b).

As described in the Q_R control implementation, the circuit will dither between two delay values, one that is optimum and one slightly longer than optimum.

VI. Prototype Circuit

A prototype converter was constructed to verify the theoretical predictions. The tested converter operates from a 36V to 75V input line and converts this input to a 2.5V output at up to 12A. The converter's block diagram is shown in Fig. 17.

The operating frequency is fixed at 500kHz by a secondary side voltage mode controller. The Resonant Reset method is used to reset the power transformer. The breadboard is designed so that both self-driven synchronous rectification and the control-driven techniques can be investigated.

A block diagram of the secondary side control circuitry is shown in Fig. 18.

The signals from the power stage are shown on the left; these are level shifted down to 0V to 3.3V signals for the logic. The power stage signals are input into Altera® MAX7000A electrically programmable logic devices (EPLD), which contain all the control logic for the synchronous rectifiers. This allows for maximum flexibility when developing the logic to process the power stage signals and to output the desired gate drive signals. To level shift between the 0 to 3.3V logic signals and the 8V gate drive rail, high-speed 4 transistor level shifters are used. TPS2812 8-pin IC gate drivers were used with both drivers in each package paralleled for higher output current drive.

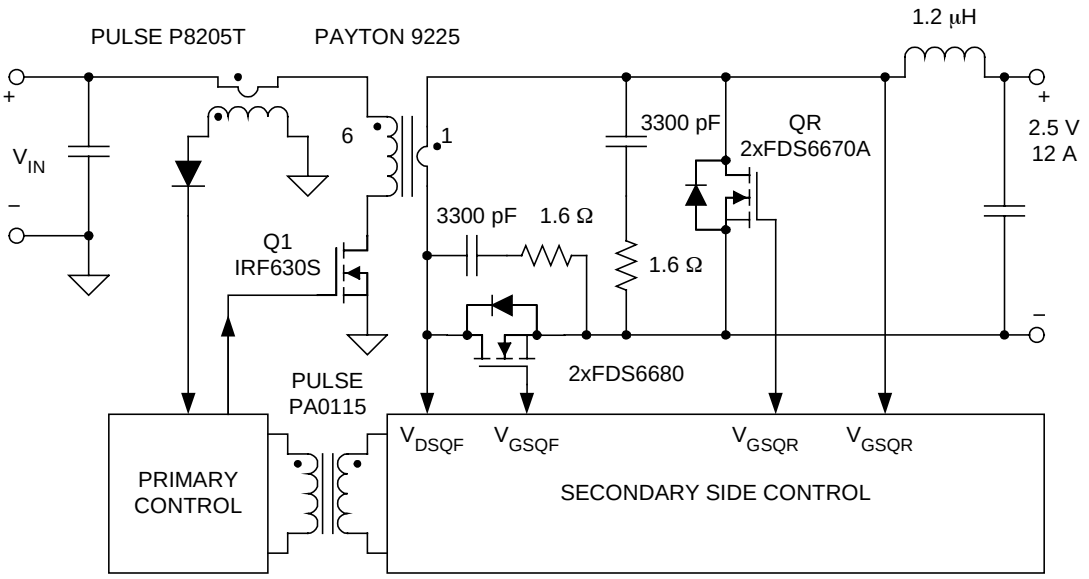

Fig. 17. Simplified prototype schematic.

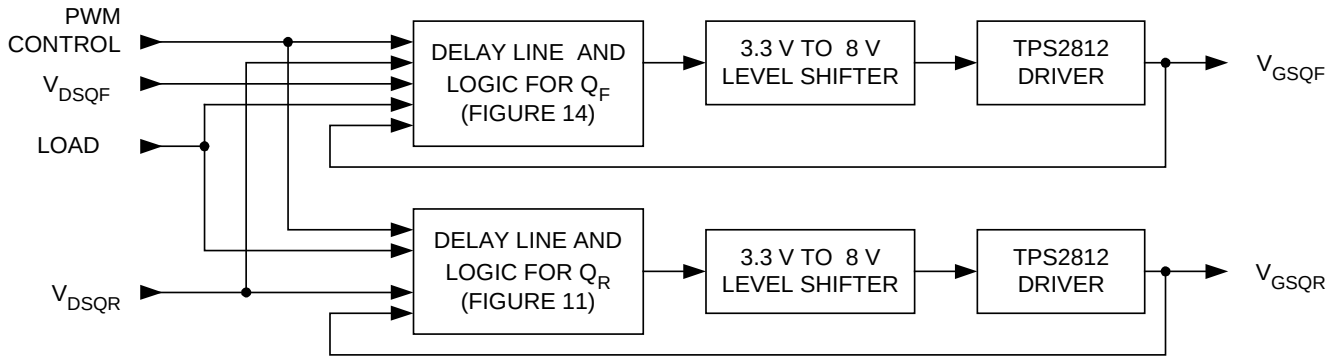

Fig. 18. Secondary side control block diagram.

To minimize the $R_{DS(on)}$ of the synchronous rectifiers, while reducing the gate charge required, an 8V power rail is used for the gate drivers. The outputs of the gate drivers were also level shifted down and input back into the logic devices. No gate drive resistors were used for either synchronous rectifier.

The three counters required for both the Q_R and Q_F control circuits are 4 bits wide, which results in a delay line with 16 elements. These delay lines are implemented with 16 bit bus drivers, part number 74AHC16244, with all sixteen drivers connected in series. The outputs from the 16 drivers are fed into the EPLDs that contain the multiplexers and all other logic. Since the delay lines are CMOS integrated circuits, the delay per element of the delay line can be adjusted by simply changing the supply voltage. For this circuit, setting the supply voltage to the delay line IC to approximately 2.7V set the delay per element to approximately 4ns. Using 4ns per delay line element is a tradeoff between dynamic range, meaning the maximum delay that can be commanded, the closed loop accuracy of the feedback loop, and the incremental power loss.

VII. Measurement Results

A. Waveforms

Fig. 19 shows the primary MOSFET drain-to-source voltage and the PWM CONTROL signal. The control signal is taken before the primary side gate driver. Note the inherent delay between the rising edge of the PWM CONTROL signal and the falling edge of the drain-to source voltage of Q_1. Likewise, the delay for the turn-off of Q_1 is significant and not the same as the turn-on delay.

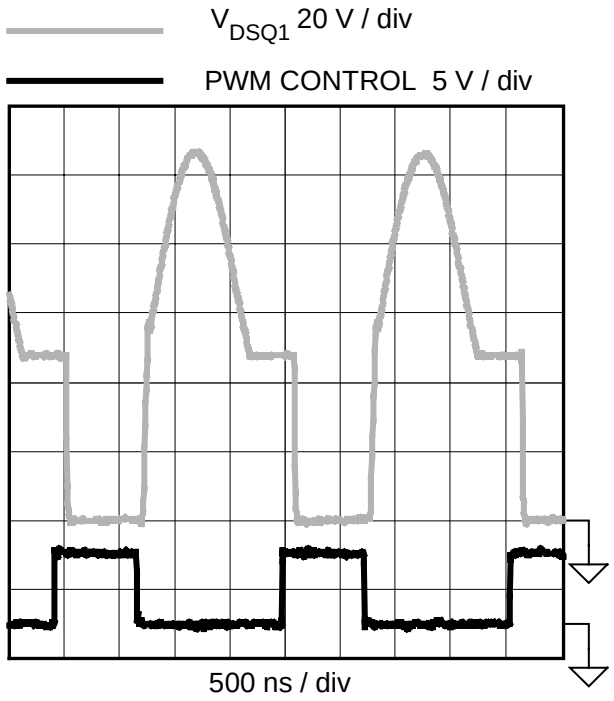

Fig. 19. Resonant reset waveforms.

Waveforms for self-driven synchronous rectification are shown in Fig. 20. These waveforms were taken at an input voltage of 48V and a load current of 3A. Note the delay from the PWM CONTROL signal to the drain-to-source voltages of Q_F and Q_R. During the dwell time interval, the body diode conduction of Q_F and Q_R is clearly visible. Since these waveforms were taken at 48V, the dwell time interval is a small

portion of the PWM period. At high line of 75V, the dwell time extends considerably, increasing the losses in both Q_R and Q_F.

The waveforms for control-driven synchronous rectification are shown in Fig. 21. From the top to the bottom are the drain-to-source of Q_R, drain-to-source of Q_F, gate-to-source of Q_F, and gate-to-source of Q_R. Both gates are controlled with the predictive delay circuitry described in this paper. A couple of interesting points can be observed. First, the gate-to-source voltage of Q_F has a resonant voltage present during the off time of Q_F. This is due to the resonant drain-to-source voltage on Q_F coupling through the gate-to-drain capacitance of Q_F.The resulting voltage seen on the gate is due to the resonant current through the driver's pull down resistance. The gate drive waveforms have the necessary overlap to minimize the loss when Q_F conducts the transformer magnetizing current during the dwell period.

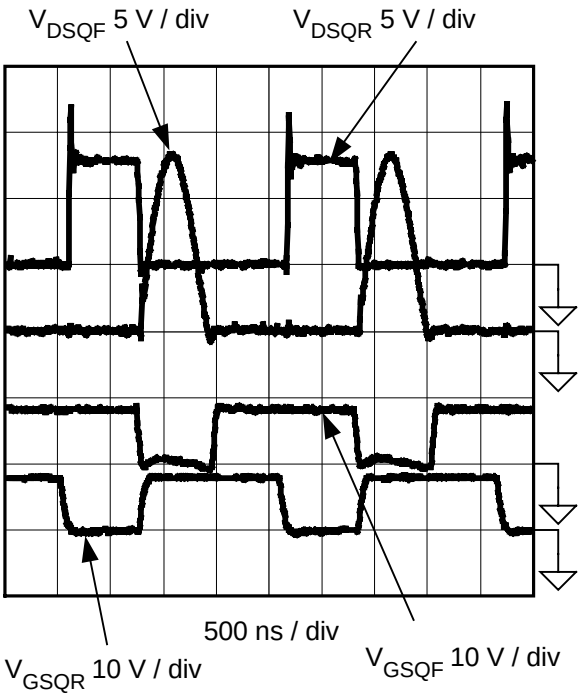

Fig. 21. Control-driven synchronous rectification waveforms.

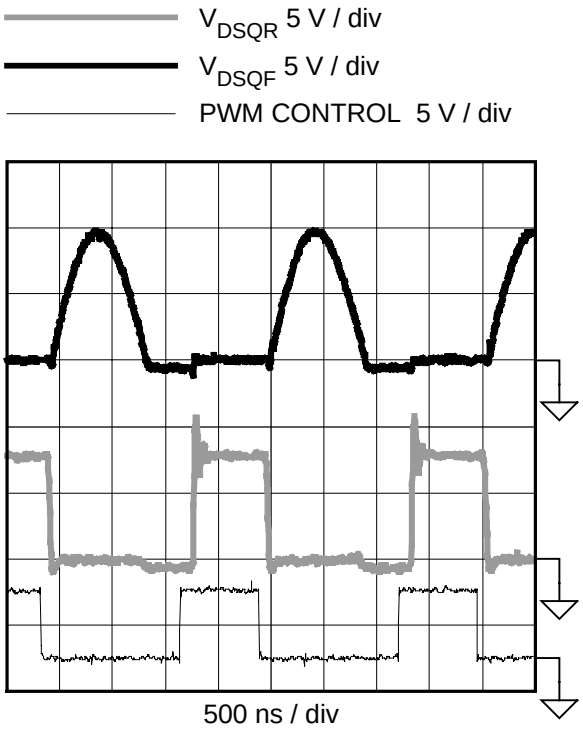

Fig. 20. Self-driven synchronous rectification waveforms.

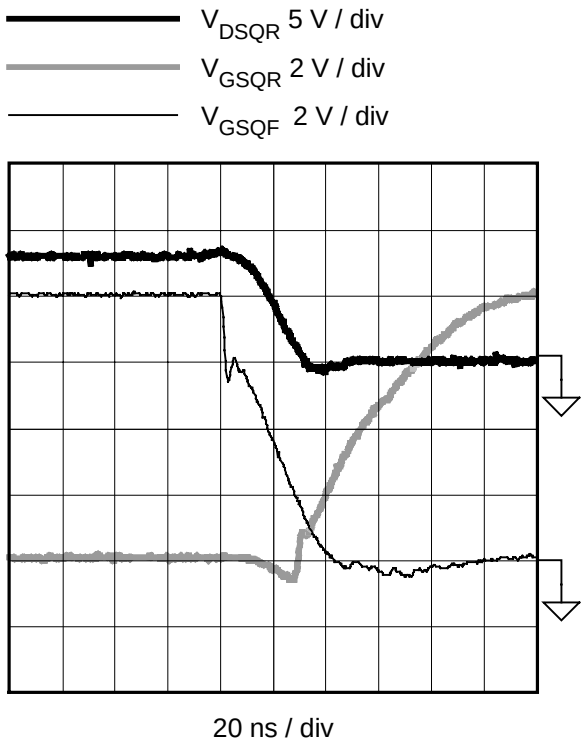

Fig. 22.Q_R turn-on waveforms.

Notice the magnified waveforms at each synchronous rectifier turn-on and turn-off transition, starting with Q_R. In Fig. 22, the drain-to-source voltage of Q_R as well as the gate-to-source voltage of both Q_R and Q_F is shown. As the drain-to-source voltage of Q_R falls, Q_F is being turned off, and Q_R is being turned on. The timing for the turn-on of Q_R and the turn-off of Q_F is being actively controlled by the feedback loops. Note that minimal body diode conduction exists on the drain-to-source voltage of Q_R.

The turn-off waveforms for Q_R are shown in Fig. 23. During the turn-off of Q_R, the high-speed comparator senses body diode conduction and the feedback loop adjusts the gate timing to eliminate this conduction. The drain-to-source voltage waveform shows virtually no body diode conduction whatsoever. This waveform shows an optimum turn-off of Q_R.

The turn-on waveforms for Q_F are shown in Fig. 24. The turn-on of Q_F is controlled without using the predictive delay circuit, so body diode conduction is expected due to propagation delays. A high-speed comparator detects Q_F's body diode conduction and turns on the gate. The resulting body diode conduction interval is seen to be approximately 50ns.

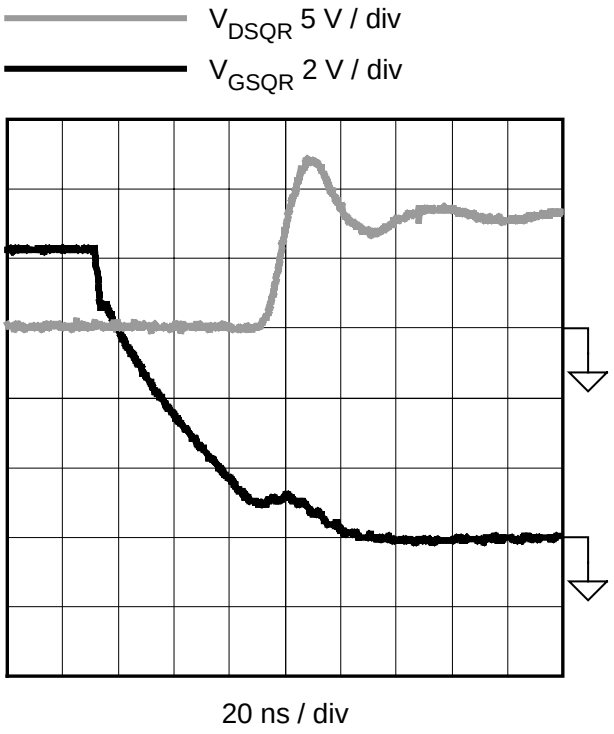

Fig. 23. Q_R turn-off waveforms.

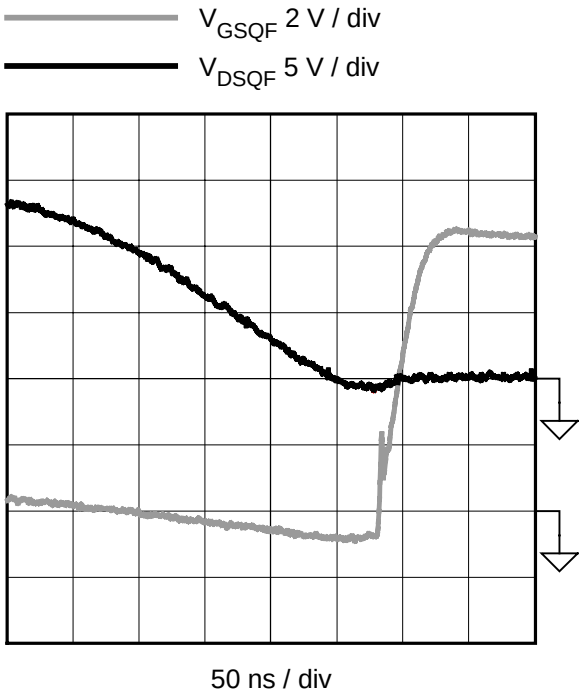

Fig. 24. Q_F turn-on waveforms.

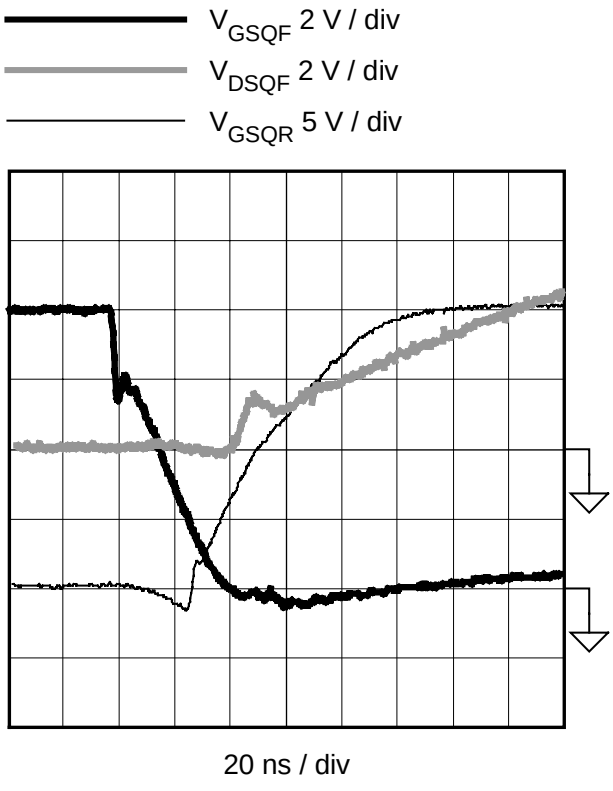

Fig. 25. Q_F turn-off waveforms.

The turn-off waveforms for Q_F are shown in Fig. 25. The predictive delay circuit shown in Fig. 14 controls the turn-off of Q_F to minimize the body diode conduction. Note that there is minimal body diode conduction seen on the drain-to-source voltage of Q_F.

B. Efficiency

A major goal of this topic is to compare the efficiency of the two control methods, self-driven and control-driven. It becomes clear that there is a third possibility, where control-driven techniques are used for Q_R, and the self-driven technique is used for Q_F. This "hybrid" control scheme has merits of simpler control which would use less circuitry, as well as the gate charge for Q_F would be recycled to the load instead of dissipated in the driver. The drawbacks to this hybrid control technique are the body diode conduction loss of Q_F during the dwell period, which in some applications may be offset by the recycled gate charge of Q_F. The efficiency of all three control techniques will be explored over line and load variation.

First, the setup for measuring efficiency is critical to drawing conclusions from the efficiency data. For the purposes of this paper, the principal concern is power stage efficiency, including the synchronous rectifier gate drive power. For this reason, the primary bias and gate drive current are ignored and not included in the efficiency calculations. Therefore, for the self-driven technique, the efficiency is measured by only including the power stage input current, while for both the hybrid and control-driven technique the 8V synchronous rectifier gate-drive bias current was included. Of course, the 8V bias current for the hybrid control is lower than the control-driven technique since only the freewheeling MOSFETs are driven. For these efficiency measurements, a lab power supply is used for the synchronous rectifier gate drive power supply. It is assumed that a suitable bias supply can be derived off the output choke or main power transformer in most applications.

Fig. 26 shows the measured efficiency over a 2A to 12A load range for the three control techniques, all at the nominal 48V input.

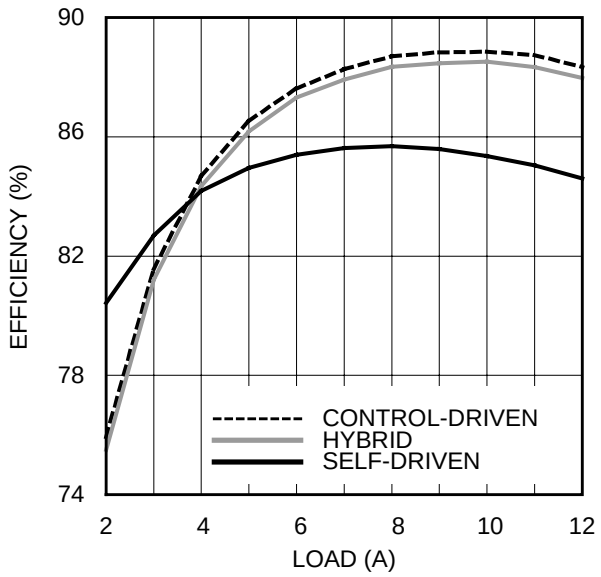

Fig. 26. Efficiency vs. load current.

As might be predicted, the highest to lowest efficiency tracks the most sophisticated to least sophisticated control technique respectively. The control-driven technique has the highest efficiency, which peaks at 88.8% at 10A load current and at full load is measured at a respectable 88.3%. The hybrid control technique also has excellent efficiency, measured at 88.5% at 10A load decreasing to 88.0% at 12A load. The efficiency difference is due to the body diode conduction of Q_F during the dwell period. The change in dissipated power between the control-driven and hybrid techniques is 400mW at full load. It needs to be recognized that the majority of this power is dissipated in the Q_F MOSFET, which only serves to increase the temperature rise and adversely affects reliability.

Interestingly, the self-driven efficiency at light load is measured to be higher than either the control-driven or hybrid techniques. This can be explained by two effects, the recycling of gate charge to the output and to the resonant tank circuit. The synchronous rectifier gate charge power is roughly independent of line and load, which adversely affects efficiency at light loads. Since the self-driven technique recycles this charge, the light load efficiency is higher than the control-driven and hybrid techniques.

Secondly, the forward body diode drop in the synchronous rectifiers is lower at light load currents, resulting in lower conduction losses. Clearly, the recycled gate charge is offsetting the additional body diode loss at these light loads.

Efficiency over a 2:1 line voltage change with a fixed output current of 10A is shown in Fig. 27.

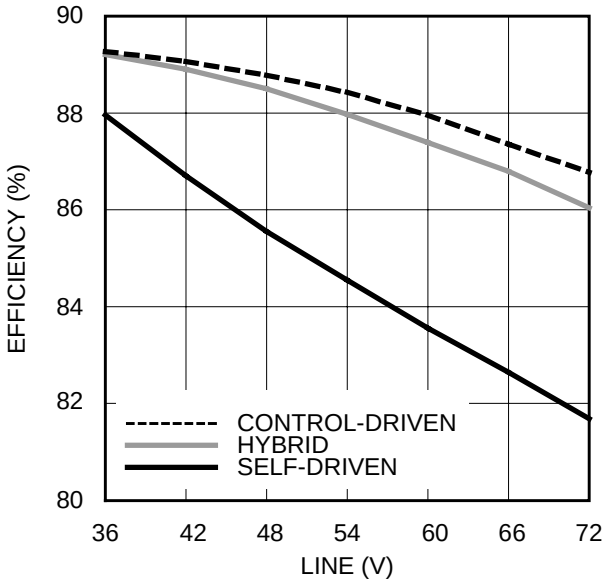

Fig. 27. Efficiency vs. input line voltage.

It is important to realize that the dwell time interval is critical to the efficiency as the line voltage is changed. The losses in the self-driven technique will increase significantly as the line voltage is increased, as the body diode of Q_R will conduct for a longer time period every switching cycle. As the line voltage is increased with the hybrid control technique, the body diode of Q_R will not conduct, but the body diode of Q_F will conduct for a longer time period every switching period during the dwell period. For the control-driven technique, no change in losses due to body diode conduction over line voltage variation is expected. All of these predictions are supported with the data. We can see that the efficiency is highest at low line for all three techniques. Switching losses, which increase as the line voltage is increased, are the dominant reason the efficiency decreases as the line voltage is increased. The hybrid efficiency is almost identical to the control-driven efficiency at low line, but the efficiency drops approximately 0.8% at high line due to the conduction of the Q_F body diode. This efficiency change represents a loss of 500mW at 72V line and 10A load current. As stated previously, this additional power loss is concentrated in the Q_F MOSFET.

VIII. CONCLUSIONS

The control-driven synchronous rectification technique can deliver the highest efficiency of the three techniques considered in this paper. However, to obtain this efficiency, precise gate timing is required for the synchronous rectifiers. A unique predictive control technique that automatically adjusts the gate timing for the synchronous rectifiers was developed and presented. This new control circuitry maximizes the efficiency of the forward converter with control-driven synchronous rectification. Texas Instruments has filed for patent protection for the entire content of this topic, including the control techniques for both synchronous rectifiers. Two products are in development that use the techniques described in this topic. An 8 pin synchronous buck driver IC for high current DC/DC applications is under development with the part number UCC37222. The UCC37223, a secondary side synchronous rectifier driver IC is also in development.

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[4] Ionel Dan Jitaru, *"High-Efficiency Rectification Techniques for Low Output Voltage and High Output Voltage Applications"*, APEC Professional Seminar, 1999.

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