Application Note

Understanding EN to VCC Start-Up Time and EN Internal Pull-Down Current in TPS56C230 Step-Down Converter

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ABSTRACT

Modern computing and processing circuits have multiple power rails and requires a precise power-up sequence. Incorrect power sequencing of these rails can cause serious problems and can lead to system level damages. This application note explains the EN, VCC signals, EN to VCC delay time and EN currents in the TPS56C230 point of load (POL) step-down converter. Detailed plots are also provided in the document to help engineers understand how to use the TPS56C230 in various systems.

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Trademarks

1 Introduction

This application note details the EN signal to VCC start-up timing and EN pin internal pull-down current in the TPS56C230 synchronous step-down converter. Figure 1-1 shows the typical application schematic of TPS56C230.

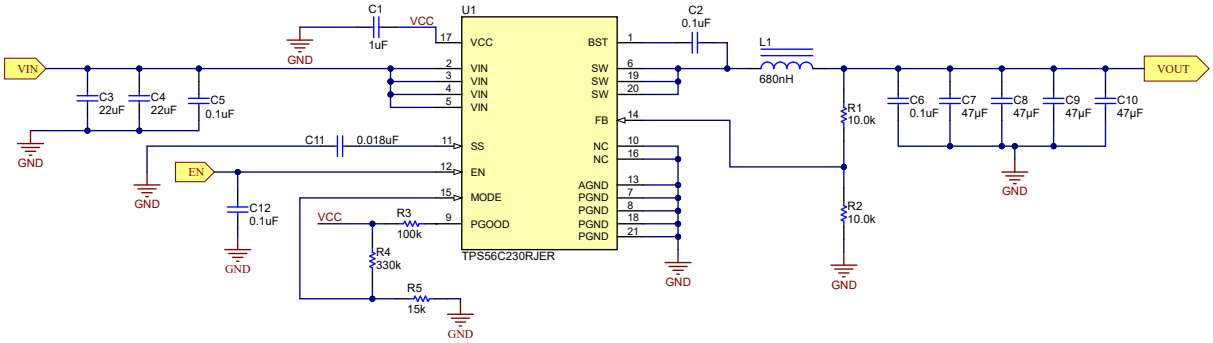

Figure 1-1. TPS56C230 Typical Application Schematic

2 EN to VCC Start-up Time

Figure 2-1 below shows the typical timing diagram of VCC rising of the device, once the enable signal crosses 0.932V typical threshold, VCC start rising after t_{VCCDLY} time. Typical value of t_{VCCDLY} = 13.5us and can vary from 6.35us to 25.6us.

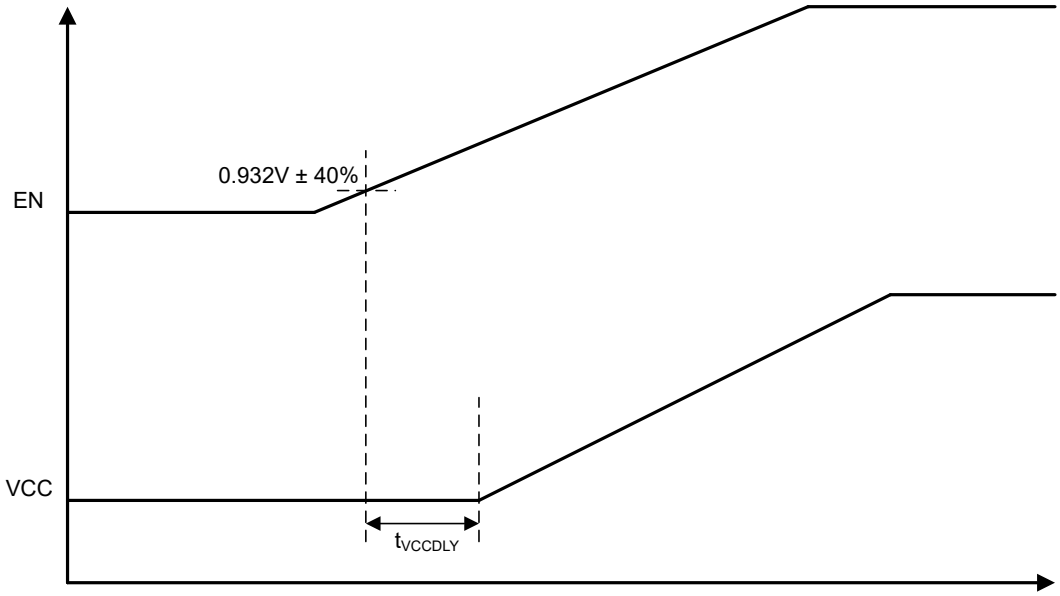

Figure 2-1. EN to VCC Start-up Delay

3 EN Internal Pull-down Current

Figure 3-1 below shows the typical EN internal pull down current of the device, once EN ≥ 0.8V there is a 2uA EN internal pull down current. If VCC ≥ 0.7V and EN-VCC ≥ 0.7V, there is an additional momentary 28uA internal pulldown current seen on EN as shown in Figure 3-1 and EN internal pulldown current recovers back to 2uA as EN-VCC < 0.7V. All the voltages and currents shown in Figure 3-1 are typical values.

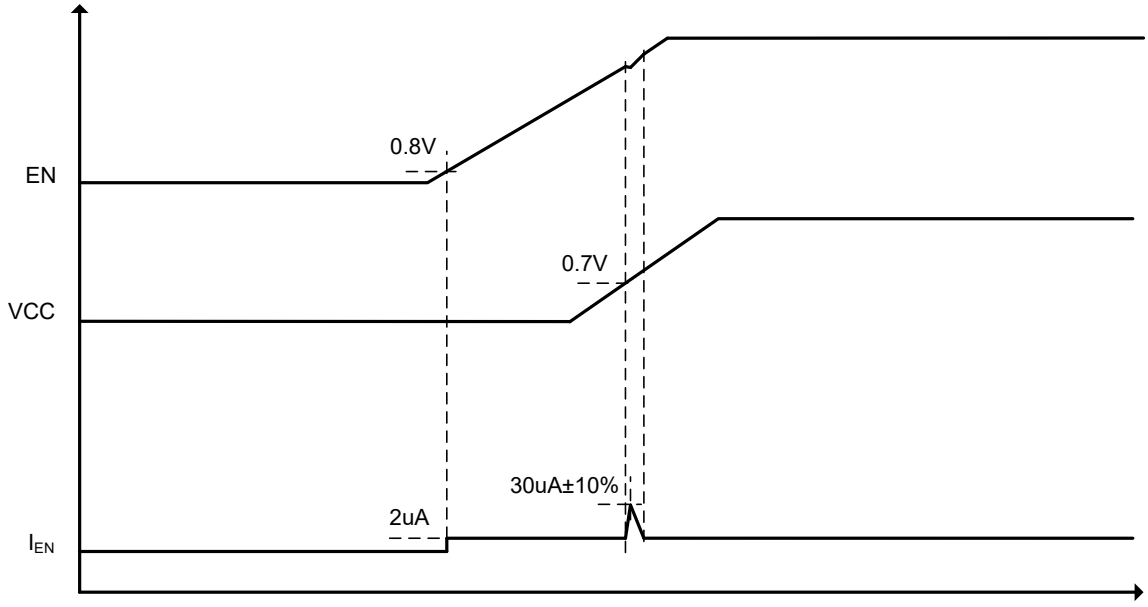

Figure 3-1. EN Internal Pull-down Current

4 Summary

This application note details the important sequencing signals, voltage thresholds, time delays, such as EN to VCC start-up time and EN internal pull-down, and voltage thresholds for sequencing using the TPS56C230. VCC starts rising after t_{VCCDLY} = 13.5us (typical) delay from EN crossing 0.932V (typical) threshold as detailed in EN to VCC Start-up Time. A 2uA internal pull-down current is seen on EN once EN ≥ 0.8V. If VCC ≥ 0.7V and EN-VCC ≥ 0.7V, then an additional momentary 28uA internal pull-down current is seen on EN. Internal pull-down current recovers to 2uA as EN-VCC < 0.7V, which is detailed in EN Internal Pull-down Current.

5 References

- Texas Instruments, TPS56C230 4.5V to 18V, 12A Synchronous Step Down Converter, data sheet
- Texas Instruments, TPS56C230 Buck Converter Evaluation Module User's Guide
- Texas Instruments, Power Supply Sequencing Solutions for Dual Supply Voltage DSPs, application note
- Texas Instruments, Sequencing With TPS54x80 and TPS54x73 SWIFT DC/DC Converters, application note
- Texas Instruments, A Smart Solution to Sequence and Monitor Multiple Power Rails in a System, technical article

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