Application Note

PassFET Hang Time with TCA39306 I2C, I3C Level Translator

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ABSTRACT

This application note explores the hang time associated with passFET's and the implications of hang-time on an I2C system.

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1 Introduction

The I2C bus often uses some type of passFET based design to allow level translation on the I2C bus. This can be in the form of an I2C controlled switch (such as TCA9548A) or I2C voltage translators (PCA9306 or TCA39306). I2C controlled switches can be used to control bus capacitance in a system or handle multiple targets with the same I2C address. I2C voltage translators can be used for voltage translation between two supply rails. These I2C devices typically use an internal switch defined as a passFET. The passFET provides a simple low-cost design for I2C bus switching and level shifting, but also introduces a short hanging effect which is defined as passFET hang time in this application note.

2 TCA39306 Level Translation Example

Figure 2-1 is a voltage translation application using the TCA39306 I3C level translator between an I^{2}C controller and an I^{2}C target device. TCA39306 is a passive device and is backwards compatible to I^{2}C.

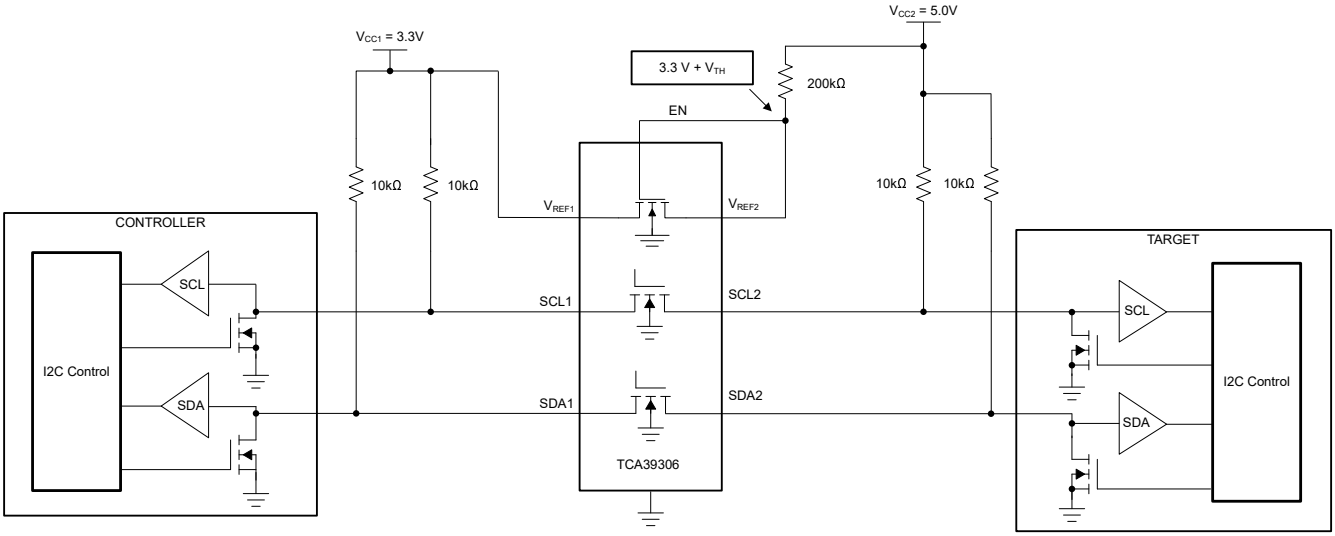

Figure 2-1. Voltage Translation Example Using TCA39306 Level Translator

The electrical settings for this example are as follows:

R_{PU} = 10kΩ

V_{CC1} = 3.3V

V_{CC2} = 5.0V

The TCA39306 is setup in level-translating mode. The TCA39306 EN and V_{REF2} pins have been shorted together (the EN and V_{REF2} pin connection is denoted as EN+REF2). This in effect creates a diode like structure that sets the $V_{EN+REF2}$ voltage to:

$$V_{EN+REF2} = 3.3V + V_{TH} \quad (1)$$

where V_{TH} is the threshold voltage of the passFET approximately 0.6V at room temperature. In the level translator the gate of each FET connecting SCL1 to SCL2 and SDA1 to SDA2 is biased to this $V_{EN+REF2}$ voltage. Therefore, each passFET gate voltage is adjusted to:

$$V_{GATE} = 3.3V + V_{TH} \quad (2)$$

The source voltage is the supply voltage due to the pull-up resistor connection, V_{SOURCE} = 3.3V.

$$V_{GS} = 3.3V + V_{TH} - 3.3V = V_{TH} \quad (3)$$

The passFET sits at the edge of the cutoff region due to $V_{GS} = V_{TH}$. When the controller pulls to a logic LOW of V_{OL} = 0.4V, the source voltage becomes equal to the V_{OL} of the open drain driver. $V_{SOURCE} = V_{OL}$ = 0.4V. Therefore the gate source voltage becomes:

$$V_{GS} = V_{GATE} - V_{SOURCE} = 3.9V - 0.4V = 3.5V > V_{TH} = 0.6V \quad (4)$$

The passFET acts like a switch in the linear operating region and turns on strongly since 3.5V is much greater than the threshold voltage. Current flows from both supply rails V_{CC1} and V_{CC2} through the pull-up resistors through the open-drain driver of the controller to GND shown in Figure 2-2.

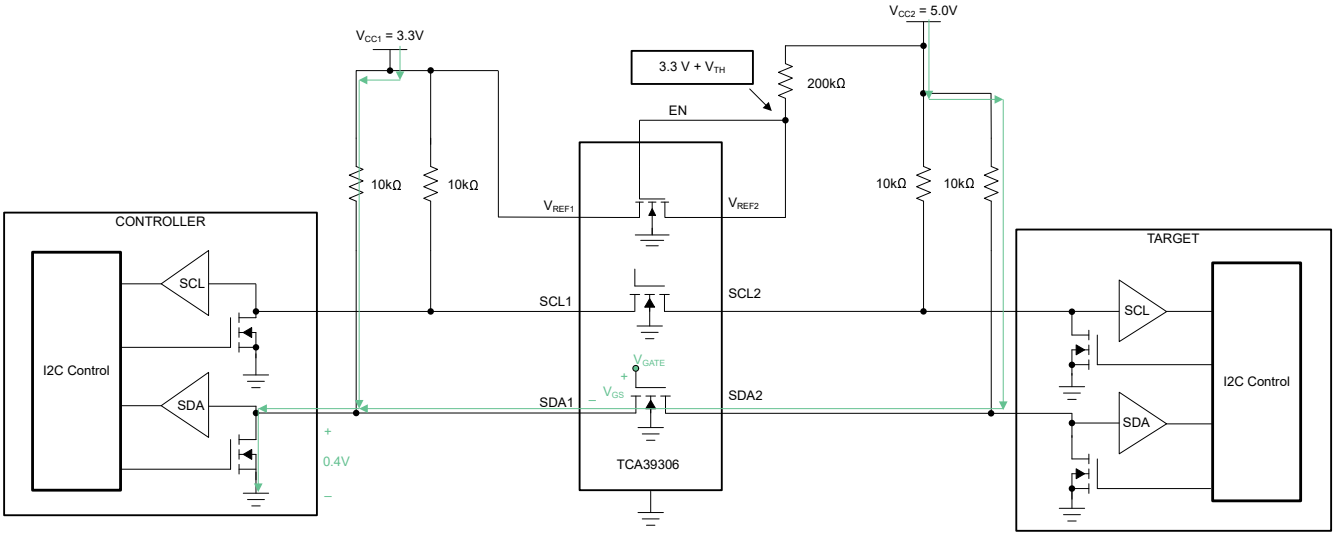

Figure 2-2. The Controller Pulls SDA LOW

When the controller releases the bus, SDA rises back to V_{CC1} through the pull-up resistor. V_{GS} decreases and the passFET enters the cutoff region resembling a high impedance state. Because the passFET drain and source terminal are interchangeable, the target can pull the SDA bus LOW. In Figure 2-3 the target pulls SDA LOW (V_{OL} = 0.4V). Once V_{GS} surpasses a V_{TH} = 0.6V, the internal passFET turns on and current flows from both supplies through the open-drain driver to GND similar to when the controller pulled LOW in the first example.

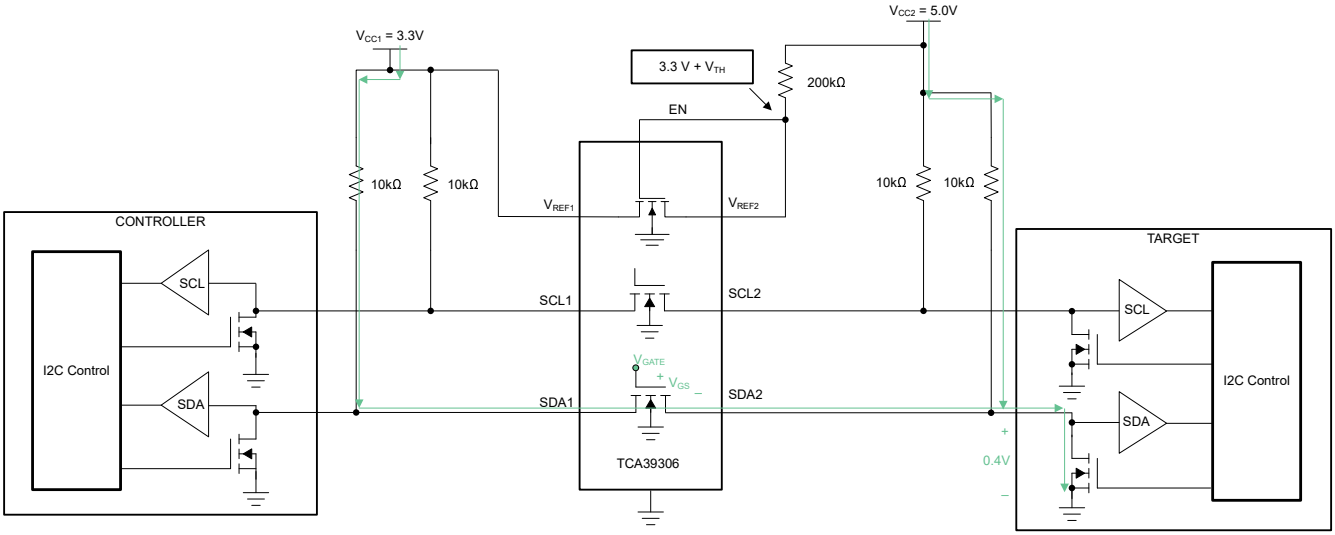

Figure 2-3. The Target Pulls SDA LOW

The simple design of the passFET is what allows seamless bi-directional level translation. The TCA39306 allows I2C level translation between two supply rails. In the LOW logic state, both the controller and target see a V_{OL}

= 0.4V. In the HIGH logic state the controller sees 3.3V and the target sees 5.0V due to the separation that the passFET produces inside the TCA39306.

2.1 What is the Hang Time Effect and Why Does the Hang Time Occur?

The hang time effect is defined in this application note as a length of time (typically nanoseconds) in which the I2C bus idles, *hangs*, before being fully pulled to a V_{OL} typically during a HIGH to LOW bus transition. This can happen on a rising edge if the slew rate is fast enough. This effect is partially due to the passFET changing drain to source resistance, but is more directly caused by the parasitic capacitance on the I2C bus. Figure 2-4 shows the same example circuit as before using the TCA39306, but this time including parasitic bus capacitance C_{BUS1} and C_{BUS2}.

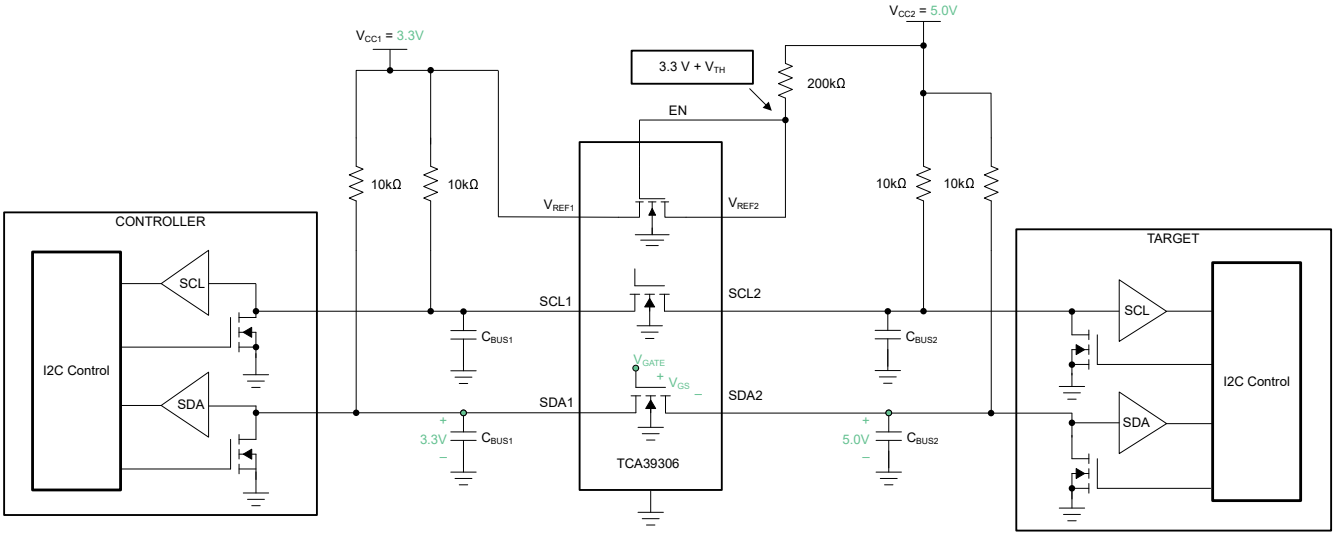

Figure 2-4. TCA39306 with Parasitic Bus Capacitance Included

If the target pulls SDA LOW, the voltage of C_{BUS2}, which is the voltage at the drain or source of the passFET, can be pulled towards a V_{OL} as shown in Figure 2-5.

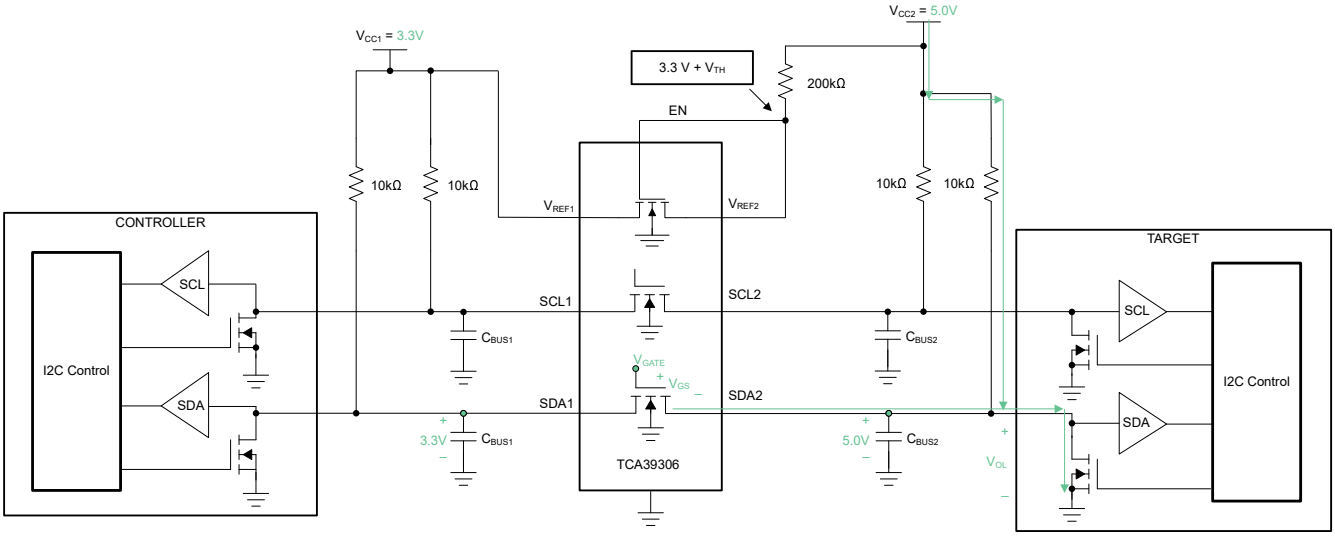

Figure 2-5. SDA2 is Pulled to a V_{OL} with C_{BUS2} Charged to 5.0V

The output low voltage V_{OL} defined in the I2C standard specifies the minimum LOW-level output current > 3mA at V_{OL} = 0.4V. In this example, V_{OL} is assumed to be near GND since the resistance of the open-drain driver is minimal.

As the target pulls LOW towards a V_{OL}, the source voltage can decrease which can result in an increase in V_{GS} quickly overcoming the threshold voltage of the passFET. This puts the passFET in a low impedance state connecting SDA1 to SDA2. The target can then see the charge on C_{BUS1} shown in Figure 2-6.

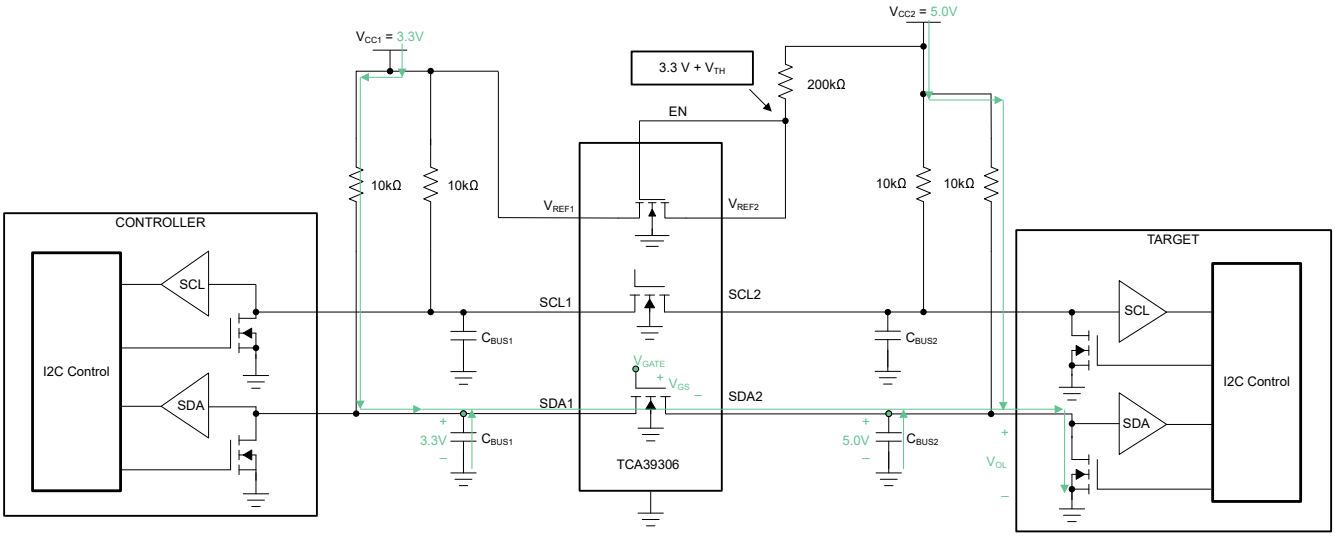

Figure 2-6. PassFET Turns On Allowing Target to see Charge on C_{BUS1}

This is exactly where the hang time effect occurs. SDA2 can resume being pulled to V_{OL} only when the charge on parasitic bus capacitors C_{BUS1} and C_{BUS2} have been balanced, effectively *hanging* the I2C bus. Once both bus parasitic capacitance C_{BUS1} and C_{BUS2} are charge balanced, SDA2 can continue pulling LOW to V_{OL}. SDA1 can follow SDA2, but SDA1 can be a R_{DS_ON} voltage drop higher than SDA2 due to passFET *ON* resistance.

The amount of time the I2C bus hangs is dependent on several factors.

- Amount of parasitic bus capacitance in the system
- Voltage supply levels
- Which side initially pulls LOW with respect to largest bus capacitance
- Drive strength

When testing the TCA39306 for hang time, the phenomenon is unnoticeable at larger time scales. Figure 2-7 is the oscilloscope capture with address 0x74 being sent on SDA. Data is labeled appropriately for SDA1 (controller side) and SDA2 (target side). I2C is sent at 100kHz with 10kΩ pull up resistors on each side of the translator.

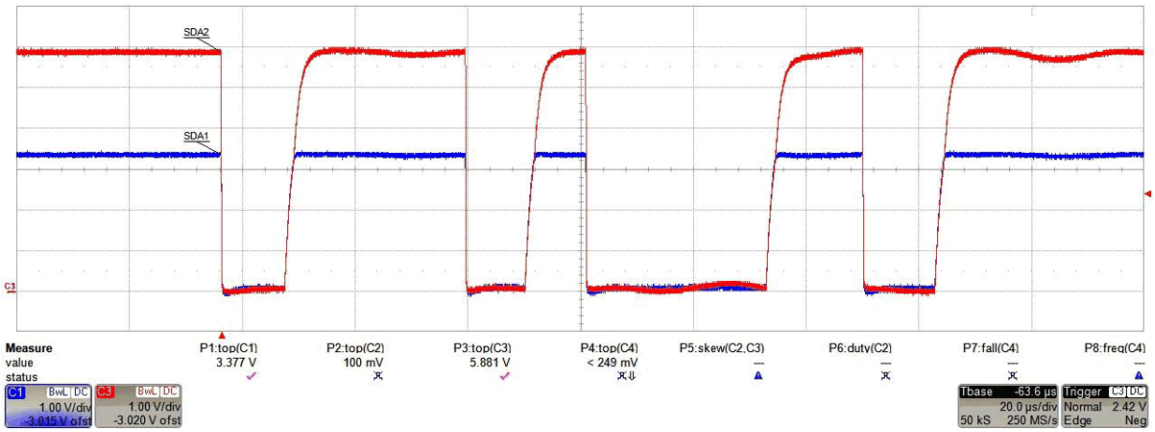

Figure 2-7. Address 0x74 Sent Across the TCA39306 when V_{CC1} = 3.3V, V_{CC2} = 5.0V, C_{BUS1} = 100pF, C_{BUS2} = 100pF, Pull LOW on Target Side (SDA2)

When the time scale is changed to 50.0ns per division, the effect becomes more apparent Figure 2-8.

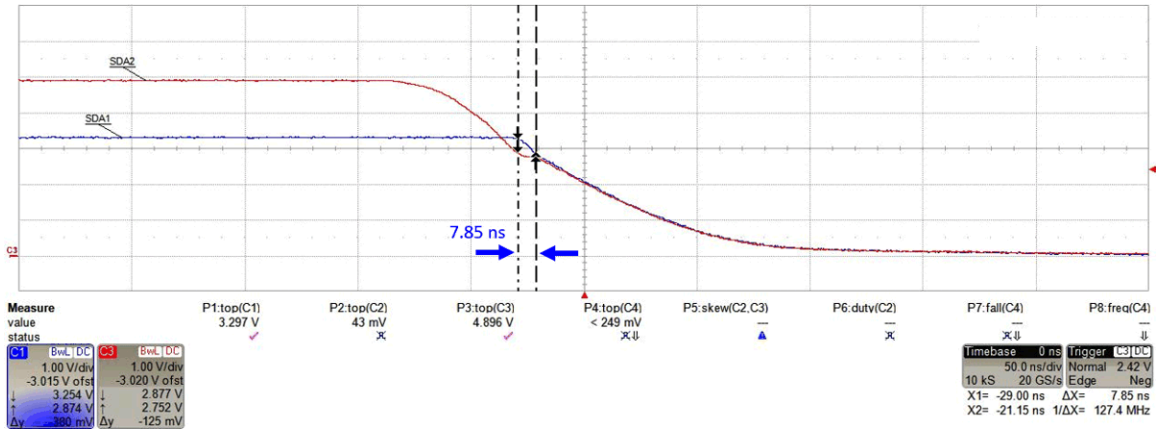

Figure 2-8. V_{CC1} = 3.3V, V_{CC2} = 5.0V, C_{BUS1} = C_{BUS2} = 100pF, Pull LOW on Target Side (SDA2)

Hang time has been measured to be 7.85ns in this test. The time that the bus hangs can be extended by adjusting the four parameters listed previously: parasitic bus capacitance, voltage supply levels, drive side, and drive strength. Drive strength can not be explored in this application note due to the inability to change this internally.

Changing the drive sides to the controller side (SDA1), hang time increases to approximately 36.25ns as in Figure 2-9.

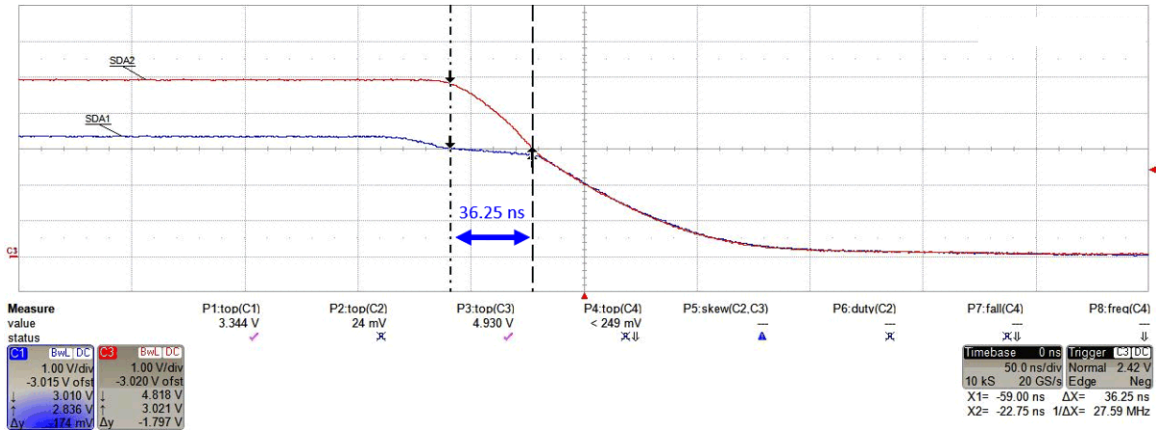

Figure 2-9. V_{CC1} = 3.3V, V_{CC2} = 5.0V, C_{BUS1} = C_{BUS2} = 100pF, Pull LOW on Controller Side (SDA1)

Recalling the setup in Figure 2-6 the target's bus capacitance C_{BUS2} is charged to 5.0V, while the controller's bus capacitance C_{BUS1} is charged to 3.3V. An increase in hang time results in 7.85ns to 36.25ns between pulling LOW on target side vs. the controller side. Pulling LOW on the controller side results in larger hang time because a capacitor with larger voltage exists on the opposite end of the passFET. Once the passFET turns *ON*, the controller suddenly sees this 5.0V capacitor in which charge begins to flow. The target side pull LOW is quicker because the 5.0V capacitor is discharged first, leaving a 3.3V capacitor on the controller side to be discharged second.

Hang time becomes larger when parasitic bus capacitance is increased. This makes sense because a larger capacitor acts like a larger battery holding more charge. Consider a case where C_{BUS1} = 100pF and C_{BUS2} = 400pF. Rearrange the following equation for capacitance for voltage.

$$C = \frac{Q}{V} \tag{5}$$

$$V = \frac{Q}{C} \tag{6}$$

If capacitance is constant, an increase in voltage must also mean that the charge *Q* on the capacitor increases. Therefore, a

400pF capacitance charged to a potential of 5V can have more charge stored than a capacitor of 100pF charged to 5V. Both capacitors exhibit the same voltage, but more capacity for charge is present on the 400pF parasitic capacitor. Thus, when controller side (SDA1) is pulled LOW there can exist a lengthen period of hang time due to the larger amount of charge stored on the 400pF parasitic capacitor on the target side (SDA2) of the passFET. This holds the bus for a longer time before SDA reaches a V_{OL}. Figure 2-10 captures this effect.

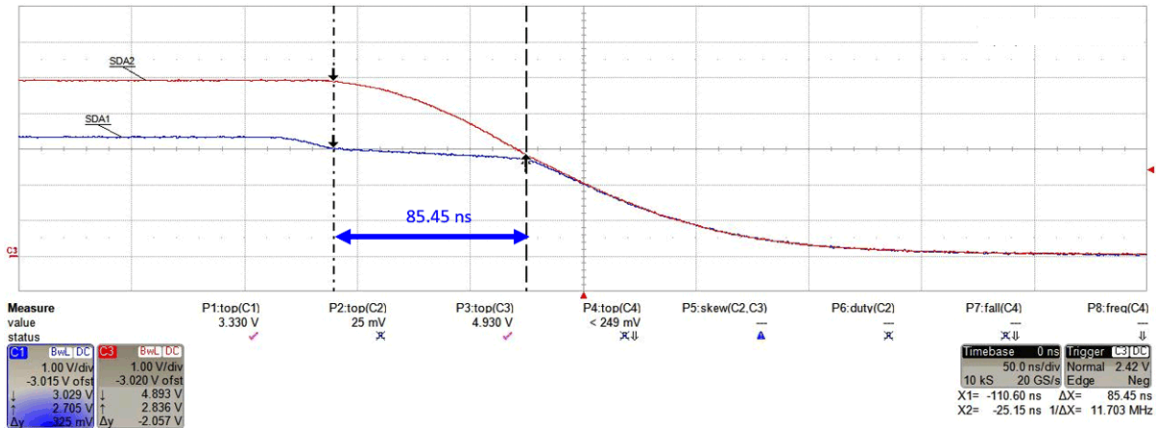

Figure 2-10. V_{CC1} = 3.3V, V_{CC2} = 5.0V, C_{BUS1} = 100pF, C_{BUS2} = 400pF, Pull LOW on Controller Side (SDA1)

Hang time increases to 85.45ns, more than double the amount in Figure 2-9. Hang time is made worse when the supply voltage of V_{CC2} is increased to 6.0V. An increased potential increases the total charge on C_{BUS2}. Figure 2-11 shows extended hang time due to larger supply voltage on V_{CC2}.

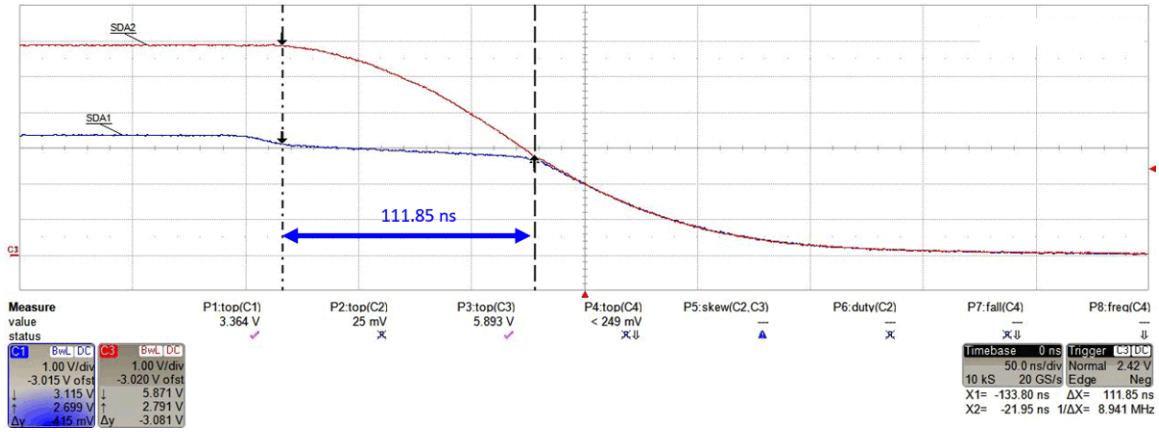

Figure 2-11. V_{CC1} = 3.3V, V_{CC2} = 6.0V, C_{BUS1} = 100pF, C_{BUS2} = 400pF, Pull LOW on Controller Side (SDA1)

2.2 Implications of Hang Time in an I2C System

Why does hang-time matter?

Hang time matters because it is inherent to every I2C system that utilizes passFET architecture. Note that hang time delay, although present, is much more harmless to an I2C system than detrimental. PassFET can be found in a variety of integrate circuits ranging from general purpose I2C multiplexers to common level translators. In general, there is little threat to the signal integrity of I2C systems due to hang-time. PassFET structures in I2C applications produce accurate data for I2C communication even up to faster speeds such as fast-mode+ (0 to 1MHz).

Even in the worst-case scenario of this application note, hang time was measured to be 111.85ns. The I2C address 0x74 is sent with the following waveform.

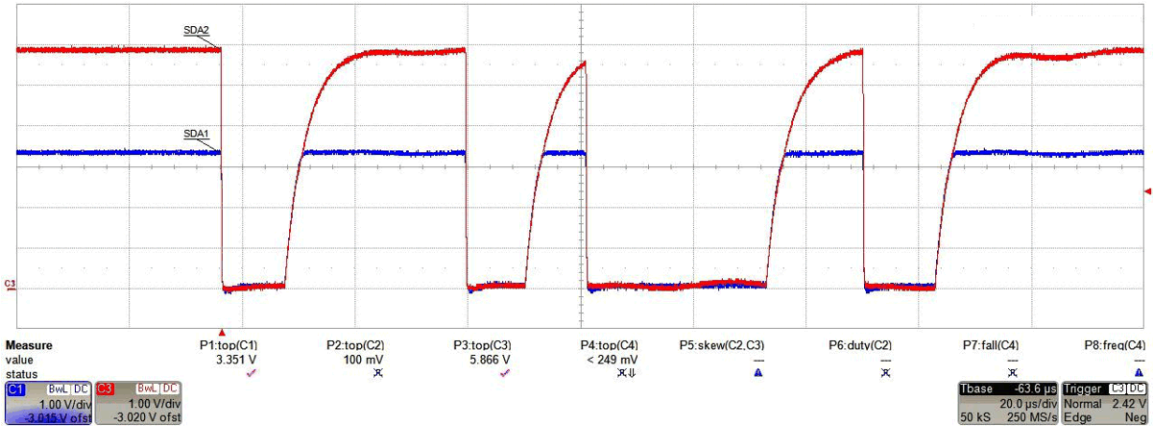

Figure 2-12. Hang Time is Unnoticeable

Hang time in this case presents no threat to the I2C application using the TCA39306. The address 0x74 is still sent properly without data corruption and level translates properly from 1.8V to 3.3V.

3 Summary

Hang time occurs due to the usage of the passFET which is present in any application that uses passive CMOS level translation. I2C level translators such as TCA39306, PCA9306, or I2C CMOS switches such as the TCA9548A all exhibit the behavior. Both types of devices can have this effect on the I2C bus but can most likely not cause data glitches due to the short timing interval.

4 References

- Texas Instruments, *TCA39306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator,* data sheet.
- Texas Instruments, *PCA9306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator,* data sheet.
- Texas Instruments, *TCA9548A Low-Voltage 8-Channel I2C Switch with Reset,* data sheet.

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