Application Note

MOSFET Selection Guide for BQ2575x Family

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ABSTRACT

This application notes aims to aid engineers in the selection of the switching MOSFETs for the BQ2575x family of devices and understand the origin of power losses from MOSFETs. The MOSFETs in use can play a large role in the overall efficiency of the system. MOSFET selection depend heavily on the system parameters, such as the switching frequency, output current, output voltage, and input voltage.

Table of Contents

Trademarks

1 Introduction

As the electrification of the grid, the automotive industry, and the internet of things (IoT) continues to proliferate, efficient power conversion becomes increasingly crucial for many systems today.

The BQ2575x family of devices is a series of charge controllers for Li-ion and LiFePO4 batteries. This family is comprised of the following devices as of the publication of this application note: the BQ25750, the BQ25756, the BQ25756E, the BQ25758, the BQ25758A, and the BQ25758S. These devices can be used to design an efficient buck or buck-boost topology for battery charging or DC-DC conversion. An example of a charger system that uses a BQ25756 charge controller is shown in Figure 1-1.

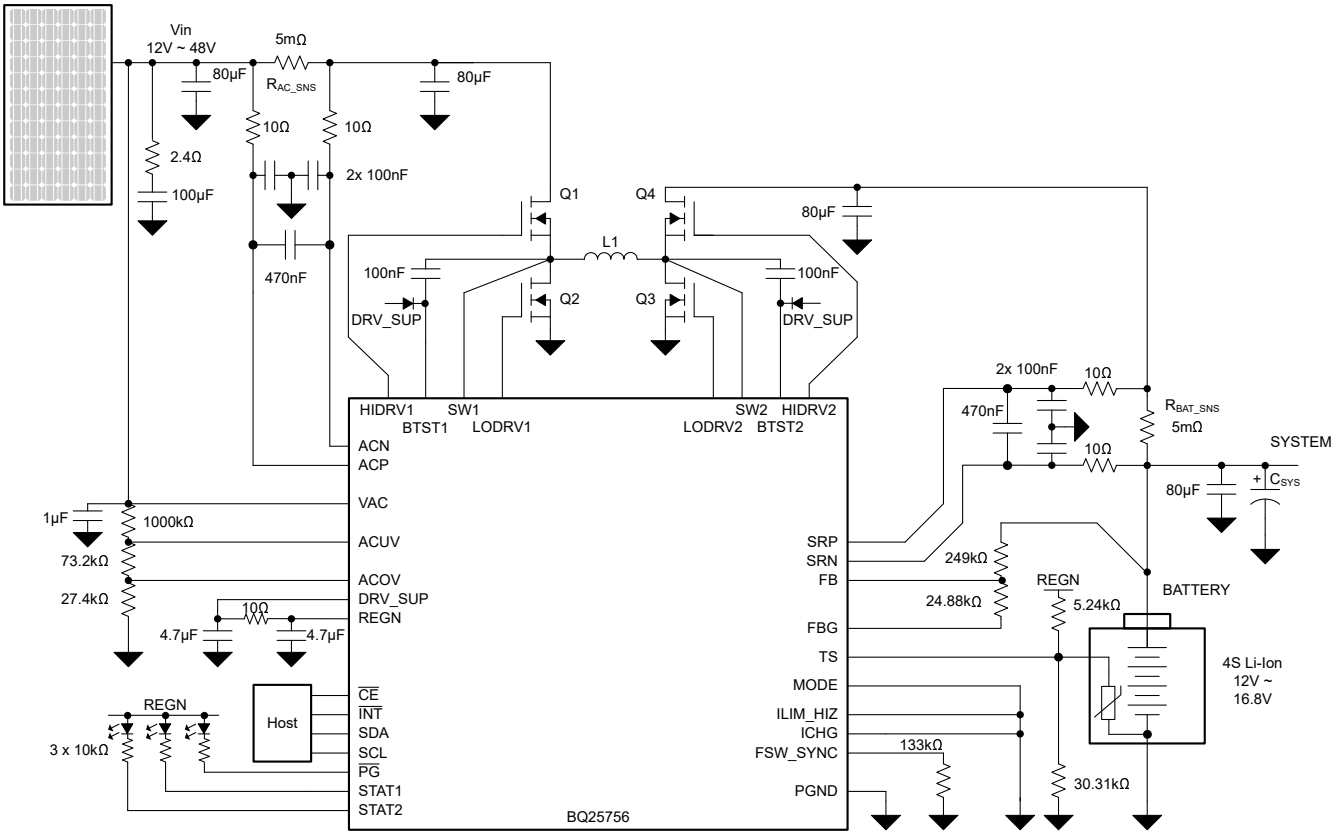


Figure 1-1. Example Application System Using a BQ25756 Device

This application note is a guide for the selection of the external MOSFETs used in combination with these devices. This is accomplished by

- Explaining where losses in these charger systems come from.
- Analyzing the key parameters typically included in MOSFET data sheets.
- Explaining the usage of the design calculator for the BQ2575x devices.
- Examining various BOMs that have been tested with the BQ2575x family of devices.

2 MOSFET Power Losses in Buck and Boost Chargers

In a switch-mode converter, the total losses come from the MOSFET losses and the parasitic resistances of the reactive and inductive components. For the energy storage elements, the losses come from the equivalent series resistance of each component. This application note focuses on the MOSFET losses and which parameters contribute to these losses. For ease of reference, Figure 2-1 is a MOSFET parasitic model.

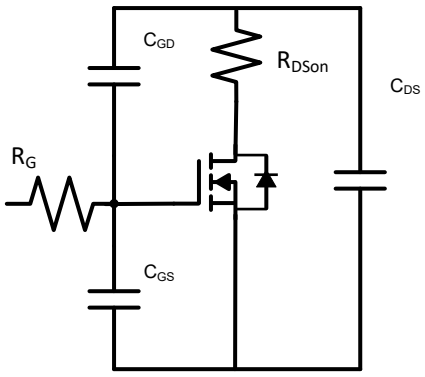


Figure 2-1. MOSFET Parasitic Model

2.1 Buck Mode Losses

For buck mode, the top FET is the synchronous FET and the bottom FET is the asynchronous FET. The power loss for the top FET can be split into the switching losses and conduction losses and is expressed in Equation 1.

$$P_{top} = P_{con\_top} + P_{sw\_top} \quad (1)$$

The conduction losses come from the MOSFET being statically-on.

$$P_{con\_top} = D \times {I_{L\_RMS}}^2 \times R_{DS(on)\_top} \quad (2)$$

$${I_{L\_RMS}}^2 = {I_{L\_DC}}^2 + \frac{{I_{ripple}}^2}{12} \quad (3)$$

The switching losses come from the current and voltage overlap during the FET turn-on and turn-off; the parasitic gate capacitance; and gate drive losses into the FET.

$$P_{sw\_top} = P_{IV\_top} + P_{Qoss\_top} + P_{gate\_top} \quad (4)$$

Where P_{IV_top} is the loss in the top MOSFET loss due to the current and voltage overlap, P_{Qoss_top} is the loss due to the MOSFET parasitic output capacitance, and P_{gate_top} is the gate drive loss. P_{IV_top} is given by the following equations:

$$P_{IV\_top} = 0.5V_{IN} \times I_{valley} \times t_{on} \times f_{sw} + 0.5V_{IN} \times I_{peak} \times t_{off} \times f_{sw} \quad (5)$$

$$I_{valley} = I_{L\_DC} - 0.5I_{ripple} \quad (6)$$

$$I_{peak} = I_{L\_DC} + 0.5I_{ripple} \quad (7)$$

Where I_{L_DC} is the DC inductor current and I_{ripple} is the peak-to-peak ripple current of the inductor. The MOSFET turn-on and turn-off times, t_{on} and t_{off} , are defined with the following equations:

$$t_{on} = \frac{Q_{sw\_top}}{I_{on}} \quad (8)$$

$$t_{off} = \frac{Q_{sw\_top}}{I_{off}} \quad (9)$$

Here, Q_{sw_top} is the switching charge of the top side FET which can be approximated by Equation 10.

$$Q_{sw\_top} = Q_{GD\_top} + Q_{GS\_top} \quad (10)$$

And I_{on} and I_{off} are defined with the following equations:

$$I_{on} = \frac{V_{DRV\_SUP} - V_{plt}}{R_{on}} \quad (11)$$

$$I_{off} = \frac{V_{plt}}{R_{off}} \quad (12)$$

Where V_{plt} is the Miller plateau voltage, V_{DRV_SUP} is the gate drive voltage on the MOSFETs, R_{on} is the total turn-on gate resistance, and R_{off} is the total turn-off gate resistance of the gate drive. The next term in the total loss calculation, P_{Qoss_top}, can be calculated with Equation 13.

$$P_{Qoss\_top} = 0.5 V_{IN} \times Q_{oss\_total} \times f_{sw} \quad (13)$$

Where Q_{oss_total} is the total parasitic output charge.

$$Q_{oss\_total} = Q_{gd\_top} + Q_{ds\_top} + Q_{gd\_bot} + Q_{ds\_bot} \quad (14)$$

The last term in the loss equation can be calculated with Equation 15.

$$P_{gate\_top} = V_{IN} \times Q_{gate\_top} \times f_{sw} \quad (15)$$

Where Q_{gate_top} is the gate charge of the top MOSFET and V_{IN} is the input voltage, not the gate drive voltage of the MOSFET. This is to include the losses generated by the internal LDO of the charge controller. If an external gate drive voltage is provided, the LDO losses can be avoided and Equation 16 can be used instead:

$$P_{gate\_top} = V_{DRV\_SUP} \times Q_{gate\_top} \times f_{sw} \quad (16)$$

The losses for the bottom MOSFET are comprised of conduction losses and switching losses:

$$P_{bottom} = P_{con\_bottom} + P_{sw\_bottom} \quad (17)$$

As for the conduction loss, the loss can be defined for buck mode similar to the top FET with Equation 18.

$$P_{con\_bottom} = \left(1 - D\right) \times {I_{L\_RMS}}^2 \times R_{DS\_ON\_bottom} \quad (18)$$

Where D is the duty cycle and I_{L_RMS} is the RMS current through the inductor. To minimize the conduction loss, the R_{DS_ON} need to be low. The next and final term in the loss calculation, the switching loss, can be calculated with Equation 19.

$$P_{sw\_bottom} = P_{RR\_bottom} + P_{dead\_bottom} + P_{gate\_bottom} \quad (19)$$

Where the P_{RR_bottom} term is the loss due to the reverse recovery charge of the MOSFET, P_{dead_bottom} is the loss due to the conduction loss of the body diode during dead time, and P_{gate_bottom} is the gate drive loss. Each term can be derived with the following equations:

$$P_{RR\_bottom} = V_{IN} \times Q_{rr} \times f_{sw} \quad (20)$$

$$P_{dead\_bottom} = V_{SD} \times I_{valley} \times f_{sw} \times t_{dead\_rise} + V_{SD} \times I_{peak} \times f_{sw} \times t_{dead\_fall} \quad (21)$$

$$P_{gate\_bottom} = V_{IN} \times Q_{gate\_bottom} \times f_{sw} \quad (22)$$

Q_{gate_bottom} is the gate charge of the bottom MOSFET, V_{SD} is the forward voltage of the body diode, and V_{IN} is the input voltage, not the gate drive voltage of the MOSFET. This is to include the losses generated by the internal LDO of the device. If an external gate drive voltage is provided, Equation 23 can be used instead:

$$P_{gate\_bottom} = V_{DRV\_SUP} \times Q_{gate\_bottom} \times f_{sw} \quad (23)$$

2.2 Boost Mode Losses

For boost mode, the top FET is asynchronous and the bottom FET is synchronous. The total power losses for the top and bottom FET can be determined in the same way as in buck mode with the following equations:

$$P_{top} = P_{con\_top} + P_{sw\_top} \quad (24)$$

$$P_{bottom} = P_{con\_bottom} + P_{sw\_bottom} \quad (25)$$

The conduction losses for the top FET are similar the buck mode losses:

$$P_{con\_top} = \left(1 - D\right) \times {I_{L\_RMS}}^2 \times R_{DS(on)\_top} \quad (26)$$

$${I_{L\_RMS}}^2 = {I_{L\_DC}}^2 + \frac{{I_{ripple}}^2}{12} \quad (27)$$

In boost mode, the top FET has losses from the reverse recovery charge, dead time, and gate capacitance.

$$P_{sw\_top} = P_{RR\_top} + P_{dead\_top} + P_{gate\_top} \quad (28)$$

The gate losses, dead time losses, and reverse recovery losses are:

$$P_{RR\_top} = V_{IN} \times Q_{rr} \times f_{sw} \quad (29)$$

$$P_{dead\_top} = V_{SD} \times I_{valley} \times f_{sw} \times t_{dead\_rise} + V_{SD} \times I_{peak} \times f_{sw} \times t_{dead\_fall} \quad (30)$$

$$P_{gate\_top} = V_{IN} \times Q_{gate\_top} \times f_{sw} \quad (31)$$

As before, if an external gate drive voltage is provided, the following equation can be used instead:

$$P_{gate\_top} = V_{DRV\_SUP} \times Q_{gate\_top} \times f_{sw} \quad (32)$$

The losses for the bottom FET can be calculated is much the same way as the synchronous buck FET.

$$P_{con\_bottom} = D \times {I_{L\_RMS}}^2 \times R_{DS(on)\_bottom} \quad (33)$$

$${I_{L\_RMS}}^2 = {I_{L\_DC}}^2 + {{I_{ripple}}^2}/{12} \quad (34)$$

The switching losses come from the current and voltage overlap during the FET turn-on and turn-off; the parasitic gate capacitance; and gate drive losses into the FET.

$$P_{sw\_bottom} = P_{IV\_bottom} + P_{Qoss\_bottom} + P_{gate\_bottom} \quad (35)$$

Where P_{IV_top} is the loss in the top MOSFET loss due to the current and voltage overlap, P_{Qoss_top} is the loss due to the MOSFET parasitic output capacitance, and P_{gate_top} is the gate drive loss. P_{IV_top} is given by the following equations:

$$P_{IV\_bottom} = 0.5 V_{IN} \times I_{valley} \times t_{on} \times f_{sw} + 0.5 V_{IN} \times I_{peak} \times t_{off} \times f_{sw} \quad (36)$$

The calculations for I_{Valley}, I_{Peak}, t_{on}, and t_{off} are the same as in buck mode.

2.3 Closing Thoughts for FET Losses

As can be inferred by the equations, switching losses are dominant when the charge current is low. As the current increases, the conduction losses increase as well and the conduction losses become the dominant loss term in the equation. Selecting an efficient FET can depend on the switching frequency of the charger and the average charge current.

Also, the recommendation is to limit the switch node capacitance such that the following is true:

$$C_{sw}(nF) < \frac{160}{V_{in}} \tag{37}$$

If V_{in} is 60V, the recommendation is to keep the total switch node capacitance (C_{sw}) under 2.67nF. This can mitigate the switching loss and is a requirement for proper device functionality.

For ease of reference, BQ2575X's gate driver resistance of R_{on} and R_{off} and the dead time (t_{dead_time}) are listed in Table 2-1. The dead time can be adjust to be 45ns, 75ns, 105ns, or 135ns.

Table 2-1. BQ2575X IC's Gate Driver Characteristics

Parameter	Typical Value
R_{on}	3.4Ω
R_{off}	1.0Ω
t_{dead_time} (Both sides)	45ns

3 Evaluating MOSFETs Using the Design Calculator

The BQ25756 Design Calculator can be used for all of the BQ2575X family of devices. This calculator can help with resistor programming, IC set-up, and the BOM selection process. The calculator can also take user inputs about the operating conditions, BOM, and system requirements to estimate the power loss and efficiency. Note that the calculator does not take into account power losses from other sources, like magnetic core losses, or copper trace losses. The efficiency calculator is best used to compare one FET to another FET.

This calculator also includes a thermistor qualification tab to estimate the minimum/typical/maximum temperature falling and rising thresholds for the various temperature charging windows. This tab can be used to select a thermistor for the application of interest, but this section focuses on the power loss/efficiency tab of the calculator.

To use this calculator, ignore the warning about circular references and fill in the yellow cells. The cells with red tabs contain additional information about the adjacent cell. Red cells highlight the cells that can have an issue. After filling out all of the yellow cells in the design calculator, the efficiency/power loss analyzer section can be used to plot the efficiency, sense resistor loss, and power losses of the two MOSFETs.

Figure 3-1 shows the input voltage max is outside of the operating range. As a result, the text is red. When the cursor hovers over the red tab, the description text appears.

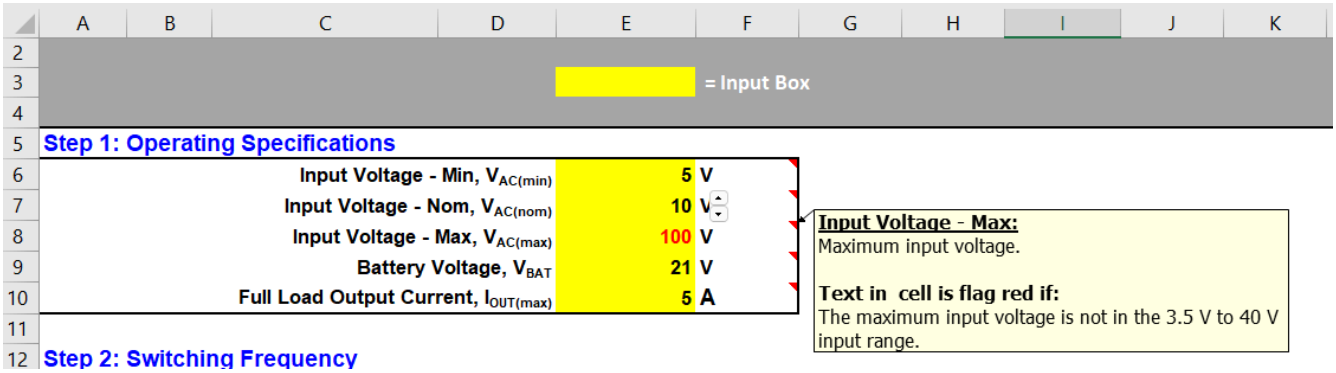
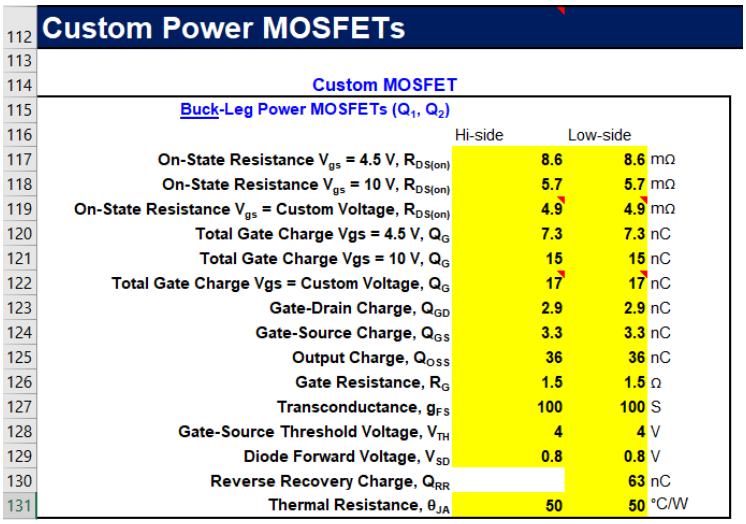


Figure 3-1. BQ2575x Design Calculator Example

3.1 Correlating MOSFET Data Sheet Parameters With the Design Calculator Parameters

This section aims to correlate device parameters typically given on a MOSFET data sheet to the parameters included in the design calculator. If a parameter is not on the data sheet, reach out to the device manufacturer.

These parameters here are the inputs required to use the design calculator. The parameters are the same for the buck-phase and the boost-phase switching MOSFETs.



Custom Power MOSFETs

	Custom MOSFET			
	Buck-Leg Power MOSFETs (Q_1, Q_2)	Hi-side	Low-side	
	On-State Resistance V_{gs} = 4.5 V, $R_{DS(on)}$	8.6	8.6	mΩ
	On-State Resistance V_{gs} = 10 V, $R_{DS(on)}$	5.7	5.7	mΩ
	On-State Resistance V_{gs} = Custom Voltage, $R_{DS(on)}$	4.9	4.9	mΩ
	Total Gate Charge Vgs = 4.5 V, Q_G	7.3	7.3	nC
	Total Gate Charge Vgs = 10 V, Q_G	15	15	nC
	Total Gate Charge Vgs = Custom Voltage, Q_G	17	17	nC
	Gate-Drain Charge, Q_{GD}	2.9	2.9	nC
	Gate-Source Charge, Q_{GS}	3.3	3.3	nC
	Output Charge, Q_{OSS}	36	36	nC
	Gate Resistance, R_G	1.5	1.5	Ω
	Transconductance, g_{FS}	100	100	S
	Gate-Source Threshold Voltage, V_{TH}	4	4	V
	Diode Forward Voltage, V_{SD}	0.8	0.8	V
	Reverse Recovery Charge, Q_{RR}		63	nC
	Thermal Resistance, θ_{JA}	50	50	°C/W

Figure 3-2. MOSFET Parameter Inputs for the BQ2575x Design Calculator

The first parameter in the design calculator is the on-state resistance ($R_{DS(on)}$). This is the resistance across the drain and source terminals when the MOSFET is turned-on. The calculator asks for $R_{DS(on)}$ at 4.5V and 10V. $R_{DS(on)}$ is typically given in the data sheet either in the electrical characteristics section or in a graph that plots the V_{gs} versus $R_{DS(on)}$.

The total gate charge (Q_G) refers to the charge (in Coulombs) necessary to charge the gate capacitance to turn on the MOSFET so that the actual gate voltage of the MOSFET matches the driving voltage. This is different from the switching charge. Q_G is typically given in the MOSFET data sheet. The gate-drain charge (Q_{GD}) and gate-source charge (Q_{GS}) are also usually provided. The output charge, Q_{oss}, is defined in Equation 38.

$$Q_{oss} = \int_0^{V_{DS}} C_{oss}\left(v\right) dv \tag{38}$$

The internal gate resistance R_G can be modeled by a resistor in series with the MOSFET gate, as depicted in Figure 2-1.

The transconductance (g_{fs}) refers to the small signal gain of the MOSFET. The threshold voltage (V_{TH}) is the voltage at which the MOSFET enters the active region and conducts current across the drain and the source terminals. Both of these parameters are typically included in the MOSFET data sheet.

The diode forward voltage (V_{SD}) is the voltage drop across the drain and source terminals when the body diode of the MOSFET is forward biased.

The reverse recovery charge (Q_{RR}) is the charge that is stored in the body diode that must be depleted before the body diode can block the flow of current in the reverse biased direction.

The thermal resistance is a measure of the thermal performance of the MOSFET. The higher the thermal resistance, the higher the temperature change of the MOSFET for a given power dissipation.

3.2 Design Calculator MOSFET Comparison Example

As an example, the design calculator is used here to compare the TI recommended MOSFET, the SiR680LDP, and the SiR880BDP as the custom MOSFET. For this example, the following operating conditions are used for both.

All other input parameters are left as the default.

Table 3-1. Operating Conditions for Design Calculator Example

Parameter	Value
V_{IN} (minimum)	5V
V_{IN} (nominal)	10V
V_{IN} (maximum)	50V
V_{BAT}	21V
V_{ext_drv}	10V
I_{out}	8A
f_{sw}	200kHz
R_{fsw}	200kΩ
I_{SAT}	19A
Selected Inductance, L	10µH
Selected Inductor DCR	12mΩ

These operating conditions then result in the following efficiency and power loss graphs.

After the yellow cells are filled in, the calculator can plot these graphs. Plot 1 is the recommendation, SiR680LDP, and plot 2 is SiR880BDP.

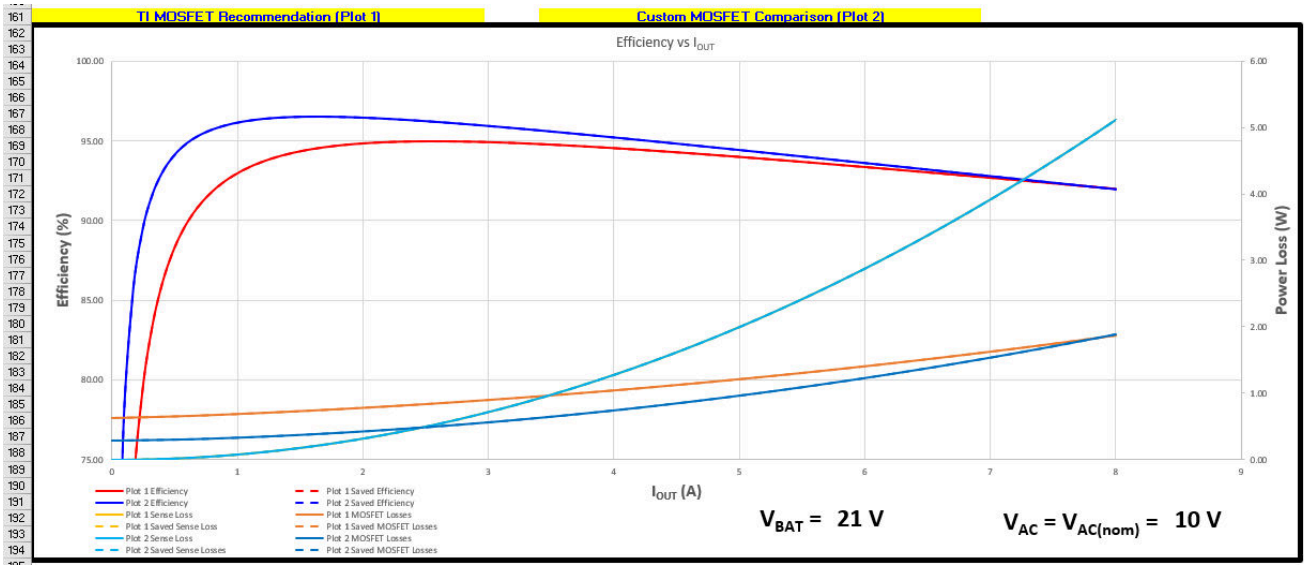


Figure 3-3. Design Calculator Efficiency and Loss Graphs for MOSFET Comparison

In this example, the SiR880BDP MOSFET (depicted in Plot 2) has a higher efficiency for a lighter load because of the lower gate capacitance and output capacitance. The lower capacitance reduces the switching losses. At higher loads, the conduction losses become greater than the switching losses and the SiR680LDP is more efficient because of the lower $R_{DS(ON)}$.

4 BOM Evaluation

Several BOMs have been evaluated for efficiencies and losses. Each found that efficient systems can be designed using the BQ2575x family of devices. A summary of the highest efficiencies for each BOM is included in Table 4-1.

The operating condition shows the output current, the bus voltage, switching frequency, input voltage, and external gate drive voltage.

Table 4-1. BOM Summary

BOM Number	MOSFET Key Properties ($R_{DS(ON)}$, voltage rating)	Switching Frequency	Inductor Properties
1	SiR880BDP MOSFET (BVdss=80V, $R_{DS(ON)}$=5.3mΩ for Vgs=10, Id=10)	450kHz	CMLB135T-100MS Inductor (L=10uH, DCR=22mΩ)
2	AON6380 MOSFET (BVdss=30V, $R_{DS(ON)}$ (Vgs=10V, Id=20A)=5.6mohm)	600kHz	HCM1103-2R2-R Inductor (L=2.2uH, DCR=8.4mΩ)
3	SiR680LDP MOSFET (BVdss=80V, $R_{DS(ON)}$=2.33mohm)	250kHz	SRP1050Wa-100M inductor (L=10uH, DCR=23mΩ)
4	SiR188LDP MOSFET (BVdss=60V, $R_{DS(ON)}$=3.1mohm)	350kHz	CMLB135T-6RBMS inductor (L=6.8uH, DCR=15mΩ)
5	SiR880BDP MOSFET (BVdss=80V, $R_{DS(ON)}$=5.3mohm for Vgs=10, Id=10)	450kHz	IHLP6767GZER150M01 inductor (L=15uH, 18.8mΩ)

The following graphs show the efficiency and losses for each of these BOMs.

In Figure 4-1 and Figure 4-2, the efficiency is highest when V_{IN} is approximately equal to V_{OUT}. Big differences from V_{IN} to V_{OUT} reduce the duty cycle and make the charger work harder. Buck-Boost mode is the most efficient mode because the buck-phase and the boost-phase operate in a low duty cycle and the switching losses are minimized.

In Figure 4-2, BOM1 is the same as the BQ25758BOM and BOM1 can cover the full range of USB-EPR voltages.

In Figure 4-3, BOM2 is designed to work with the 100W USB-PD and fit the components into a small area.

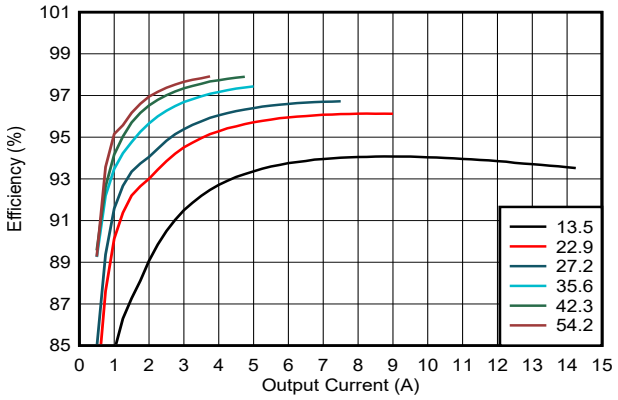


Figure 4-1. BOM1 Efficiency and Loss With V_{IN}=48V

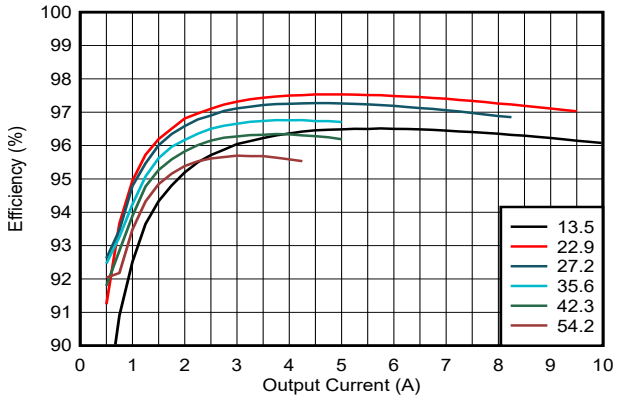


Figure 4-2. BOM1 Efficiency and Loss With V_{IN}=20V

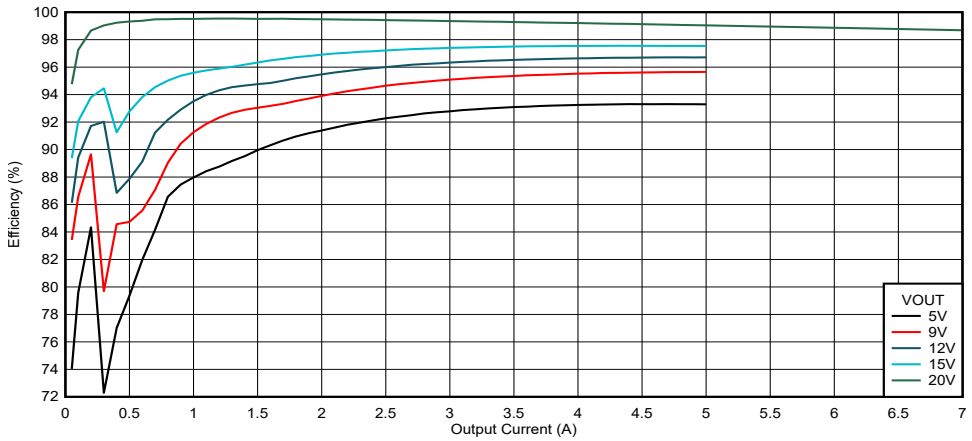


Figure 4-3. BOM2 With V_{IN}=20V

In Figure 4-4, BOM3 is designed for automotive applications to work with 12V $LiFePO_4$ batteries.

In Figure 4-5, BOM4 was designed to work with 140W USB-PD charging. In the graph, BOM4 is using a external gate drive supply of 7V.

In Figure 4-6, BOM5 is designed for automotive applications with a 48V $LiFePO_4$ battery.

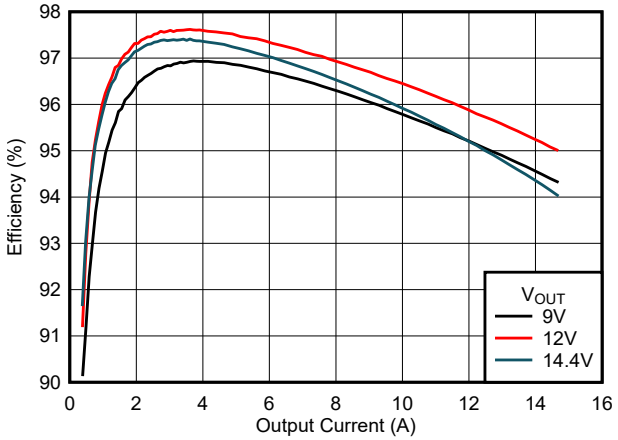


Figure 4-4. BOM3 Efficiency Graph With V_{IN}=12V

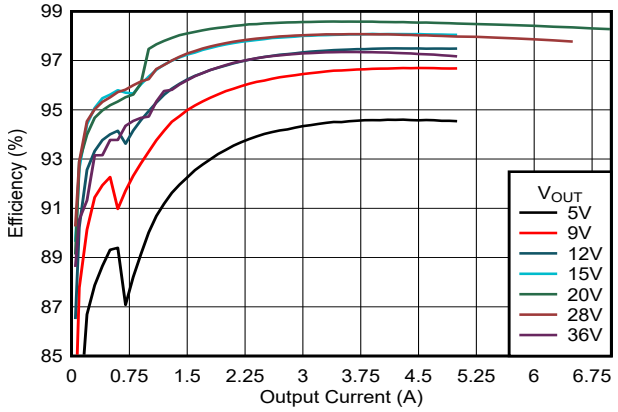


Figure 4-5. BOM4 Efficiency Graph With V_{IN}=20V

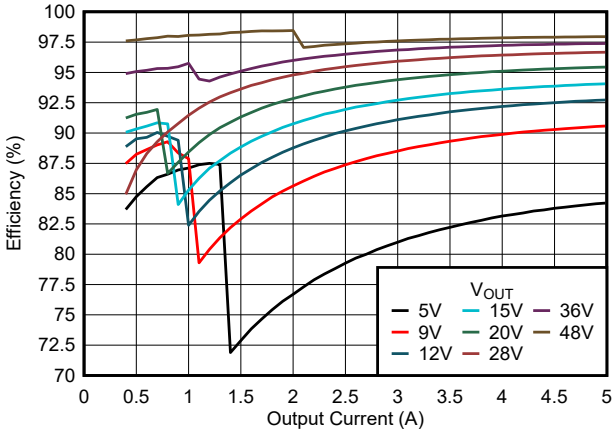


Figure 4-6. BOM5 Efficiency With V_{IN}=48V

The key takeaway here is that the end application can inform the operating conditions and BOM selection. Efficiency is highest when VIN is close to VOUT. These decisions can largely determine the overall efficiency of the system.

Next, a closer examination of different gate drive voltages can be performed. Now, compare cases with the same input voltage, output voltage, and BOM but with different gate drive voltages:

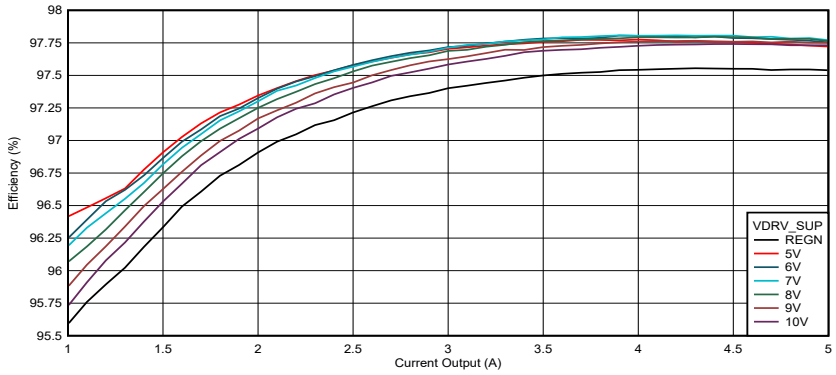


Figure 4-7. BOM2 With V_{IN}=20V and V_{OUT}=15V

Note, the device has an internal LDO that provides the gate drive voltage for the switching converter. Having an external drive omits the losses caused by the internal LDO, REGN. The higher the input voltage, the higher the LDO losses. This effect can be observed in the above figure.

To make the graph easier to read, Figure 4-8 is the gate drive supplies compared at only 5A.

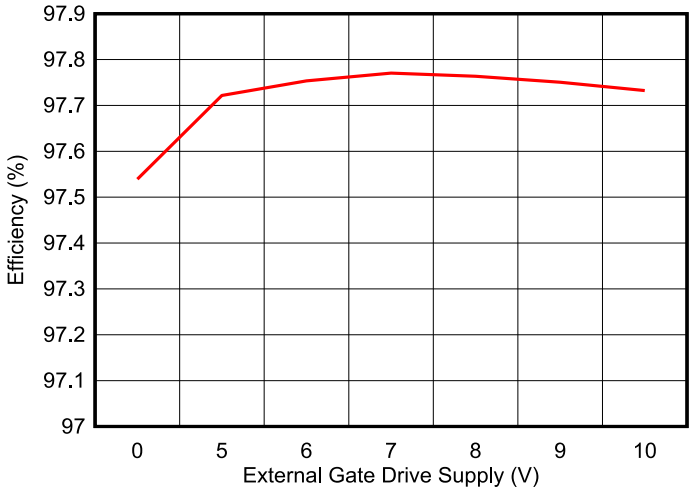


Figure 4-8. BOM2 With V_{IN}=20V, V_{OUT}=15V, and I_{CHG}=5A

In this case, 7V was found to be the voltage at which the switching losses and conduction losses are lower. For 10V, the switching losses increase to offset the reduced FET conduction gained. Figure 4-9 shows the increased efficiency with a 7V external gate drive.

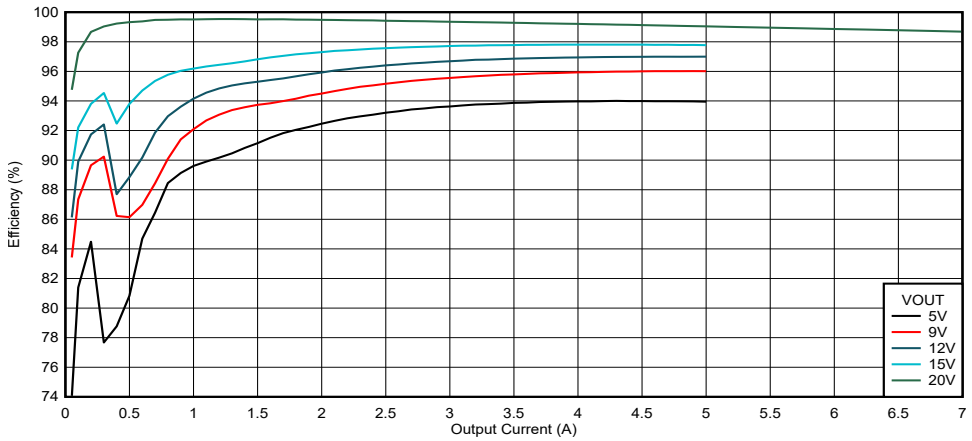


Figure 4-9. BOM2 With V_{IN}=20V and V_{DRV_SUP}=7

5 Summary

The BQ2575x family of devices can be used to create efficient charger systems for a myriad of applications. The efficiency of these systems can vary based on the operating conditions of the system and BOM selection, especially the MOSFET selection. The data sheet parameters of the MOSFET need to be reviewed and considered carefully, especially the gate charge parameters and the $R_{DS(ON)}$. How the MOSFET is used can impact these parameters so the operating conditions like the switching frequency, the gate drive voltage, and the output load need to be considered as well.

6 References

1. Texas Instruments, *GaN to the rescue! Part 1: Body-diode reverse recovery*, Technical Article
2. Texas Instruments, *BQ25756: Standalone/I²C Controlled, 1- to 14-Cell Bidirectional Buck-Boost Battery Charge Controller*, data sheet
3. Texas Instruments, *BQ25750: Standalone/I²C Controlled, 1- to 14-Cell Bidirectional Buck-Boost Battery Charge Controller with Direct Power Path Control*, data sheet
4. Texas Instruments, *BQ25758: I²C Controlled, Bidirectional Buck-Boost Controller with Wide Voltage Range*, data sheet
5. Texas Instruments, *BQ25756-Design-Calc*, design calculator
6. Vishay, *Measuring Power MOSFET Characteristics*, application note

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