Application Note

Challenges and Solutions for Half-Bridge Gate Drivers in Bidirectional DC-DC Converters

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ABSTRACT

Bidirectional buck-boost converters are used in applications such as electric vehicles DC-DC converters at high power and output current levels (>200A load). These multi-phase DC-DC converters are common in the 48V to 12V power systems found in mild hybrid automotive applications. These designs are typically multi-phase systems with the ability to enable and disable phases to optimize efficiency in different operating modes of the controller. These different operating modes pose unique operating conditions for the gate drivers that the designer needs to be aware of. The 100V half-bridge gate drivers are used in various high power, high power density applications with a 48V bus. These drivers are commonly used in the bidirectional DC-DC power systems and are the focus of this application note. This paper cover unique operational challenges with respect to driver bootstrap bias operation for gate drivers in the multi-phase buck-boost power systems used in automotive as well as grid power systems.

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1 Start-Up Operation

To maintain proper expected operation of the power converter, one must understand the start-up sequence of the half-bridge driver especially if using a bootstrap bias for the floating high-side driver. Some designers possibly may not be aware of the timing sequence of the half-bridge driver IC unless the designers encounter issues with the converter operation. For the driver outputs to respond to the LI (low-side) and HI (high-side) inputs, the VDD voltage level must be above the rising VDD UVLO (under voltage lockout) threshold. After the VDD UVLO threshold is satisfied there is a UVLO delay time before the outputs responds to the driver inputs. There is also a UVLO on the HB (high-side) bias, so the HB bias must be well above the rising HB UVLO threshold for the HO output to respond to the HI input. The HB UVLO circuit also has a delay time before the HO (high-side driver output) responds to the HI input.

To better understand the concerns of driver startup in a bidirectional DC-DC converter, we look at the driver start-up sequence in a standard DC-DC synchronous buck starting at 0V on the output as a reference.

The preferred startup sequence for the driver is to have VDD rise and well above the UVLO threshold before the PWM signals for LI and HI start. Since there is a UVLO delay on VDD, we recommend a delay of 10us or longer from VDD rising to the PWM signal start. In the typical synchronous buck with the output starting at 0V, there is a path from VDD through the boot diode to HB to charge the HB capacitor. This capacitor is charged when HS is close to ground which is the case at startup since VOUT is 0V and the output inductor provides a path from HS to ground, refer to Figure 1-1. The HB to HS capacitor charges at the same time that VDD is rising due to this path to the output which starts at 0V. Once VDD is above the UVLO threshold and HB-HS is above the UVLO threshold for 5-10us for most typical half-bridge drivers, the LO and HO outputs respond to the LI and HI inputs. Regarding the HB floating bias bootstrap circuit, the forward current in the driver boot diode typically has low forward current assuming the VDD rise time dV/dt is low which is the case in most systems. Typically, the bootstrap capacitor is fully charged before switching begins in the driver and power stage. Figure 1-2 shows this sequencing as well as how HS voltage rises to reverse bias the bootstrap diode.

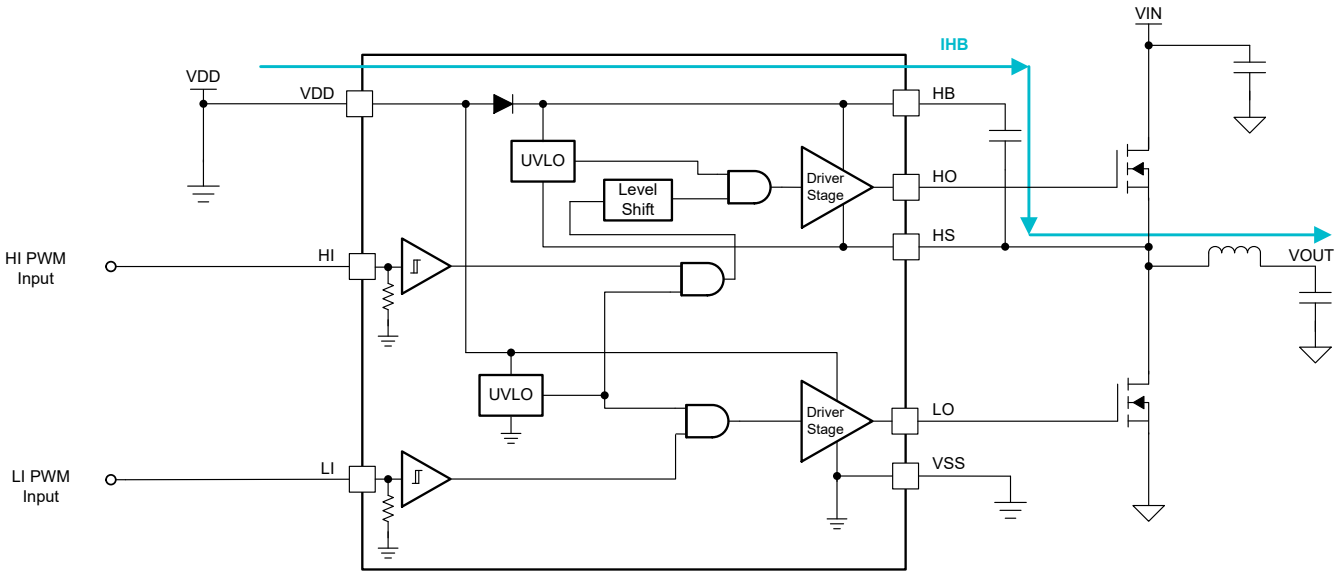

Figure 1-1. Simplified Synchronous Buck Showing Boot Capacitor Charging Path

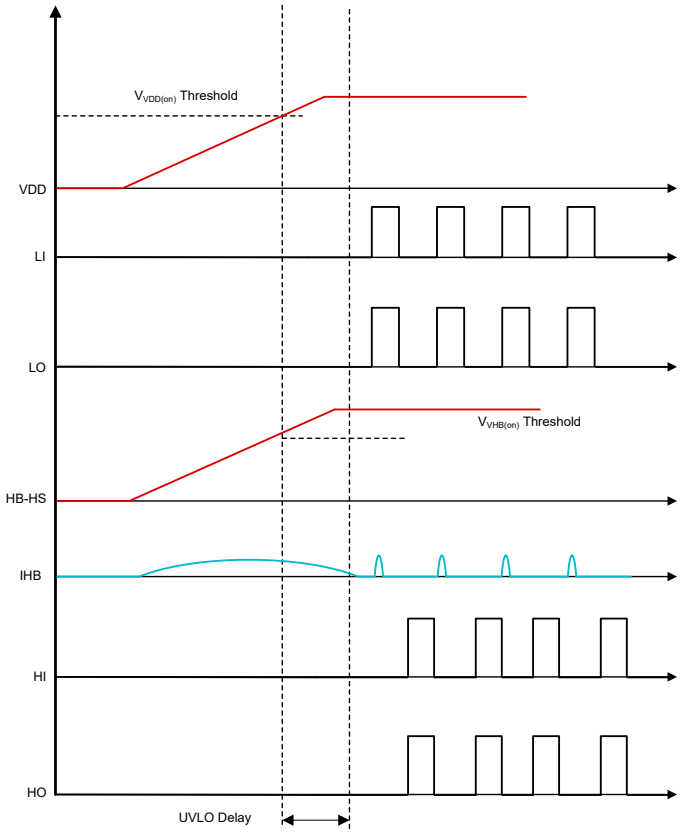

Figure 1-2. Synchronous Buck Timing Diagram

With bidirectional DC-DC converters many applications have multi-phase synchronous buck-boost to support high current outputs. A common practice to increase efficiency at lighter loads is to disable phases as the output current/power is decreased. Figure 1-3 illustrates a 2-phase configuration with one phase active and one in the inactive state. In practice there can be additional phases in the converter. In this case there is 12V on the output supplied by the active phase and the 2nd phase has the 12V output on the power stage switch node. On the inactive phase, the driver IC HS pin is at 12V which prevents the boot capacitor from charging assuming VDD is 12V or less. When the inactive phase starts switching the 1st LI input turns on the low side FET providing the charging path for the boot capacitor current (IHB) through the boot diode. Also, negative inductor current starts flowing from the 12V output through the low side FET as well. With 12V applied to the boot diode anode and high dV/dt on the HS pin, there is high initial boot diode forward current flowing. In many applications this can exceed 10A and significantly higher depending on the driver IC boot diode dynamic resistance. If the PWM pulses to the idle phase are enabled such that there is a short initial LO pulse, the forward current in the boot diode can be very high at the time the low side turns off. With 12V on the converter output there is negative current ramping in the output inductor when LO turns off. This negative inductor current results in the switch node transitioning high and clamping to the 48V input. This forces off the boot diode with high forward current flowing which results in potentially high reverse current in the boot diode. This reverse recovery stress can damage the internal boot diode.

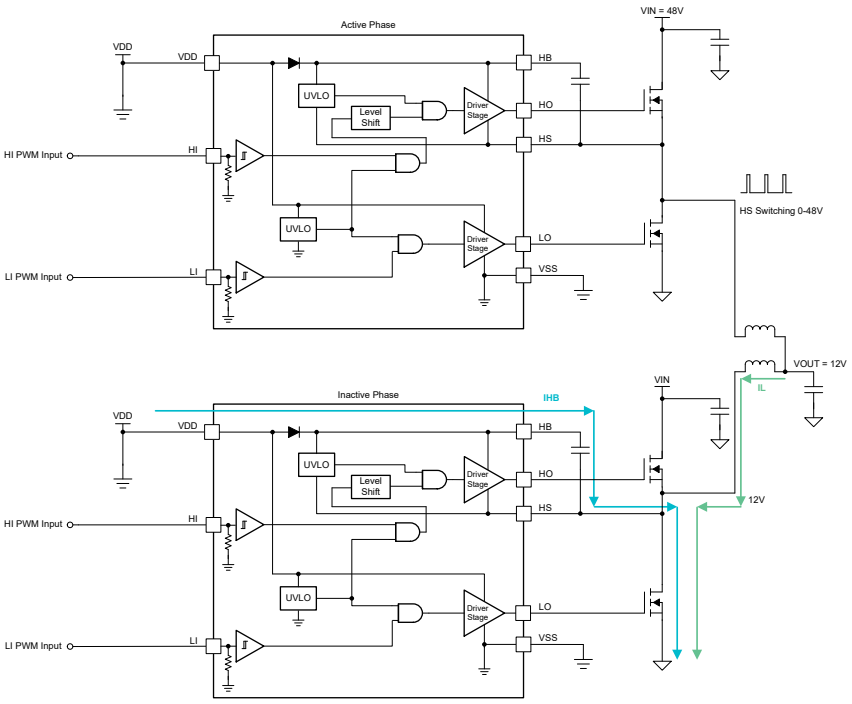

Figure 1-3. Multi-Phase Synchronous Buck-Boost HB Capacitor and Inductor Current Paths

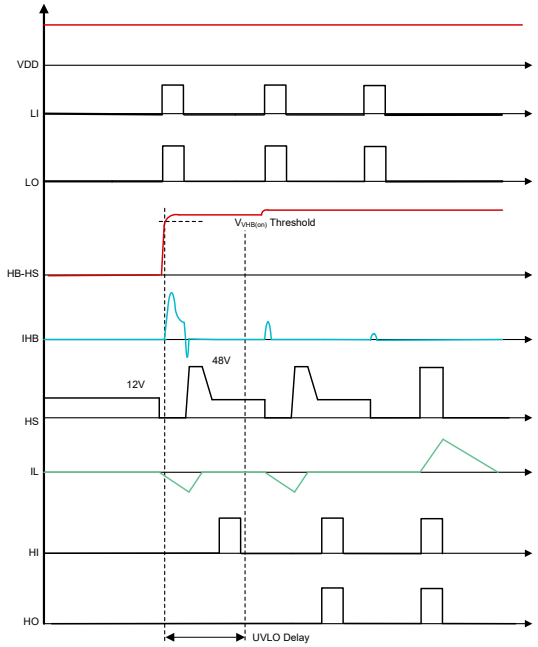

Figure 1-4. Timing Diagram of Inactive Phase Start-Up

2 Design Considerations

There are considerations in the design to help reduce the stress on the boot diode and ways to mitigate possible damage to the boot diode in the bidirectional DC-DC applications.

Firstly, proper sizing of the bootstrap capacitor is important to properly driving the power MOSFETs and also resulting in the fastest start-up of the HB-HS bias. We do not recommend oversizing the bootstrap capacitor in these applications.

There are additional design considerations that can address the gate driver and bootstrap start-up as follows:

1. Incorporate a low frequency LO pulse on the phase that is not actively delivering power. This makes sure that the HB-HS bias is fully precharged prior to the phase being enabled.
2. Make sure that when a phase is enabled, that the 1st initial LO pulse is a long pulse adequate to charge the bootstrap capacitor where the boot diode forward current has gone to zero or near zero. Random enabling of the phase during the normal HI and LI pulse widths can result in short LI initial pulse widths leading to high forward current flowing in the boot diode and then higher reverse recovery current when HS goes high.
3. Add an external Schottky diode in parallel with the driver internal boot diode. Use a small package diode to allow close placement to the IC VDD and HB pins with low V_F and low R_{DYN}.

3 Proper Sizing of Bootstrap and VDD Capacitors

Correct sizing of the bootstrap capacitor and VDD capacitors is important in any application but even more so in the bidirectional DC-DC converters. The following is a quick review of the process to select the bootstrap and VDD capacitor values. The application note "Bootstrap circuitry selection for half-bridge configurations" is also a good reference on this topic.

Initially, calculate the allowable voltage drop on the bootstrap capacitor from charging the MOSFET Q_G.

$$\Delta V_{HB} = V_{DD} - V_F - V_{HBmin} \quad (1)$$

Where...

- V_{DD} is the supply voltage of the gate driver device
- V_F is the bootstrap diode forward drop
- V_{HBmin} is the minimum HB bias voltage to drive the MOSFETs

Next determine the total charge needed per switching cycle from the bootstrap capacitor, normally this is dominated by the MOSFET Q_G.

$$Q_{TOTAL} = Q_G + I_{HBS}\, x \left(\frac{D_{MAX}}{f_{SW}}\right) + \left(\frac{I_{HB}}{f_{SW}}\right) \quad (2)$$

Where...

- Q_G is the total MOSFET gate charge on the high-side driver output
- I_{HBS} is HB to VSS leakage current from the data sheet
- D_{MAX} is the converter maximum duty cycle on the high-side MOSFET
- I_{HB} is the HB quiescent current from the data sheet

Lastly, the target minimum bootstrap capacitor value can be determined from the following equation.

$$C_{BOOTmin} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \quad (3)$$

The minimum bootstrap capacitance value is obtained from the above analysis to provide adequate bootstrap bias charge to properly drive the high-side MOSFET Q_G with adequate V_{GS}. The capacitor must be a high-quality dielectric such as X7R or better and the designer needs to consider tolerance with temperature and voltage applied and add some margin.

If the design cannot accommodate the suggested timing of the starting pulses of the LI input when a phase is enabled or a low frequency LI pulse cannot be accommodated to keep the HB-HS bias capacitor charged while idle, we advise to make provisions for an external boot diode in parallel with the internal boot diode in the driver. Also, selection of a 100V half-bridge driver such as the LM5101A, UCC2720x(A), UCC27211A, UCC27301A or UCC27311A is important.

The external boot diode must be a Schottky diode with a voltage rating adequate to meet the maximum voltage on HS in the worst-case operating condition including any HS voltage overshoot. Also the external diode V_F must be such that the external diode conducts the majority of the bootstrap charging current to reduce the stress on the driver internal diode. Placing the external diode close to the driver VDD and HB pins is important so a small package device is best for this.

Figure 3-1 shows the diode forward voltage curves of a good candidate for a 100V Schottky external diode which is in a small SOD123 package. Also shown in red are the driver internal boot diode V_F parameters at 80mA and 100uA.

You can see the red markers of the driver internal boot diode V_F is noticeably higher than the external diode which is the target. Also keep in mind the small package which is needed for close placement to the driver IC and choose a diode with high peak current capability since the boot diode can have high peak current during the initial charging pulse charging the bootstrap capacitor from 0V.

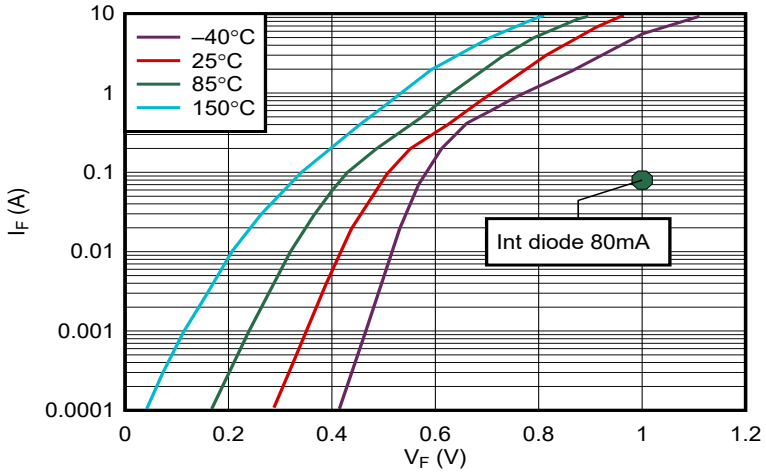

Figure 3-1. V_F Vs I_F of Example External Boot Diode

4 High Power Continuous Operation

The trend in many applications of bidirectional DC-DC converter is increasing power and output current levels. Multi-phase designs up to 3.6kW are not uncommon which can result in high current in each phase of 75A or higher. There are details in the operation that relate to the gate driver in steady state, high current operation that the designer must pay close attention to.

The timing of the low side MOSFET and high-side MOSFET switching has some dead time to prevent potential cross conduction of the MOSFET half-bridge. During the dead time when the low-side power MOSFET is off and the high-side power MOSFET is off the current flowing in the output inductor conducts through the body diode of the low side power MOSFET. During the dead time the voltage drop across the MOSFET body diode is higher than the voltage drop during the low side MOSFET on conduction which results in the switch node transitioning to a lower negative HS voltage level. This transition when the low side FET turns off and later the high-side MOSFET turns on results in details in the gate driver operation that are important to understand. Refer to the timing shown in Figure 4-1.

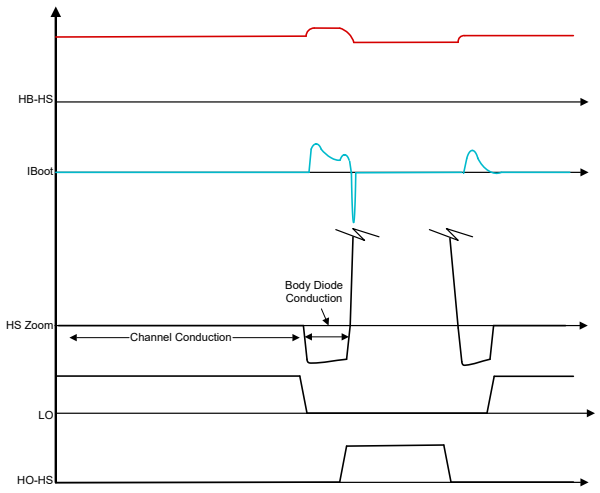

Figure 4-1. Detail Timing Diagram of Steady State HS Voltage and Boot Diode Current

The area of concern is the transition of the low side driver turn off, dead time and high-side driver turn on. When the low side driver and low side MOSFET is on the output inductor current is flowing through the MOSFET channel and the HS or switch node voltage is slightly negative based on the inductor current and MOSFET R_{DSON}. After the low side MOSFET turns off the inductor current flows through the low side MOSFET body diode which results in a more negative HS voltage based on the body diode forward drop. Referring to Figure 4-1, this increase in negative HS voltage causes the boot diode to start conducting to charge the HB capacitor back to the VDD- V_F of the boot diode resulting in boot diode forward current. The boot diode peak current during this time depends on the body diode forward drop and the boot diode dynamic resistance, which for a body diode drop of 1.5V and boot diode resistance of 1Ω can result in a 1.5A boot diode forward current. During the dead time the HO output of the driver transitions high to initiate the turn on of the high-side MOSFET which discharges the HB-HS capacitor to charge the high-side MOSFET Q_G. This causes some voltage drop on the bootstrap capacitor which also results in some forward current in the boot diode to restore the charge on the bootstrap capacitor. These two events cause the boot diode to start conducting current at a time close to when the high-side MOSFET turns on resulting in the switch node transitioning high. If the forward current in the boot diode has not decreased sufficiently to a low level when the switch node transitions high, this results in high reverse recovery current in the boot diode when forced off, possibly causing stress or damage on the internal boot diode.

Figure 5-1 shows the body diode forward current Vs forward drop of a 100V low R_{DSON} MOSFET to illustrate the shift in negative HS voltage during the dead time. The red marker indicates the maximum voltage at 40A which is at cold temp. One thing to keep in mind is the HS negative voltage shift of interest is the difference between the channel conduction and body diode conduction. You can see in the graph in Figure 5-1 that the body diode drop increases at cold temperature which is also the condition where the R_{DSON} voltage drop decreases due to the negative temperature coefficient of the MOSFET R_{DSON}.

5 Design Considerations

The ways to mitigate the possible overstress on the internal boot diode are the same as with the multiphase start up concern discussed earlier. Determine the required bootstrap capacitance to drive the high-side MOSFETs but do not oversize the capacitance value. Consider making provisions for an external boot diode with the same parameter recommendations previously discussed. Selecting a driver for these applications is important such as the LM5101(A), UCC2720x(A), UCC27211A, UCC27301A, or UCC27311A. Also, if the dead time between the low side MOSFET turn off to the high-side MOSFET turn on can be increased, this allows the boot diode current to reduce to a lower level before the switch node rises.

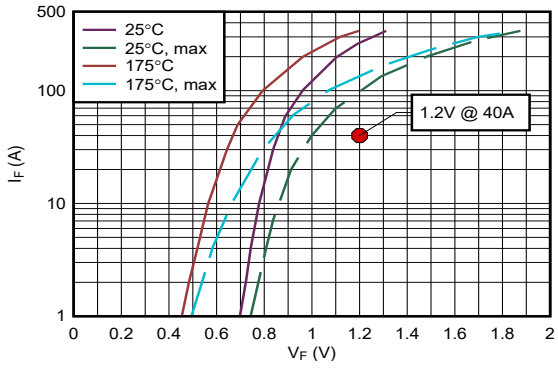

Figure 5-1. Power MOSFET Example Body Diode V_F Vs I_F

6 Summary

This application note has clearly identified some of the critical operating modes of bi-directional DC-DC converter where special design attention is needed from the half-bridge gate driver perspective. This paper has made very clear recommendation regarding boot-strap bias circuit design, including bootstrap diode and bootstrap capacitor. These guidelines and recommendation shall help many design engineers to build robust, efficient, and reliable bi-directional DC-DC converters for many automotive and industrial applications.

7 References

- Institute of Electrical and Electronics Engineers, *Bootstrap Voltage and Dead Time Behavior in GaN DC–DC Buck Converter With a Negative Gate Voltage* publication.

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