Application Note

BMS Breakers and Designing With TPS1210-Q1 and TPS4810-Q1 Low IQ Smart High-Side Drivers System Architectures

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ABSTRACT

With the overwhelming increase in the use of Lithium Ion batteries in today's automobile systems, the design of battery management systems (BMS) is becoming quite crucial. The battery management system monitors the battery and possible fault conditions, preventing the battery from situations in which it can degrade, fade in capacity, or even potentially harm the user or surrounding environment. The BMS is responsible to provide an accurate state-of-charge (SOC) and state-of-health (SOH) estimate to make sure an informative and safe user experience over the lifetime of the battery. Designing a proper BMS is critical not only from a safety point of view, but also for customer satisfaction. There is also definitive move towards solid state disconnects from contractors and this brings in new system design challenges to realize a high current disconnect switch. Robust protection during system fault conditions and low IQ requirement adds another layer of complexity while designing these systems.

This application note highlights how the new TPS1210-Q1 and TPS4810-Q1, low IQ dual high-side driver simplifies the high current disconnect switch design for BMS system with various features such as protection during various system fault conditions, capacitive load driving and diagnosis of the external FETs and the gate driver for safety applications.

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Trademarks

1 Introduction

The TPS1210-Q1 and TPS4810-Q1 is a family low IQ, smart high side drivers with protection and diagnostics targeted for BMS breaker application. TPS1210-Q1 has an operating voltage range of 3.5V – 40V, and is designed for 12V, system designs whereas the TPS4810-Q1 has an operating voltage range of 3.5V – 80V with 100V of absolute maximum rating making TPS1210-Q1 designed for 48V system designs. The devices has two strong (2A) GATE drivers with separate control inputs (INP1, INP2) to drive back-to-back MOSFETs in common source configuration. Strong GATE driving enables power switching using parallel FETs in high current system designs. The device provides configurable short-circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. Current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. Diagnosis of the integrated short circuit comparator is possible using external control on SCP_TEST input. The device indicates fault ($\overline{FLT}$) on open drain output during short circuit, charge pump undervoltage, and input undervoltage conditions. Low Quiescent Current of 35µA in operation enables always ON system designs. Quiescent current reduces to 1.5µA (typical) with EN/UVLO low.

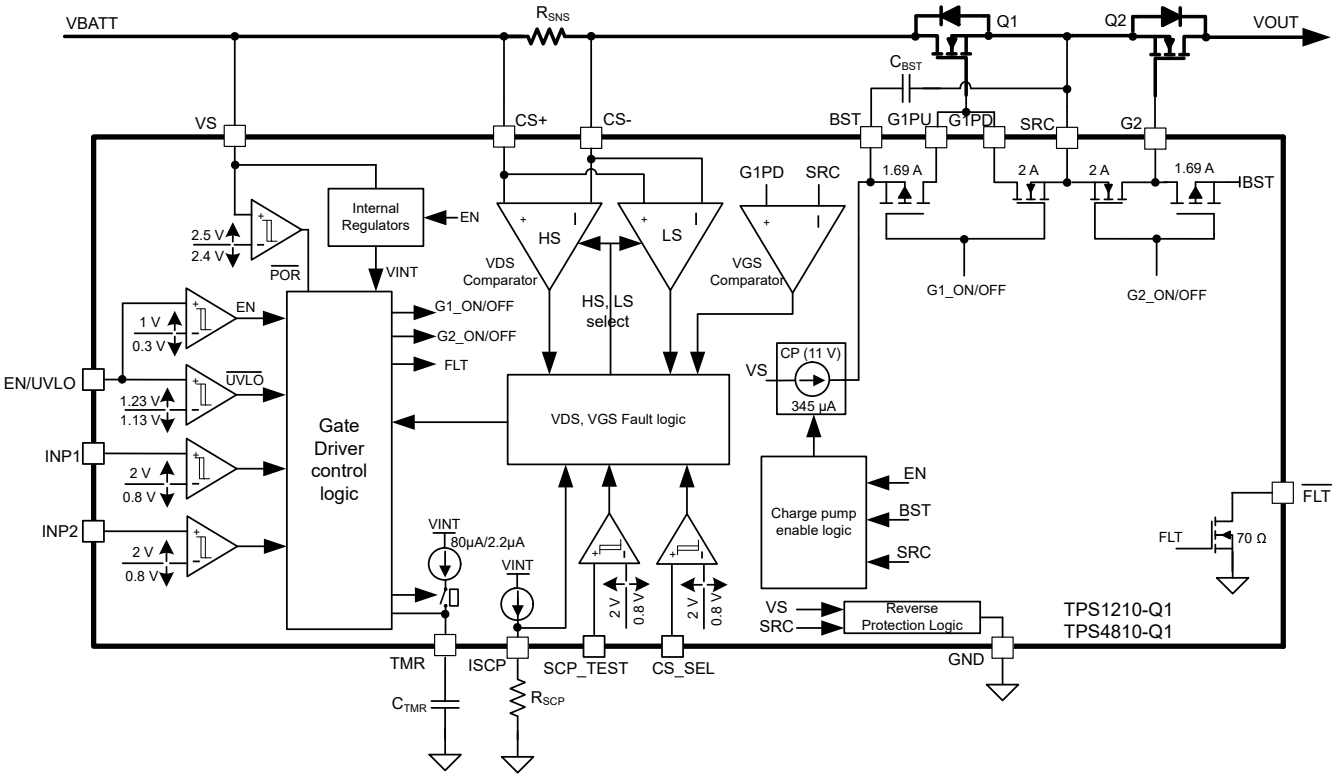

Figure 1-1. Functional Block Diagram

2 BMS System Overview

Battery management system (BMS) monitors, protects, and optimizes battery performance of the electric vehicle battery.

Figure 2-1 and Figure 2-2 shows the block diagram of the BMS system.

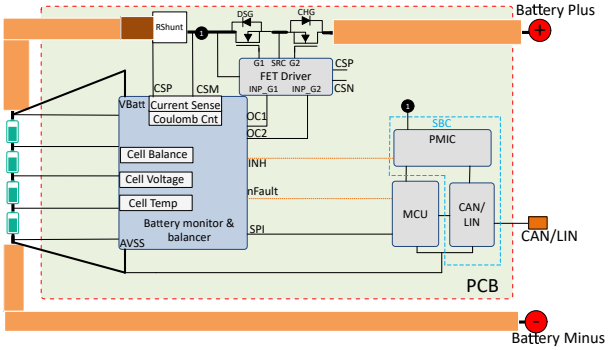

Figure 2-1. BMS System With High Side Current Sensing

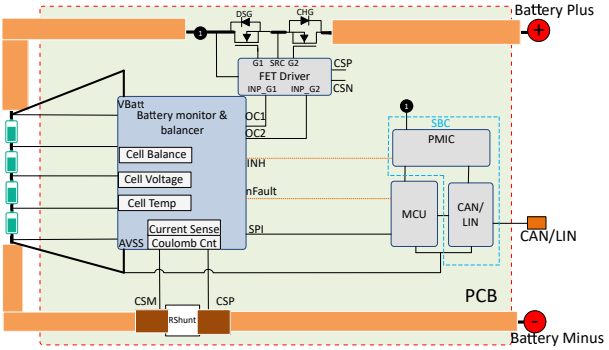

Figure 2-2. BMS System With Low Side Current Sensing

The BMS system typically comprises of cell monitor and balancing unit to diagnose cell voltages and temperature, balance cell characteristics and communicate with the system controller. A shunt resistor is placed either on the high side or on the low side for sensing current through the battery cells for couloumb couting and protection.

Battery disconnect switches disconnect the battery cells from the charger and the loads during system fault conditions such as over temperature of the cells, over currents during charging and discharging making sure EV safety during parking, charging, and discharging.

The Switches are in a back to back configuration to block the current in charge and discharge directions during the system fault. Based on the end-application goals the back to back switches can need to be controlled separately or together at the same time.

Some system design architectures for the battery disconnect switches based on the TPS1210-Q1 and TPS4810-Q1 high side drivers and the associated end-application goals are outlined in the following sections.

3 Application of TPS1210-Q1 and TPS4810-Q1 to accomplish the Battery Disconnect Switch Design

The battery disconnect switch is responsible for the entire control of the switches that connect and disconnect the battery from the load. The battery disconnect switch needs to accomplish the following tasks with diligence and precision:

1. Drive parallel branches back to back FETs between the battery and the load.
2. Provide protection to the BMS as well as the down stream components from short circuit current and reverse polarity.
3. Provide diagnostic support for hassle free debug in the event of a failure or malfunction.
4. Have low power dissipation to maintain the thermal stability inside the battery pack.

The previous features, if not more, can be realized using the TPS1210-Q1 and TPS4810-Q1 high-side drivers in the battery disconnect switch design.

3.1 Separate Charge and Discharge FET Control

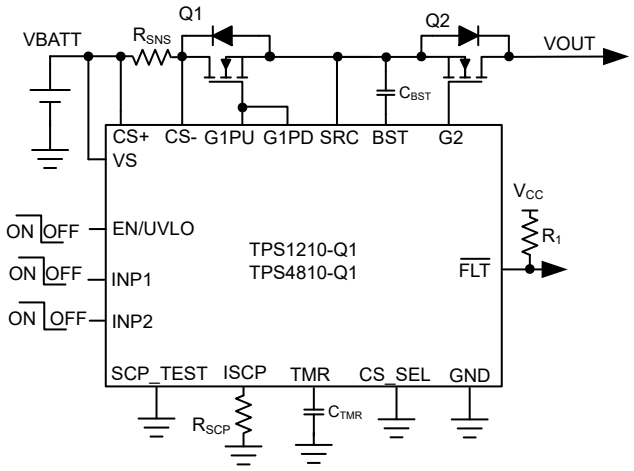

Figure 3-1. Application Circuit for Separate Charge and Discharge FET Control

The devices have two gate drivers (G1, G2) and gate control inputs (INP1, INP2) which can be used to control the discharge FET (Q1) and the charge FET (Q2) separately. With this feature, following four different modes of operation of the switches can be supported in the BMS system.

- **Fully ON state with discharge and charge FETs ON** – In this mode of operation, current is allowed to flow in both discharge and charge directions.
- **Fully OFF state with discharge and charge FETs OFF** – In this mode of operation, the battery is completed disconnected from the load. This condition can happen during system fault conditions.
- **Ideal Diode from battery to load with discharge FET ON and charge FET OFF** – In this mode of operation, current is allowed to flow from battery to load only. Battery charging is disabled in this state as the charge FET is turned OFF. Load current flows through the discharge FET and the body diode of the charge FET. This state of the switches can be used in 12V BMS systems when the system is in sleep state but the always ON loads need to be powered. In sleep state of the system the battery cell monitoring and balancing functions are disabled to reduce the system level IQ hence blocking the charging path makes sure that the uncontrolled charging of the battery does not happen.
- **Ideal Diode from load to battery with discharge FET OFF and charge FET ON** – In this mode of operation, battery discharging is blocked and only charging is allowed. This condition can happen when the battery voltage level is very low or if the battery is in a deep discharged state.

3.2 Charge, Discharge FET Control With Pre-Charge Functionality

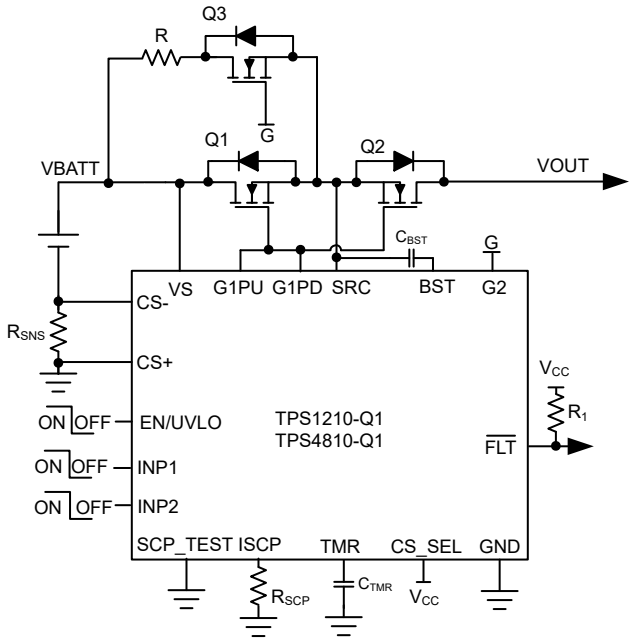

Figure 3-2. Application Circuit for Pre-charge Functionality

Loads such as ECUs, motor drives can have large amount of input capacitance. To limit the high inrush current during power up pre-charge feature of the TPS4810-Q1 and TPS1210-Q1 can be used. These devices can be configured as shown in Figure 3-2 to drive back to back FETs in the main path and also a parallel pre-charge FET. INP1 controls the Q1, Q2 FETs in the main path and INP2 controls the pre-charge FET Q3.

Once the load capacitor charges close to battery voltage then the main FET path can be turned ON and the pre-charge path can be turned off using the INP1 and INP2 control inputs.

3.3 Current Sensing for Short Circuit Protection

In the event of a short circuit on the load side, it is critical to disconnect the FETs as soon as the fault occurs to protect the downstream components as well as to avoid any damage in the system. TPS4810-Q1 and TPS1210-Q1 devices provides a robust short circuit protection.

The CS+ and the CS- pins are used to sense the load current flowing in the system either by connecting a very small sense resistor or through FET VDS sensing. The device supports various current sense configurations as shown in below application diagrams.

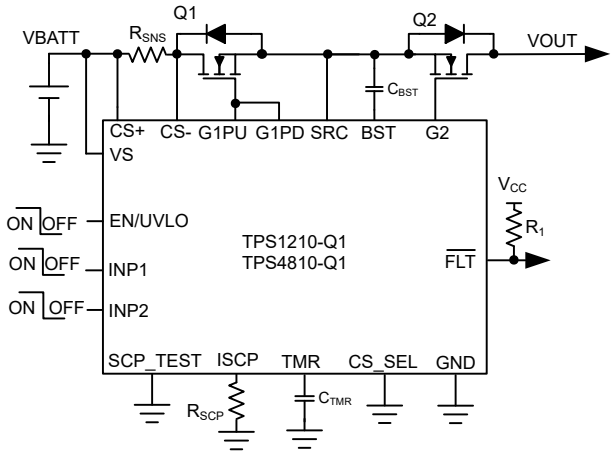

Figure 3-3. High-Side Rsense Based Current Sensing

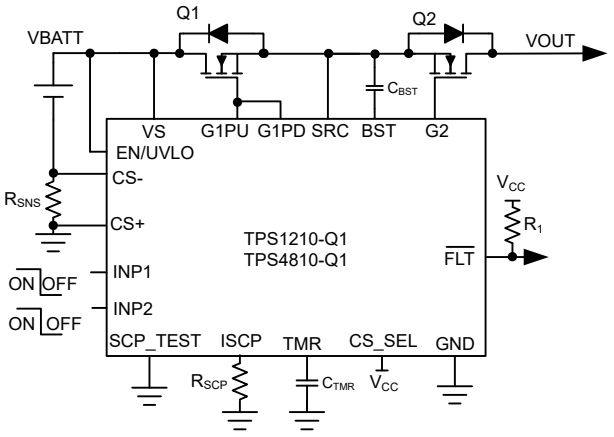

Figure 3-4. Low-Side Current Sensing

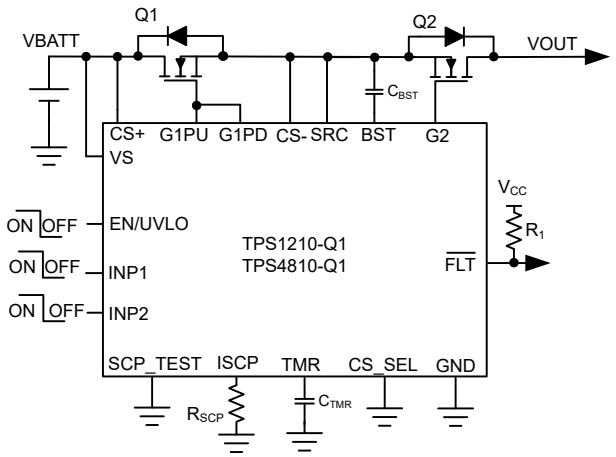

Figure 3-5. High-Side MOSFET VDS Based Current Sensing

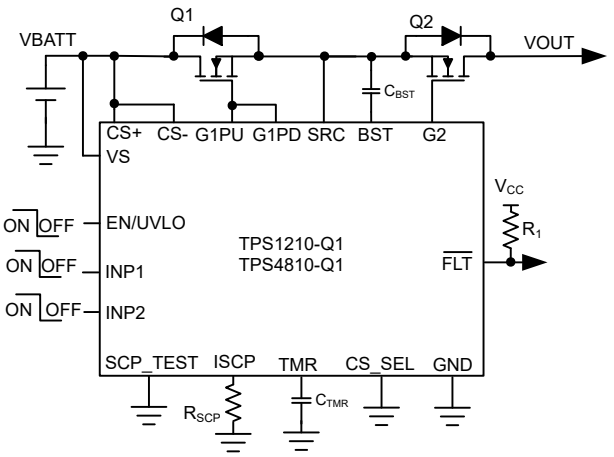

Figure 3-6. Without Current Sensing

3.4 Reverse Polarity Protection

Reverse polarity faults occur during installation and maintenance of the end equipments. The TPS4810-Q1 and TPS1210-Q1 devices have integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Back to back FETs are turned OFF in such events to protect the load and the battery. The device is tolerant to reverse polarity voltages down to -65V both on input and on the output. On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems the output negative voltage level can be limited within -65V by external clamps such as a TVS or a diode.

3.5 Diagnostics

BMS is a safety critical end equipment and the BMS disconnect switches are responsible for critical functions of charge, discharge control for battery cell and load protection. One of the key requirements in such system designs is the FET diagnosis for functional availability of the charge and discharge function and the short circuit protection comparator diagnosis.

3.5.1 FET Diagnostics

A diagnosis concept to verify the functional availability of the battery disconnect switch needs to be implemented without disconnecting vehicle loads. Therefore, either a separate by-pass connection or several switched parallel channels shall be used as shown in Figure 3-7.

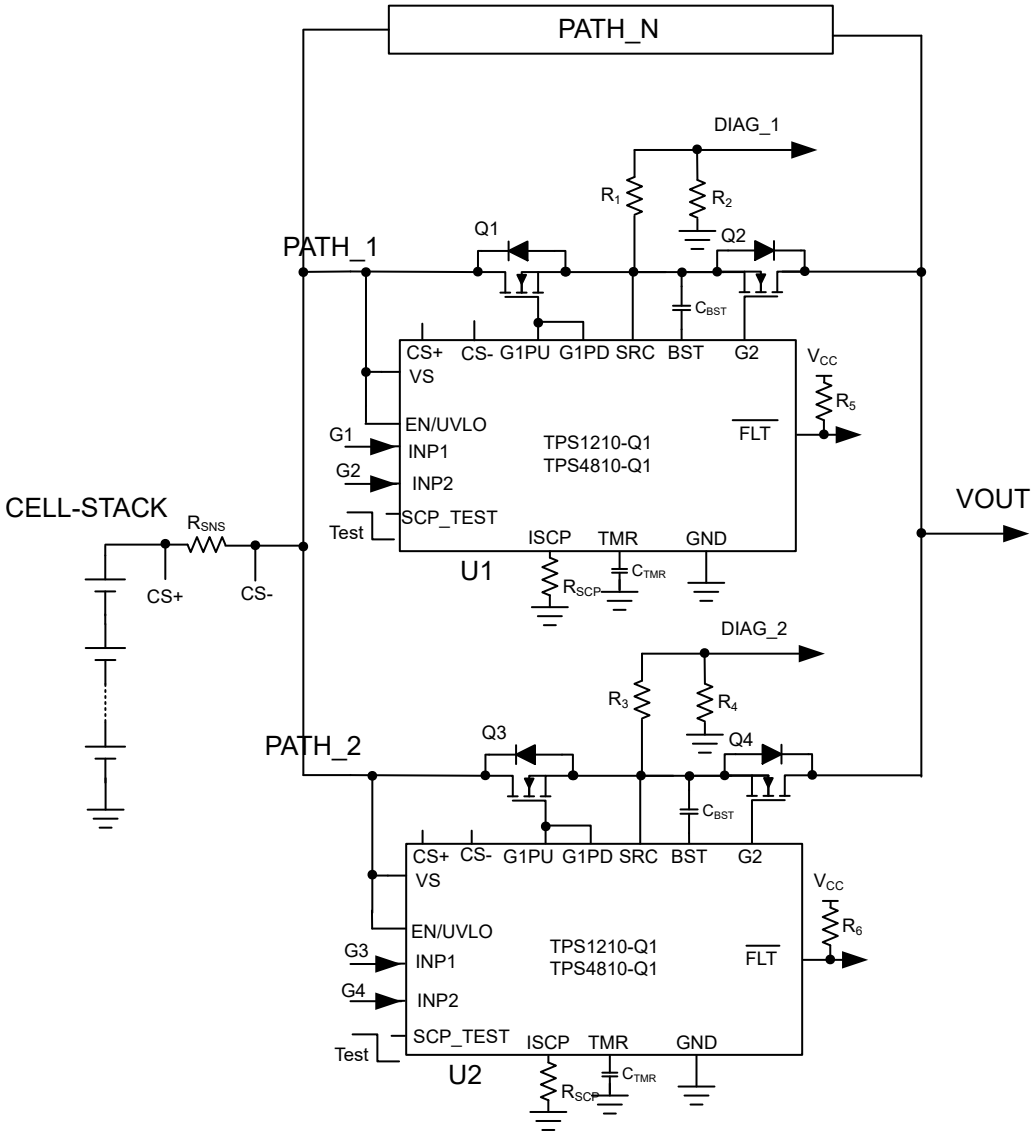

Figure 3-7. System Configuration With Switched Parallel Channels for FET Diagnosis

By this arrangement of parallel disconnect switches, one of the paths can be opened and the functionality of the disconnect switch on the other path can be verified during vehicle operation without disconnecting the vehicle loads. The diagnosis is done during low current operating mode of the vehicle. For verification of the availability of the discharge function the voltage (DIAG_x) in between the charge and discharge circuit breaker shall be measured.

The Table 3-1 gives the information on how the diagnostics can be performed for the charge and discharge FETs.

Table 3-1. Input Control Signals Sequence and FET Status

INP1	INP2	Q1 status	Q2 status	V(DIAG_1)	FET diagnosis result
Low	Low	Stuck OFF	OFF	Low	
High	Low	Stuck OFF	OFF	Low	Q1 stuck OFF detected
Low	High	Stuck OFF	ON	High	
Low	Low	OFF	Stuck OFF	Low	
High	Low	ON	Stuck OFF	High	
Low	High	OFF	Stuck OFF	Low	Q2 stuck OFF detected

The same approach can be followed for determining the diagnostics of Q3 and Q4 as well. Hence, having two separate gate controls enables diagnostic features, which determine the state of the FET. This can help in safe turn ON and OFF of the BMS power path.

3.5.2 Short Circuit Protection Comparator Diagnostics

The short circuit event is highly critical for any system especially the BMS. The integrated short circuit protection comparator can be diagnosed to check its functionality by using the SCP_TEST pin. When the SCP_TEST pin is driven low to high then, a voltage is applied internally across the SCP comparator inputs to simulate a short circuit event. If the gate drive and $\overline{\text{FLT}}$ goes low then it indicates that the internal short circuit protection comparator is good otherwise it is to be treated as SCP feature is not functional. If the SCP_TEST feature is not used, then connect SCP_TEST pin to GND. The SCP comparator diagnosis can be performed before system startup.

3.5.3 Fault Indication

The fault indication is an important feedback from the IC to the BMS. In an event of a short circuit fault, gate driver UVLO, UVLO and SCP_TEST, the $\overline{\text{FLT}}$ is asserted. The $\overline{\text{FLT}}$ is an open drain pin, and when pulled up to a voltage source with the help of a resistor, the $\overline{\text{FLT}}$ reads high when there is no fault and during a fault condition, the pin reads low. The value of resistor to be used can be determined from the specifications of the $\overline{\text{FLT}}$ pin from the data sheet.

4 Summary

With the features such as integrated 2A gate drivers with seperate gate controls for back to back FET driving, high-side, low side current sensing with low IQ, the TPS4810-Q1 and TPS1210-Q1 devices offer flexibility in design architectures for 48V and 12V BMS systems addressing the protection and diagnosis requirements for Battery disconnect switch designs.

5 References

- Texas Instruments, *TPS1210-Q1 45-V, Automotive Low IQ, Back-to-Back MOSFET Smart High Side Driver With Short-Circuit Protection and Diagnostics*, data sheet.
- Texas Instruments, *TPS4810-Q1 100V Automotive Low IQ, Back-to-Back MOSFET Smart High Side Driver With Short-Circuit Protection and Diagnostics*, data sheet

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