Application Note

Design Considerations of Stacked BQ769x2 With High-Side N-MOSFET

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ABSTRACT

One single BQ769x2 family battery monitor can support up to a 16s battery pack which is good enough for 36-V and 48-V applications. For 60 V and higher battery packs, two stacked BQ769x2 family monitors are required. This document describes how to stack devices for the BQ769x2 monitor family and utilize the integrated charge pump to drive high-side N-channel MOSFETs. The key design considerations are analyzed to secure fast and robust MOSFET switching on and off times, minimize the current gaps between two stacked groups, and enable easy communications design between the stacked BQ769x2 devices and host MCU.

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Trademarks

1 Introduction

Because of the weight limit and longer endurance needs, the battery cell chemistry of the e-motorcycle, light electric vehicles, and garden tool battery packs is shifting from Lead-acid to Li-ion, Li-polymer, or Li-ion phosphate (LiFePO4) types and the pack voltage is shifting from 36 V or 48 V to 60 V or 72 V, or even higher. For 60 V and higher battery packs, two stacked BQ769x2 family monitors are required.

One critical requirement of a battery pack is how to attain safe use during the entire battery pack lifetime. The stacked BQ769x2 family monitor architecture spawns some challenges of how to monitor the information of all battery cells and detect unsafe working conditions, and how to control the on and off switches to protect the battery pack away from dangerous use-cases. TI released the TIDA-010247 reference design where a stacked BQ769x2 family monitors a battery-pack design with high-side N-MOSFET control. Figure 1-1 shows the TIDA-010247 block diagram. This document identifies the common design challenges in stacked BQ769x2 family monitor architecture and explains how to address the challenges.

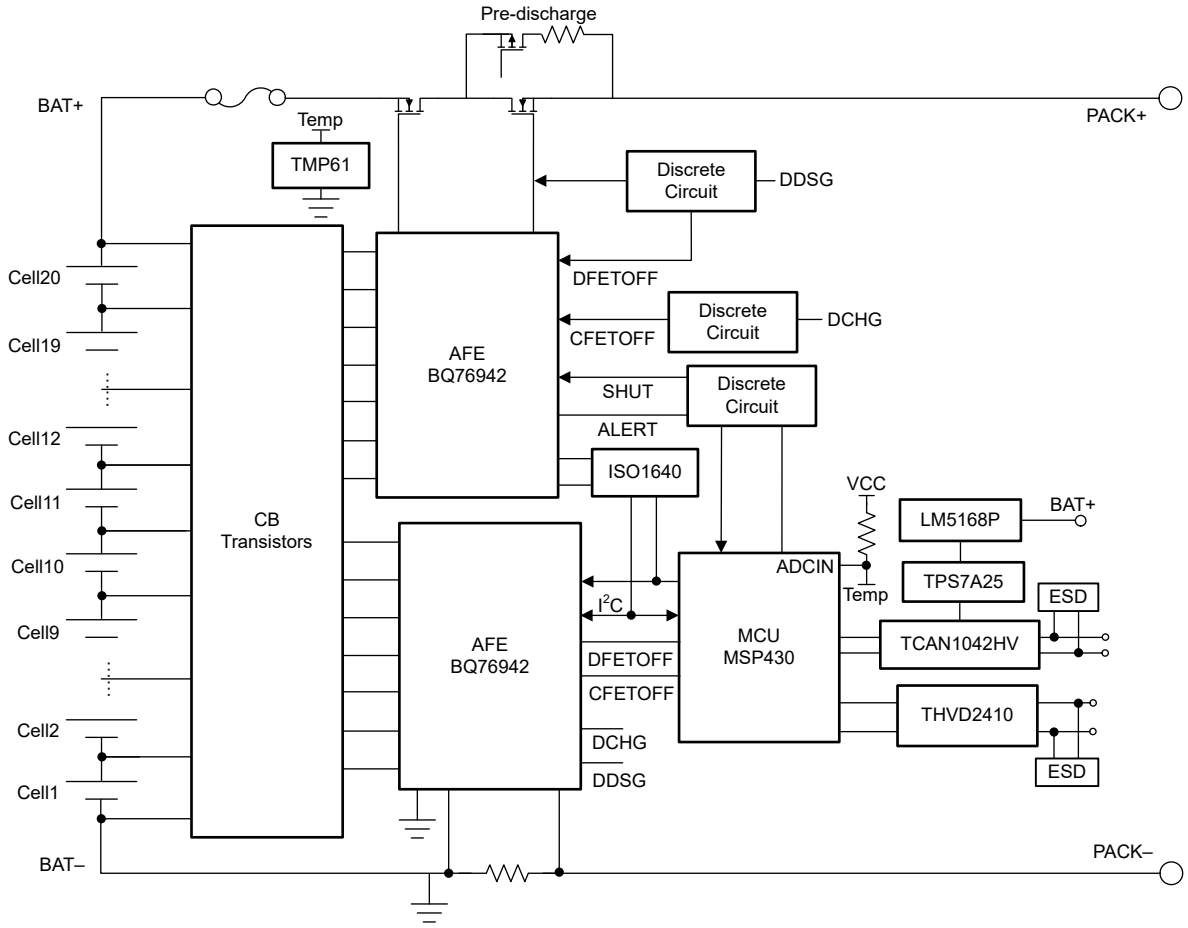

Figure 1-1. TIDA-010247 Block Diagram

2 Stacked AFE Communication

To cover battery packs with higher than 16s cells, and greater than 60-V applications, two BQ769x2 family monitors are stacked to monitor up to 32s battery cells. Each BQ769x2 monitors up to 16s battery cells in one group. The bottom BQ769x2 shares the same ground with the whole pack and MCU, while the top BQ769x2 references the stack voltage of the bottom group. Therefore, an isolation device or a high-voltage level shifter is required for the communications between the top BQ769x2 and the MCU.

2.1 Data Communications

The BQ769x2 supports both I2C and SPI communications. The TIDA-010247 uses an I2C isolator, ISO1640, for up to 400-kHz isolated I2C communication between the top BQ769x2 and host MCU. To simplify the hardware design and save MCU resources, two stacked BQ769x2 devices are connected with the I2C bus. The two target BQ769x2 devices share the same I2C address by default, causing conflicts to any host I2C commands. *Importantly*, the BQ769x2 supports changing the I2C address with one-time programmable memory (OTP), making it easier for host MCU to communicate with two BQ769x2 devices separately without any conflicts. There are two ways to program OTP for the BQ769x2; with the TI GUI or the host MCU. More OTP details are found in the BQ769x2 Calibration and OTP Programming Guide and it is sufficient to perform OTP programming on only the bottom BQ769x2 with a different I2C address. The secondary side of ISO1640 must be powered on before the communications with the top BQ769x2. One way to accomplish this is to add an *isolated power module* to make sure both sides are powered off of the ISO1640. An easier option is to use the BQ769x202 version of the device, which enables the REG1 3.3-V output by default, and powers both sides of the ISO1640 with BQ769x2 REG1. For the other versions of the device, the top BQ769x2 also needs OTP programming to enable the REG1 output.

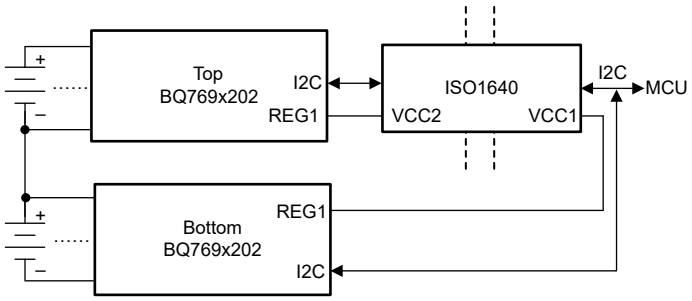

Figure 2-1. Communication With the Top and Bottom BQ769x2

Table 2-1. Default Configurations of Different BQ769x2 Versions

Part Number	Communications Interface	CRC Enabled	REG1 LDO Default
BQ769x2	I2C	N	Disabled
BQ769x201	SPI	Y	Disabled
BQ769x202	I2C	Y	Enabled, 3.3 V
BQ769x203	SPI	Y	Enabled, 5 V
BQ769x204	SPI	Y	Enabled, 3.3 V

2.2 Control Signals

As for the other relatively slow switching signals, like ALERT, TS2, RST_SHUT, DFETOFF, CFETOFF, use discrete level shifters or optocouplers which are more cost-effective.

Since the bottom BQ769x2 monitors the pack current, bottom group cell voltages and temperature, but also the charge and discharge MOSFET are driven by the top BQ769x2, allow the bottom BQ769x2 to turn off the charge and discharge MOSFETs directly without the host MCU. This is especially helpful for faster protections like SCD. In TIDA-010247, the DDSG and DCHG pins of the bottom BQ769x2 are configured for DDSG and DCHG functionality and the DFETOFF and CFETOFF pins of the top BQ769x2 are configured for DFETOFF and CFETOFF functionality. Two discrete level shifters allow the bottom BQ769x2 DDSG and DCHG to control the top BQ769x2 DFETOFF and CFETOFF separately. The bottom BQ769x2 DDSG is also ORed with an MCU IO to drive Q47 to make sure the discharge MOSFET is completely off, so DDSG has to be configured as active-high (more details for the MOSFET driver are described in High side N-Channel MOSFET). But DCHG is configured as active-low to save power.

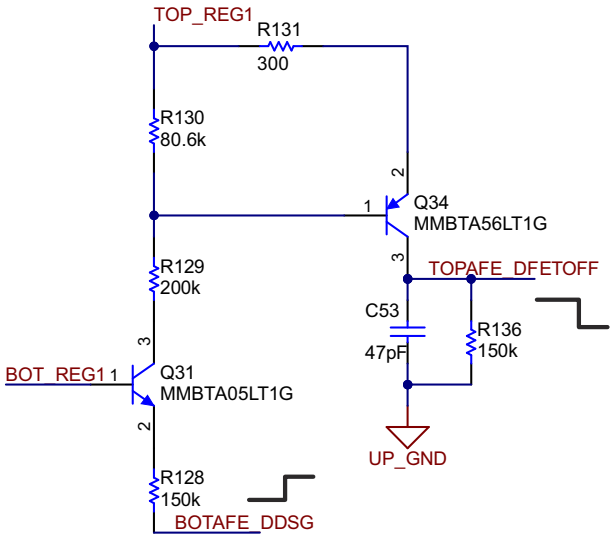

Figure 2-2. DDSG Level-Shifter Circuit

3 High-Side N-Channel MOSFET

The TIDA-010247 supports a high-side N-channel MOSFET architecture and uses the top BQ769x2 charge pump to drive the MOSFET on and off. The high-side MOSFET architecture always secures the ground connection, being good for communications between pack and outside but have new design challenges. Since the top BQ769x2 references the bottom stack voltage, when the top BQ769x2 tries to turn the DSG MOSFET off, the DSG pin voltage drops towards the LD pin voltage and finally to the bottom stack voltage (top BQ769x2 ground), the bottom stack voltage is too high to completely turn the DSG MOSFET off. The TIDA-010247 uses a discrete circuit (shown in Figure 3-1) to make sure the DSG MOSFET turns off completely and quickly.

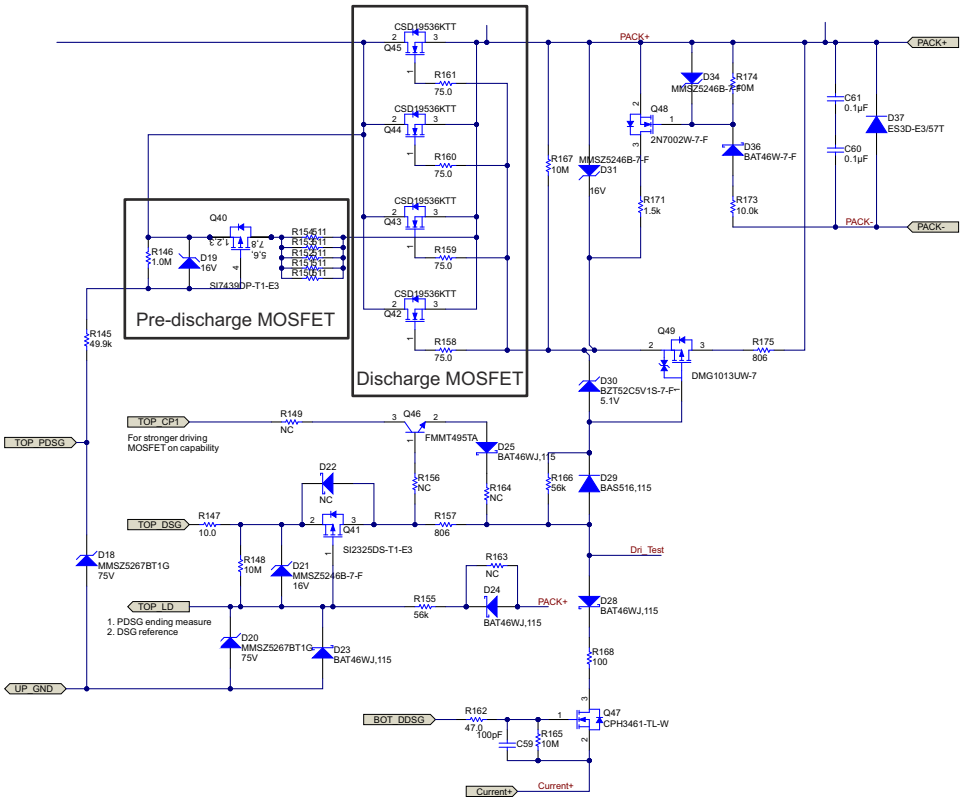

Figure 3-1. High-Side MOSFET Drive Circuit in TIDA-010247

3.1 Discharge MOSFET Turn On and Off Processes

The MCU or bottom BQ769x2 DDSG turns on Q47 when the system needs the DSG MOSFET off which drives the Dri_Test node low. P-channel MOSFET Q49 is turned on to discharge gate-source voltage of the DSG MOSFET with R175. Zener D30 protects the Q49 source-gate voltage. The top BQ769x2 device drives TOP_DSG towards TOP_LD to turn off Q41, blocking further discharging of the charge pump and allowing Dri_Test to reach ground to make sure the DSG MOSFET turns off completely. D21 and R148 protect the Q41 gate-source voltage and make sure that Q41 is in the off state. When the DSG MOSFET is completely off, the PACK+ voltage is low, D24 blocks current from UP_GND and TOP_LD to charge PACK+ and protects the top BQ769x2 from negative voltage. Q47 is able to be turned off to save power after the DSG MOSFET turn off process finishes.

When the system needs to turn the DSG MOSFET on again, the system first checks that Q47 is off and then drives TOP_DSG with the top BQ769x2 charge pump voltage. Q41 is on and charges gate-source voltage of the DSG MOSFET through R147, Q41, R157, D29, and D30. Since D24 blocks TOP_LD from following PACK+ when PACK+ is low, TOP_LD can be charged too fast to slow down the turn on process of Q41. This design reserves R163 in parallel with D24 on the board but leaves R163 unconnected for lower current consumption. Schottky D23 is reserved to prevent negative voltage on TOP_LD for protection.

3.2 PACK Port High Voltage

Energy recovery when braking is a requirement for some motor-driving applications. If the battery is fully charged and both charge and discharge MOSFETs are off, the PACK side can have a high voltage, damaging the BQ769x2 if the PIN voltage is higher than 85 V. One easy way to block high voltage is to add a series diode D29 between the discharge MOSFET and TOP_DSG, but the diode also blocks the sink current to turn off discharge MOSFET. A resister R166 is connected in parallel with D29 to supply a current path to turn on Q49 when turning off the discharge MOSFET. D20 and R155 protect TOP_LD voltage over the maximum limitations of the top BQ769x2. D20 is also helpful to limit the TOP_DSG voltage because the DSG pin is always driven toward LD pin when turning the discharge MOSFET off. For the other high-voltage pins of both the top BQ769x2 and bottom BQ769x2, the Zeners and resisters are always helpful to limit the voltages within the absolute maximum values. But if these high-voltage pins are used for voltage measurement, further calibrations are normally required to secure good accuracy with the protective Zeners and resisters.

3.3 Quickly Turning Off the Discharge MOSFET

Turning off the discharge MOSFETs quickly is necessary, especially in the event of a short-circuit discharge (SCD) fault. When an SCD fault occurs with the MOSFET on, discharge current increases to a very large value and triggers the SCD protection to turn off the discharge MOSFET. The discharge current drops quickly, generating significant negative voltage on PACK+ because of the parasitic inductance of the short-circuit connectors and PCB traces. Negative voltage on PACK+ prevents current into the Zener D30 cathode and makes Q49 turn off, slowing down the discharge MOSFET turn off process. Diode D37 is necessary to limit the maximum negative voltage. Considering the discharge current can be huge and the D37 forward voltage can potentially reach the gate-source threshold voltage (Vgs_th) of the discharge MOSFET, Q48, R171, D34, R174, D36, and R173 are added to supply another path to discharge the input capacitance (Ciss) of the discharge MOSFET and speed up the turn off process. When Q48 is on because of negative voltage on PACK, Ciss of the discharge MOSFET discharges through Q48 and R171. To make sure the circuit works normally, Q48 has to be on before gate-source voltage of discharge MOSFET reaches the Vgs_th of the discharge MOSFET, considering the voltage divider of R174, R173, and D36. This condition is also necessary to make sure the discharge MOSFET is off for the reverse voltage tests on PACK side. D36 eliminates leakage current when PACK has normal high voltage and R173 limits current when the PACK side has a very high negative voltage, protecting D34 and Q48.

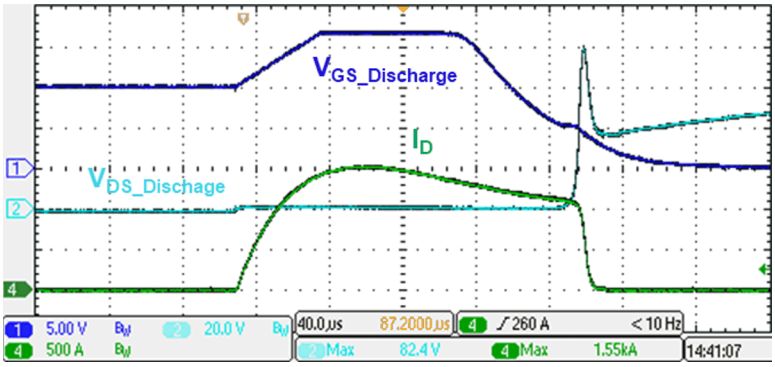

Figure 3-2. TIDA-010247 SCD Protection

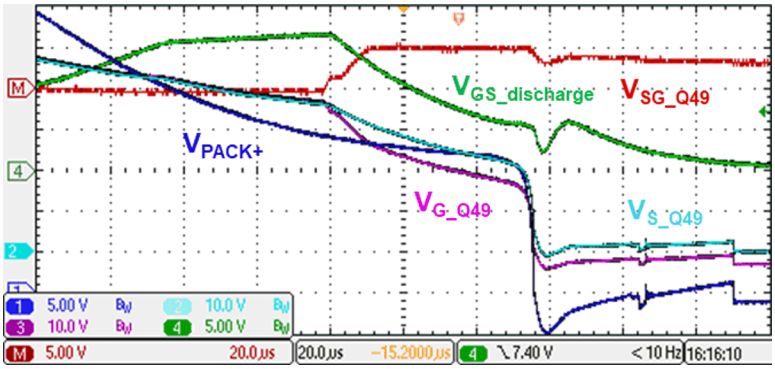

Figure 3-3. Turning Off Discharge MOSFET With Q49 at SCD

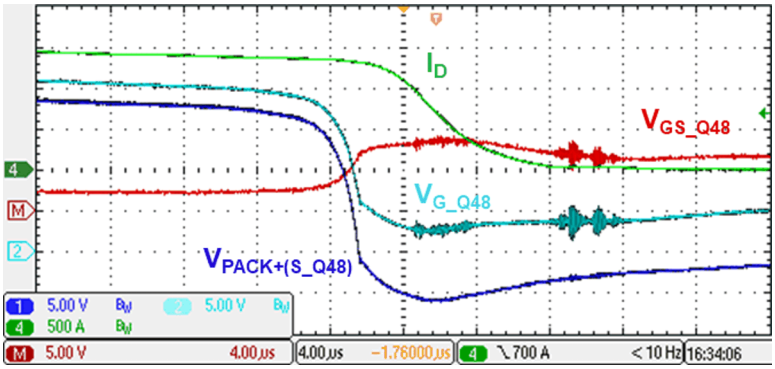

Figure 3-4. Turning Off Discharge MOSFET With Q48 at SCD

4 Current Consumption of Stacked Groups

The TIDA-010247 design guide describes the auxiliary power strategy of the stacked BQ769x2 design. In standby mode with the MOSFETs on (DET pulled low to ground), TIDA-010247 has about 300-µA total current consumption and about 10-µA current gaps between stacked groups. If the MOSFETs are off (DET floating), the total current consumption decreases to about 200 µA and the current gap increases to about 50 µA. TIDA-010247 utilizes the top BQ769x2 charge pump to switch the MOSFETs on and off; therefore, there is larger current consumption from the top BQ769x2 with the MOSFETs on causing larger total current consumption than the MOSFET off condition. In standby mode, the host MCU switches off ISO1640 power supply and disables the DC-DC LM5168P by pulling EN low to save power, and the 5-V and 3.3-V rails are provided by the bottom BQ769x2 regulator. There is about 50-µA total current including the MCU, transceiver, and other leakage current causing the current gaps since there is no further current consumption from the top BQ769x2, except the IC supply current. An external IO circuit is designed in TIDA-010247 to detect if the battery is attached with a load or charger. Choosing the appropriate pullup resister (R178) is helpful to shrink the current gaps with DET attached (which allows the MOSFETs to turn on). This is especially helpful for a specific working condition.

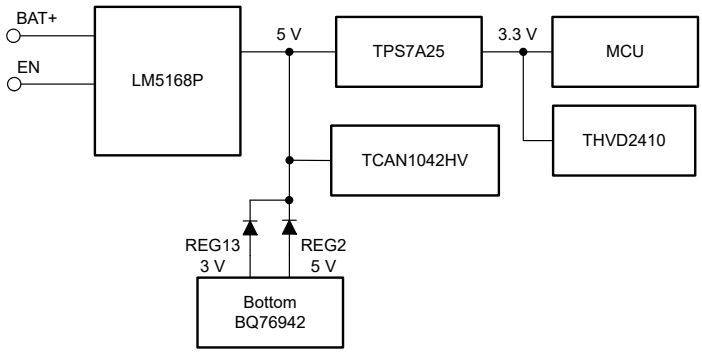

Figure 4-1. TIDA-010247 Auxiliary Power Strategy

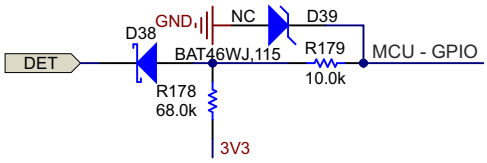

Figure 4-2. DET Circuit to Detect Charger or Load in TIDA-010247

When a charging or discharging current wakes up the TIDA-010247, the DC-DC is enabled, taking over the 5-V and 3.3-V rail and does not cause an imbalanced current. The I2C isolator ISO1640 is still powered by the top and bottom BQ769x2 regulators separately to reduce the imbalanced current (see Figure 2-1, Figure 2-1).

The supply current specifications of the ISO1640 device are listed in Table 4-1. The supply current gaps of the ISO1640 device contribute the most group imbalance current under normal working conditions.

Table 4-1. ISO1640 Supply Current Characteristics (3 V ≤ VCC1, VCC2 ≤ 3.6 V)

Parameter		Test Conditions	MIN	TYP	MAX	Unit
ICC1	Supply Current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open		5.2	7.1	mA
		VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open		3	4	mA
ICC2	Supply Current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open		4.9	6.7	mA
		VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open		2.8	3.5	mA

A good way to further decrease the current gaps is to add TI *isolated power modules* to power the secondary sides of ISO1640 and use the main 3.3-V rail to power the isolated power module and ISO1640 primary side. Figure 4-3 shows the block diagram.

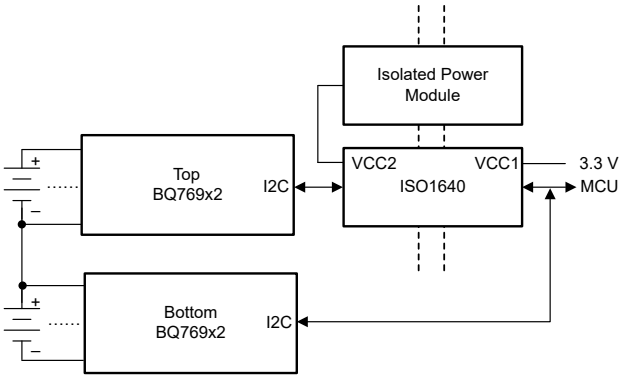

Figure 4-3. Power ISO1640 With Isolated Power Module

Both sides of the ISO1640 device are powered by the main 3.3-V rail, since the main 3.3-V rail is designed to sink power from the total pack voltage, eliminating further current gaps between groups.

Since the BQ769x2 device also supports SPI communications with the host MCU, another solution is to replace I2C with SPI communication and use the TI ISOW7741 device. The ISOW7741 is a digital isolator integrated DC-DC converter. ISOW7741 achieves the isolation of SPI communication and integrates isolated DC-DC to power the secondary side. All power comes from the main 3.3-V rail which results in no imbalanced current.

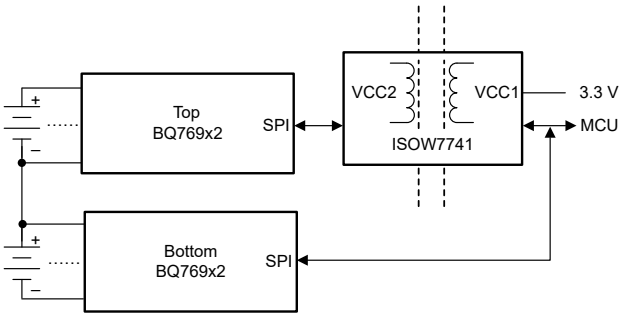

Figure 4-4. Isolated SPI Communication With ISOW7741

The TIDA-010247 also reserves external pack balancing functions through REG2 of both the top and bottom BQ769x2. The host MCU can enable either BQ769x2 REG2 to start pack balancing, but needs to note the maximum balancing current must follow the BQ769x2 regulator current limitations.

5 Summary

The stacked BQ769x2 family monitor design is able to monitor 60 V and above Li-ion, LiFePO4 battery packs and achieve robust and fast high-side MOSFET drive to secure battery safety without external driver devices. This document analyzed some external discrete components in detail to describe how those parts benefit the data and commands communications between the host MCU and both the top and bottom BQ769x2. The high-side MOSFET drive architecture benefits system safety and communications but requires further design efforts to secure robust and safe MOSFET switching. The stacked architecture causes group imbalance because of current consumption gaps between the stacked groups, harming the total battery run time and lifetime. Several designs are introduced in this document to shrink the current gaps at different working conditions. The TIDA-010247 is a good reference of stacked BQ769x2 family monitor design, for 60 V and above battery packs designs.

6 References

1. Texas Instruments, TIDA-010247 *High-Side N-MOSFET Control (Up to 32s) Battery Pack Reference Design With Stacked Battery Monitor* design guide
2. Texas Instruments, ISO164x Hot-Swappable Bidirectional I2C Isolators with Enhanced EMC and GPIOs data sheet
3. Texas Instruments, *BQ76952 3-Series to 16-Series High Accuracy Battery Monitor and Protector for Li-Ion, Li-Polymer, and LiFePO4 Battery Packs* data sheet
4. Texas Instruments, BQ76952 *Technical Reference Manual*
5. Texas Instruments, *BQ769x2 Calibration and OTP Programming Guide* application note
6. Texas Instruments, Multiple FETs with the BQ769x2 Battery Monitor application note

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